TANDY®

Service Manual

26-3901

TANDY 600
PORTABLE COMPUTER

Catalog Number: 26-3901



CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

PREFACE

This manual is designed for service personnel in the field and at repair centers who have maintenance responsibility for the TANDY 600.

A basic knowledge of the 80C88 microprocessor, as well as the 81C55PI0, 82C51USART, WD2797 FDC and HD61830, is required in order to use this manual. Appendix C contains information on the microprocessor and LSI chips.

This manual is organized as follows:

Section 1 Hardware specifications

Section 2 Connectors, switches and controls

Section 3 Disassembly instructions

Section 4 Maintenance and adjustments

Section 5 Operations

Section 6 Troubleshooting

Section 7 Exploded views and parts list

Section 8 Circuit diagrams

Section 9 PCB views

Appendix A Description of I/O commands

Appendix B Character code table

Appendix C Documentation of Microprocessor and LSI

Appendix D Installation of optional RAM and ROM

NOTE: The following is a comparison of the labels on the boards and their meanings:

OPKK Board: Keybard PCB
OPLF Board: LCD Controller
OPMP Board: Main PCB
OPRM Board: RAM Card

Table of Contents

		Page
Section 1	**HARDWARE SPECIFICATIONS**	1
	1.1 Front View	1
	1.2 Keyboard Layout	1
	1.3 Hardware Specifications	2
Section 2	**CONNECTORS, SWITCHES AND CONTROLS**	5
	2.1 Connectors	5
	2.2 Switches	5
	2.3 Controls	6
Section 3	**DISASSEMBLY INSTRUCTIONS**	7
	3.1 Unit and Boards	7
	3.2 FDD Unit	15
Section 4	**MAINTENANCE AND ADJUSTMENTS**	27
	4.1 Cleaning	27
	4.2 Modem Transmission Level Calibration	27
	4.3 FDD Controller Calibration	29
	4.4 Real Time Clock (RTC) Calibration	29
	4.5 FDD Unit Calibration	30
Section 5	**OPERATIONS**	43
	5.1 Overview	43
	5.2 CPU	44
	5.3 Storage	47
	5.4 I/O	53
	5.5 Interrupts	57
	5.6 Keyboard	61
	5.7 Floppy Disk Drive (FDD)	65
	5.8 Printer Interface	81
	5.9 LCD	82
	5.10 Serial Interface	96
	5.11 Buzzer Control	107
	5.12 Real Time Clock (RTC)	108
	5.13 Power Supply Control and DC/DC Converter	112
Section 6	**TROUBLESHOOTING**	117
	6.1 Troubleshooting Flowchart	118
	6.2 Check List	142
Section 7	**EXPLODED VIEW AND PARTS LIST**	143
	7.1 Exploded View	143
	7.2 Parts List	146
Section 8	**CIRCUIT DIAGRAMS**	175
	8.1 Circuit Diagrams	175

Section 9 **PCB VIEWS** 193
9.1 Main PCB Views 193
9.2 Keyboard PCB Views 198
9.3 LCD Controller Board Views 199

Appendix A **DESCRIPTION OF I/O COMMANDS** 201

Appendix B **CHARACTER CODE TABLE** 223

Appendix C **DOCUMENTATION OF MICROPROCESSOR AND LSI** 231
C.1 MSM80C88 231
C.2 MSM82C84ARS 241
C.3 MSM81C55RS (PIO) 245
C.4 HD146818 (Real-Time Clock Plus RAM) 249
C.5 MSM825C51ARS 253
C.6 MSM6946RS 259
C.7 MSM6234RS 264
C.8 HM6264LP-15 268
C.9 HM6264LFP-15 271
C.10 HN613256P 274
C.11 WD2797 276
C.12 μPD8257 281
C.13 HD61830 287

Appendix D **INSTALLATION OF OPTIONAL RAM AND ROM** 303
D.1 Installation of Optional RAM Card 303
D.2 Installation of Optional ROM Chip 304

List of Illustrations

FIGURE NUMBER	DESCRIPTION	PAGE
3-1	Front Bezel Assembly	16
3-2	PCB Assembly	17
3-3	TR 00 Sensor Assembly	18
3-4	Carriage Assembly	19
3-5	Steel Belt Assembly	20
3-6	Sealed Wire Harness	20
3-7	Spindle Motor Assembly	21
3-8	Stepping Motor Assembly	22
3-9	Steel Belt Assembly	22
3-10	M Carriage Assembly	23
3-11	Head Carriage Assembly	24
3-12	E level Set	24
3-13	Level Set	25
3-14	M Carriage Set	25
4-1	Test Point Position	28
4-2	Test Point Position	29
4-3	Test Point Position	30
4-4	TPA-1 AMP Output Waveform	31
4-5	Adjusting Motor Extension Cable Installation Diagram	32
4-6	Track 00 Sensor Position Adjusting Waveform	33
4-7	INDEX SIGNAL Adjusting Waveform	34
4-8	Position of Spindle Motor Adjusting VR	35
4-9	Spindle Motor Adjusting VR Turning Method	35
4-10	INDEX TIMING Adjusting Waveform	36
4-11	Offset Adjusting Waveform	37
4-12	Track Adjusting Waveform	38
4-13	Step Motor Adjusting Waveform	39
4-14	Azimuth Adjusting Waveform	40
4-15	Relationship between Azimuth and Pattern	40
4-16	Read Waveform Diagram	41
4-17	Modulation Check Waveform Diagram	42
4-18	Stopper Adjustment	42
5-1	Block Diagram	43
5-2	82C84 and Peripheral Circuits	45
5-3a	READY Control Circuit	46
5-3b	READY Control Timing Chart	47
5-4	Memory Map	48
5-5	Memory Address Decoder Circuit	50
5-6	Standard Memory Block Diagram	51
5-7	Optional RAM Block Diagram	52
5-8	ROM Block Diagram	53
5-9	I/O Address Decorder Circuit	55
5-10	Ports A – C	56
5-11	Port D	56
5-12	Port E	57
5-13	Interrupt Control Circuit	58
5-14	NMI Circuit	59
5-15	RTC Interrupt Generation Circuit	59

FIGURE NUMBER	DESCRIPTION	PAGE
5-16	TRC Interrupt Generation Circuit	60
5-17	FDC Interrupt Generation Circuit	60
5-18	81C55 Interrupt Generation Circuit and Timing Chart	61
5-19	Capacitive Key Input Circuit and Timing Chart	62
5-20	Mechanical Key Input Circuit and Timing Chart	63
5-21	Capacitive Key Design and Timing Chart	64
5-22	FDD and Peripheral Circuitry Block Diagram	65
5-23	FDD Conrol Program General Flowchart	66
5-24	Block Diagram of DMAC and Peripheral Circuitry	67
5-25	DMA Transmission Start Sequence	68
5-26	DMA Operation Timing Chart	69
5-27	DMA Transmission Address Constitution	69
5-28	WD2797 CPU Interface Circuit and Timing Chart	70
5-29	FDD interface Circuit Diagram	71
5-30	WD2797 VF0 and Data Separator	72
5-31	STEP Signal Waveform	75
5-32	Data Write Timing	76
5-33	INDEX Signal Waveform	76
5-34	Data Read Timing	77
5-35	Control Timing	78
5-36	Control CPU Process Flowchart	80
5-37	Printer Interface Circuit Diagram and Timing	81
5-38	LCD Block Diagram	82
5-39	HD61830 CPU Interface Circuit Diagram	83
5-40	HD61830 VRAM Interface Circuit Diagram and Timing Chart	84
5-41	HD61830 LCD Interface Circuit Diagrm and Timing Chart	86
5-42	Abbreviated LCDC Control Program Flowchart	87
5-43	Display Screen Memory Configuration	88
5-44	Construction of LCD Panel	89
5-45	Operation Theory of LCD Board	90
5-46	Matrix Configuration	90
5-47	LCD View Angle	91
5-48	HD61103 Internal Circuitry	92
5-49	HD61100 Internal Circuitry	92
5-50	LCD Unit Screen Constitution	94
5-51	LCD Unit Interface Timing Chart	94
5-52	LCD Waveform	95
5-53	Serial Interface Block Diagram	96
5-54	USART (82C51A) Pin Layout Definitions	98
5-55	MODEM/RS232C Switching Circuit	99
5-56	RS232C Interface Circuit	100
5-57	Modem Circuit Diagram and Timing Chart	101
5-58	Modem Connector Interface and Ring-Detection Circuit	103
5-59	Serial Interface Interrupt Control	105
5-60	Auto-Dialing Circuit Diagram and Timing Chart	106
5-61	Buzzer Control Diagram	107
5-62	RTC Address Map	109
5-63	IRQ Signal Waveform	109
5-64	HD146818 Peripheral Circuitry	111
5-65	HD146818 Timing Chart	111

FIGURE NUMBER	DESCRIPTION	PAGE
5-66	Power Supply Control Circuit Diagram	113
5-67	Power ON/OFF Sequence Timing Chart	114
5-68	DC/DC Converter Circuit Diagram	115
5-69	Vc Waveform of TR6	116
8-1	General Circuit Diagram	175
C-1	MSM80C88 Block Diagram	231
C-2	MSM80C88 Pin Configuration	231
C-3a	Memory Organization	236
C-3b	Reserved Memory Locations	236
C-4	Basic System Timing	239
C-5	Interrupt Acknowledge Sequence	241
C-6	MSM82C84ARS Terminal Connection	241
C-7	MSM82C84ARS Circuit Configuration	242
C-8	MSM82C84ARS CLOCK and RESET Signal Timing Chart	244
C-9	MSM82C84ARS READY Signals Timing Chart	244
C-10	MSM81C55RS Terminal Connection	245
C-11	MSM81C55 Circuit Configuration	245
C-12	MSM81C55 Read Cycle Timing Chart	247
C-13	MSM81C55 Write Cycle Timing Chart	247
C-14	MSM81C55 Strobed Input Mode Timing Chart	248
C-15	MSM81C55 Storbed Output Mode Timing Chart	248
C-16	MSM81C55 Basic Input Mode Timing Chart	248
C-17	MSM81C55 Basic Output Mode Timing Chart	249
C-18	MSM81C55 Timer Timing Chart	249
C-19	HD146818 Circuit Configuration	250
C-20	HD146818 Terminal Connection Diagram	250
C-21	MSM82C51ARS Circuit Configuration	253
C-22	MSM82C51ARS Terminal Connection	253
C-23	MSM82C51ARS Write Data Cycle Timing Chart	255
C-24	MSM82C51ARS Read Data Cycle Timing Chart	255
C-25	MSM82C51ARS Transmitter Control and Flag Timing Chart (ASYNC MODE)	256
C-26	MSM82C51ARS Transmitter Clock and Data Timing Chart	256
C-27	MSM82C51ARS Receiver Clock and Data Timing Chart	257
C-28	MSM82C51ARS Receiver Control and Flag Timing Chart	257
C-29	MSM82C51ARS Write Control or Output Port Timing Chart	258
C-30	MSM82C51ARS Read Control or Input Port Timing Chart	258
C-31	MSM6946RS Terminal Connection	259
C-32	MSM6946RS Circuit Configuration	259
C-33	MSM6946RS Timing Chart	263
C-34	MSM6234RS Terminal Connection	264
C-35	MSM6234RS Circuit Configuration	264
C-36	MSM6234RS TONE OUT Terminal Output Control Timing Chart	266
C-37	MSM6234RS Relationship between R_1-R_4, C_1-C_4 and TONE OUT Timing Chart	267
C-38	HM6264LP-15 Terminal Connection	268
C-39	HM6264LP-15 Circuit Configuration	268
C-40	HM6264LP-15 Read Cycle Timing Chart	269
C-41	HM6264LP-15 Write Cycle (OE) Timing Chart	270
C-42	HM6264LFP-15 Terminal Connection	271
C-43	HM6264LFP-15 Circuit Configuration	271
C-44	HM6264LFP-15 Read Cycle Timing Chart	272

FIGURE NUMBER	DESCRIPTION	PAGE
C-45	HM6264LFP-15 Write Cycle (OE) Timing Chart	273
C-46	HN613256P Terminal Connection	274
C-47	HN613256P Circuit Configuration	274
C-48	HN613256P Timing Chart	275
C-49	WD2797PL-02 Circuit Configuration	276
C-50	WD2797PL-02 Terminal Connection	277
C-51	WD2797LFP-02 CPU Interface Timing Chart	279
C-52	WD2797 SEEK Timing Chart	280
C-53	WD2797 WRITE DATA Timing Chart	280
C-54	WD2797 READ DATA Timing Chart	280
C-55	μPD8257 Terminal Connection	281
C-56	μPD8257 Circuit Configuration	281
C-57	μPD8257C-5 READ Timing Chart	285
C-58	μPD8257C-5 WRITE Timing Chart	285
C-59	μPD8257C-5 DMA Mode Timing Chart (a)	286
C-60	μPD8257C-5 DMA Mode Timing Chart (b)	286
C-61	HD61830 Terminal Connection	287
C-62	HD61830 Circuit Configuration	288
C-63	Mode Control Register	292
C-64	HD61830 CPU Interface Timing Chart	300
C-65	HD61830 External RAM and ROM Interface Timing Chart	300
C-66	HD61830 and LCD Unit Interface Timing Chart	301
D-1	Optional RAM Installation	303
D-2	Optional ROM Installation	304

List of Tables

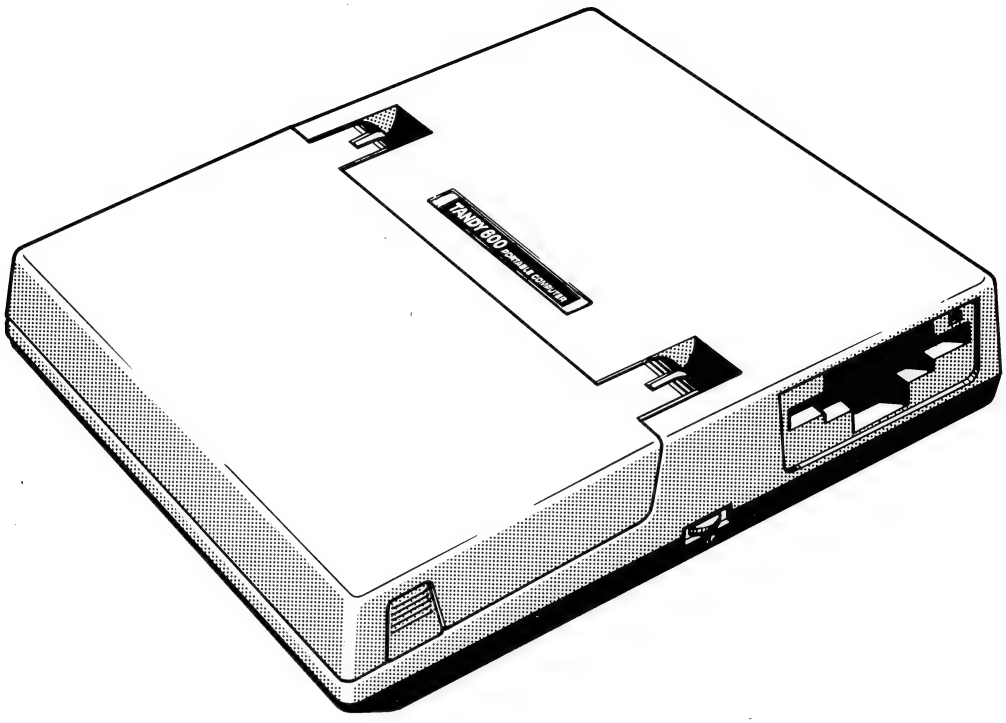
TABLE NUMBER	DESCRIPTION	PAGE
5-1	Memory and Capacity	47
5-2	Function Table	49
5-3	I/O Map	54
5-4	Interrupt Level and Type	57
5-5	Interrupt Vector	57
5-6	Supplied +5V$_2$ Part	73
5-7	Signal Connector Pin Array	74
5-8	Power Supply Connector Pin Array (CN$_2$)	79
5-9	LCD Interface Signals	85
5-10	Relationship between Segment Data and Common	93
5-11	Power Supply Usage	116
A-1	Contents of WD2797 Status Register	204
C-1	S3 and S4 Signals	232
C-2	S0, S1 and S2 Signals	235
C-3	QS0 and QS1 Signals	235
C-4	Segment and Register	237

TABLE NUMBER	DESCRIPTION	PAGE
C-5	S0, S1 and S2 Signals	238
C-6	S3 and S4 Signals	238
C-7	Relationship between TONE OUT Terminal and Output Frequency	266
C-8	Character Display and Graphics Mode	299

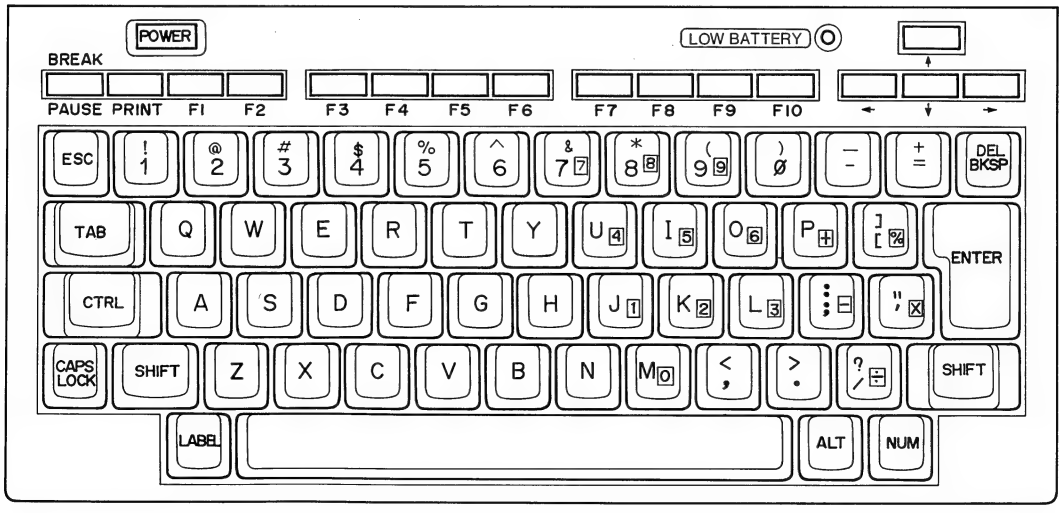
Section 1
HARDWARE SPECIFICATIONS

SECTION 1 – – HARDWARE SPECIFICATIONS

1.1 Front View



1.2 Keyboard Layout



1.3 Hardware Specifications

(1) CPU MSM80C88

(2) CPU Clock 3.07 MHz

(3) RAM

Standard:	32K bytes
Total:	224K bytes
Chip:	64K bits S-RAM
RAM retention:	Data in all RAMs is retained by a backup battery while power is off.

(4) ROM

Standard:	160K bytes
Total:	160K bytes
Chip (standard):	256K bits MASK ROM

(5) Display

Effective display area:	230 (W) × 61 (H)mm
Number of pixels:	480 (W) × 128 (H)
Pixel size:	0.43 × 0.43mm
Gap between pixels:	0.05mm
Controller:	HD61830
Display memory:	64K bits S-RAM × 2
Contrast:	Operating voltage adjusted by control
Number of characters on display:	80 characters × 16 lines
Character construction:	6 × 8 dot matrix

(6) Keyboard

Number of keys:	72
Key top type:	Step sculpture
Key switch:	Capacitive type × 56 Mechanical type × 16
Depression force	
Capacitive key:	70 ± 30g
Capacitive space key:	150g
Mechanical key:	300g
Key stroke	
Capacitive key:	4mm
Mechanical key:	0.3mm
Keyswitch life	
Capacitive key:	30 million operations
Mechanical key:	5 million operations
Power On/Off switch:	100,000 operations (mechanical)

(7) FDD

FDD drive	
Memory capacity (unformatted):	500K bytes
Recording density:	8187 BPI
Data transfer rate:	250K bits/sec.
Track density:	135 TPI
Number of tracks:	80
Recording method:	MFM
Rotating speed:	300 RPM
Latency (average):	100 msec.
Access time	
Track-to-track:	3 msec.
Settling:	30 msec.
FDD controller:	WD2797
DMA controller:	μPD8257
Power saving:	Power to the FDD, FDC and DMAC automatically goes off when an FDD is not accessed for 5 seconds.

(8) Modem/Coupler

Baud rate:	300 bps
Program items	
Data length:	6, 7 or 8
Parity:	None, odd or even
Stop bit:	1 or 2
Auto-dialing function (selected by software)	
Pulse dialing:	10 pps/20 pps (software selected) 255-dial digits
Tone dialing:	Controller (MSM6234RS)
Ring detector function:	Ringing tone triggers "CPU Wake-up Functions" when power is off.
Auto-answering function:	Available
Communication mode:	Full duplex/half duplex
Operating mode:	Originate/answer
Modulation mode:	F.S.K

(9) RS232C

Standard:	EIA RS232C
Program items:	Data length of 6, 7 or 8 None, odd or even parity Stop bit 1 or 2 Baud rate of 110, 300, 600, 1200, 2400, 4800, 9600 or 19200
Communication mode:	Full duplex/half duplex
Operating mode:	DTE

(10) Calendar Clock

Controller:	HD146818
Calendar set:	Year, month, day, day of week, hour, minute
Calendar read:	Year, month, day, day of week, hour, minute, second
Alarm set:	Month, day, hour, minute
Alarm operation	
If power is off:	CPU Wake up
If power is on:	CPU Interrupt
Clock retention:	HD146818 is retained by a backup battery when power is off.

(11) Printer Interface (Centronics standard)

Handshake signals:	$\overline{\text{STROBE}}$, BUSY, $\overline{\text{BUSY}}$

(12) Operation Battery (main battery)

Type:	4/4000 RS

(13) Backup Battery (sub-battery)

Type:	51FT-P (3.6V 50 mAh)
Mounting:	On the main board (OPMP board)
Charging:	Through the main battery
Retention:	All RAMs, calendar clock

(14) Auto-power Off

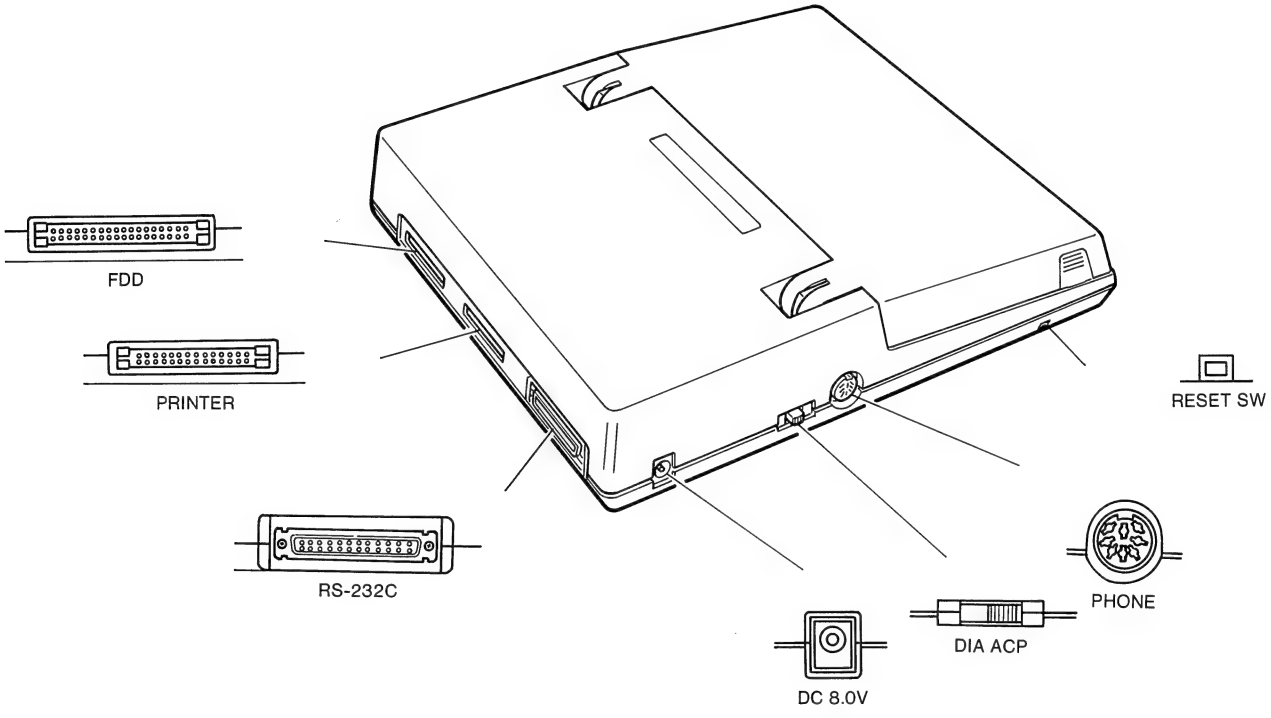
The main battery goes off automatically when no data is keyed in for 10 minutes.

Section 2
CONNECTORS, SWITCHES AND CONTROLS

SECTION 2 – – CONNECTORS, SWITCHES AND CONTROLS

2.1 Connectors

RS232C:	25 pins (RDBD25S)
Printer:	26 pins (FRC2-C26)
Modem:	8 pins (TCS-4490)
Optional floppy disk drive:	34 pins (FRC2-C34)
AC adapter:	5.5mm diameter (center-minus)



2.2 Switches

The **POWER switch**, located on the keyboard, is a toggle-action switch that alternately turns the power supply on and off when pressed.

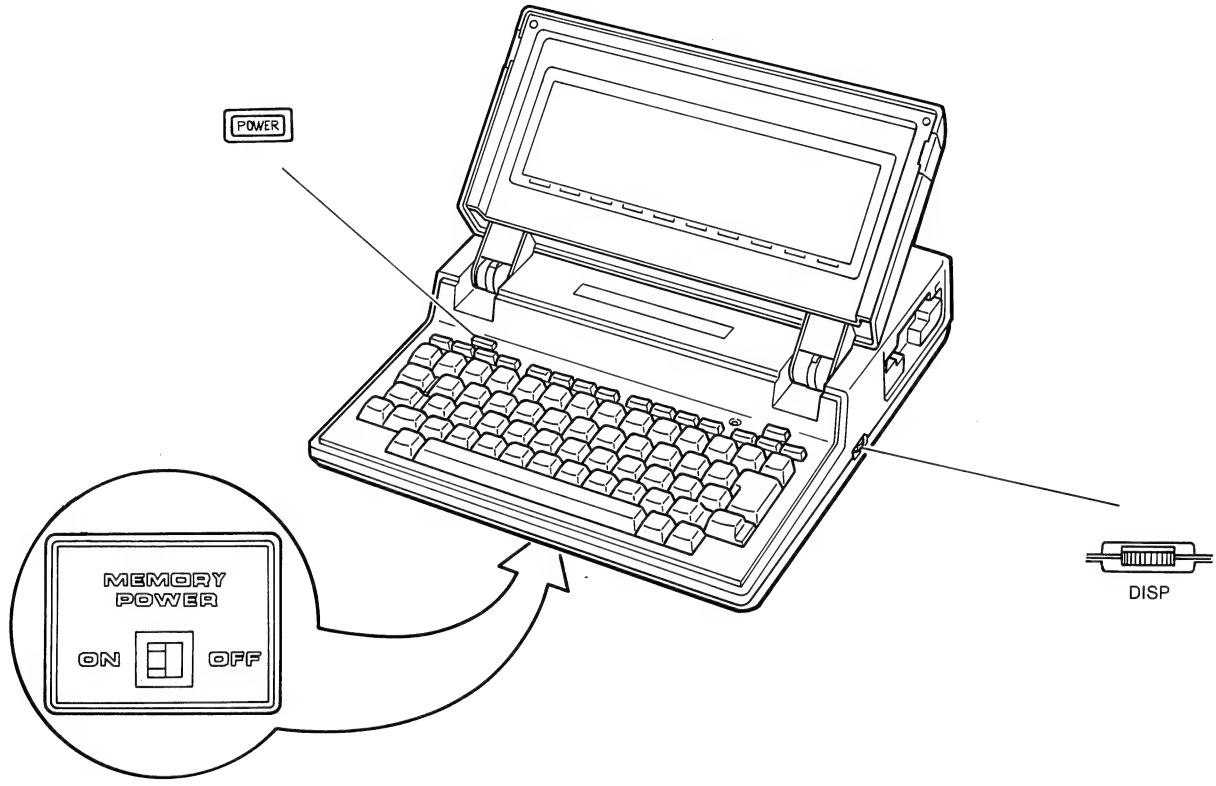
The **DIR/ACP selector switch** selects direct or acoustic coupling for the serial interface. The DIR setting enables direct communication via telephone line; the ACP setting enables communication via acoustic coupler.

The **MEMORY POWER switch** protects the nickel-cadmium battery used for backing up the RAM from discharging. The discharge protection function does not operate when the switch is set to OFF. It should be set in the OFF position when the unit is not to be used for an extended period.

Pressing the **RESET switch** activates a cold start, which means that the system is initialized and the main menu is displayed. An example of this switch in use is a program which enters an infinite loop.

2.3 Controls

The **DISP control** adjusts the contrast on the LCD. Set the control so that the LCD can be easily read.



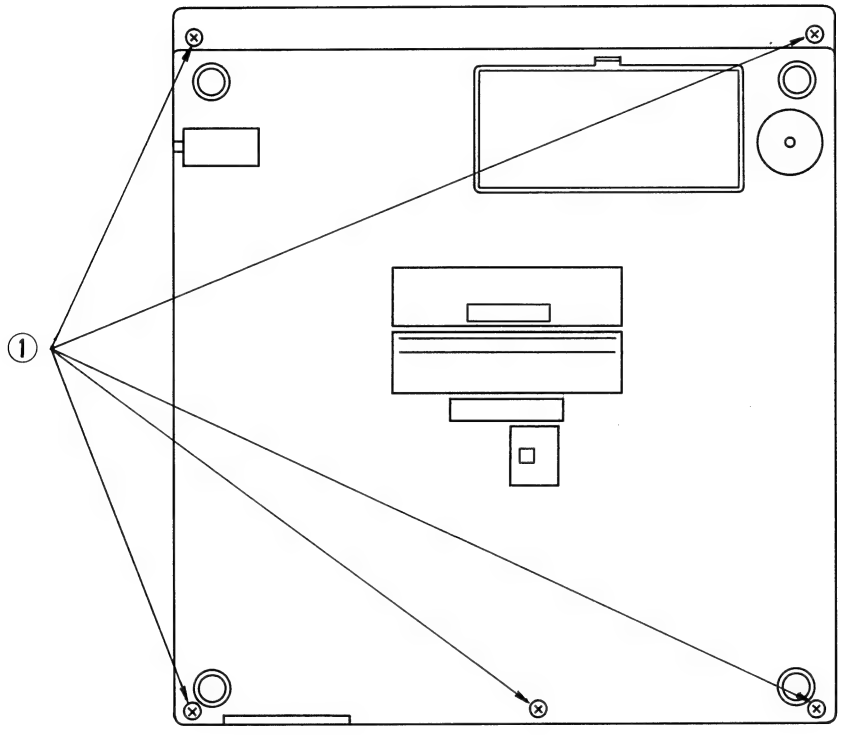
Section 3
DISASSEMBLY INSTRUCTIONS

SECTION 3 – – DISASSEMBLY INSTRUCTIONS

3.1 Units and Boards

3.1.1 Cover Assembly

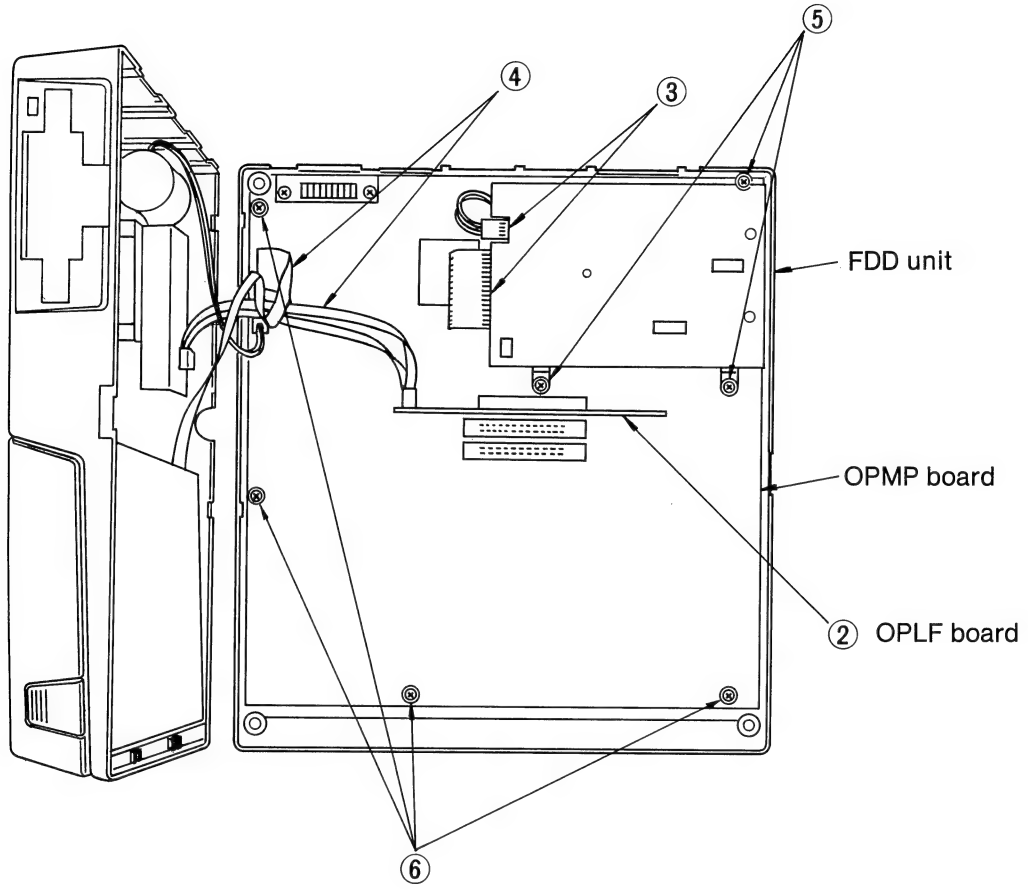
(1) Remove the five screws labeled ① from the rear panel.
(2) Carefully lift off the top cover assembly.



Note 1: Turn off the Memory Power Switch when disassembling.
Note 2: The cover is held in place both by the screws and by clips. Be careful not to break the clips when removing the cover.

3.1.2 Main Board (OPMP Board) and FDD Unit

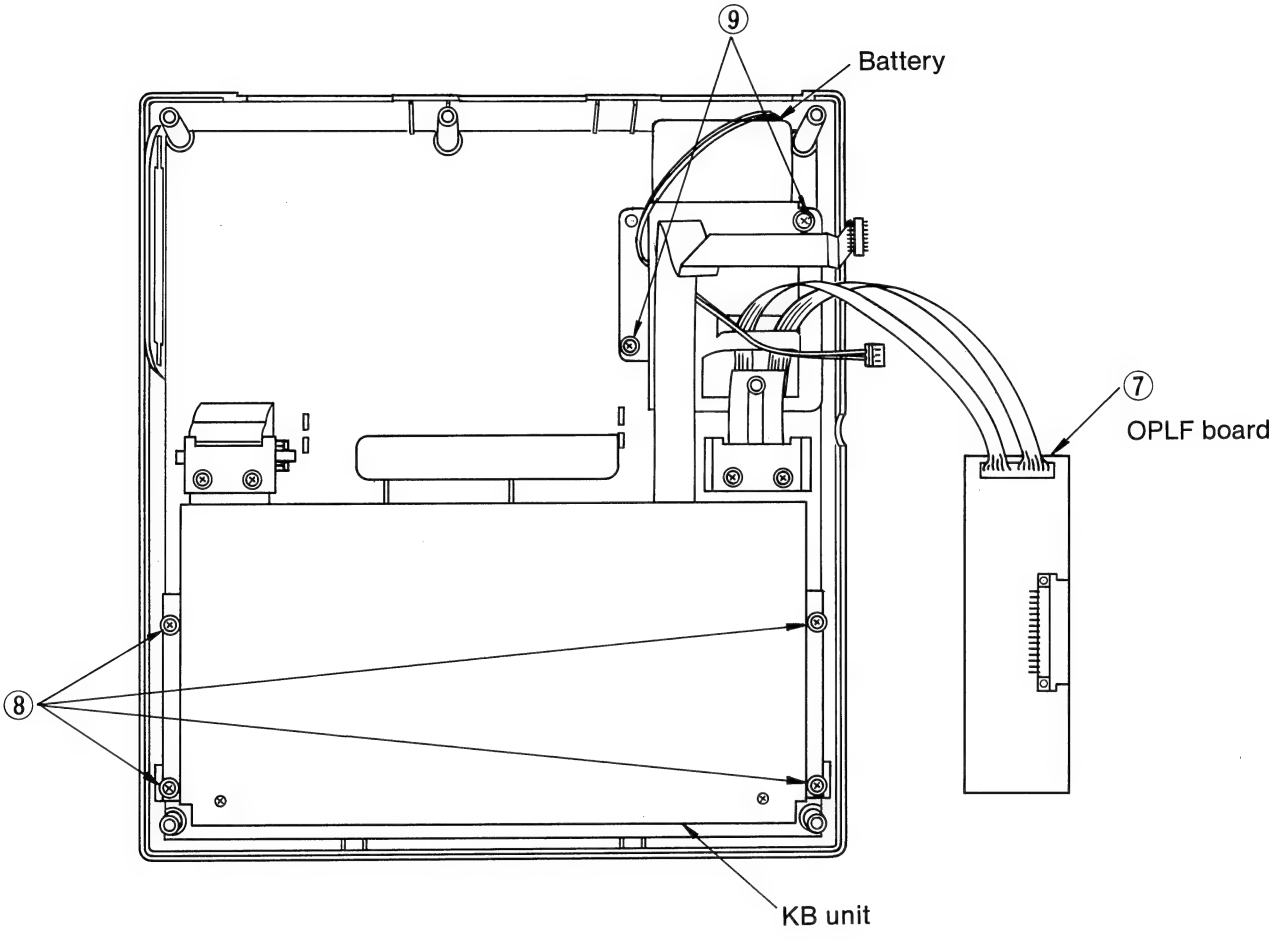
(1) Remove the OPLF board ②
(2) Remove CN11 and CN12 ③ which are connected to the FDD unit.
(3) Remove CN4, and CN9 ④
(4) Remove the three screws labeled ⑤ and lift out the FDD unit.
(5) Remove the four screws labeled ⑥ and remove the OPMP board.



Note: Be careful not to press the RESET switch when removing the OPMP board.

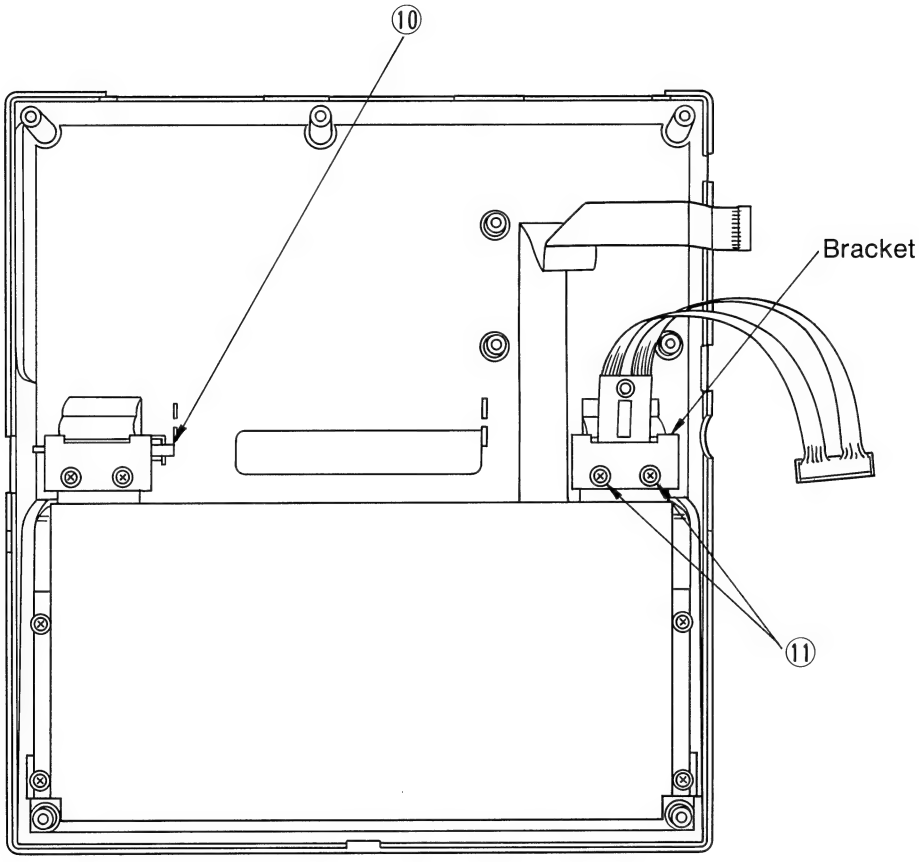
3.1.3 LCD Controller Board (OPLF Board), KB Unit and Battery

(1) Disconnect the connection to the OPLF board ⑦, then remove the OPLF board.
(2) Remove the four screws labeled ⑧, then remove the KB unit.
(3) Remove the two screws labeled ⑨ and remove the bracket and the battery.



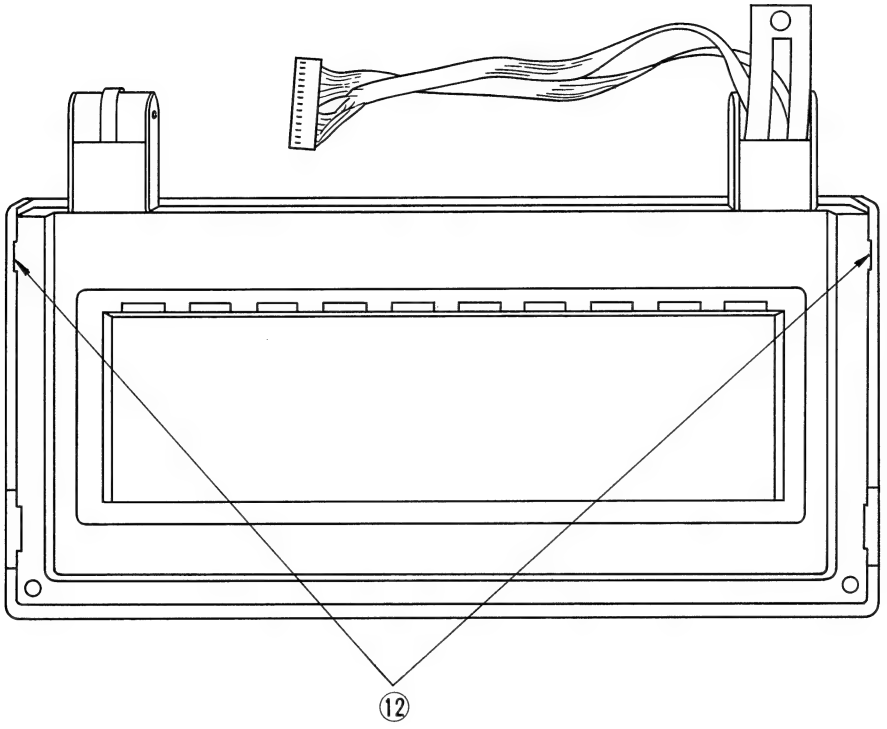
3.1.4 LCD Unit

(1) Remove the E-rings on the shafts and slide the shafts ⑩ out.
(2) Remove the set of two screws labeled ⑪ , then remove the brackets.
(3) Remove the LCD assembly.



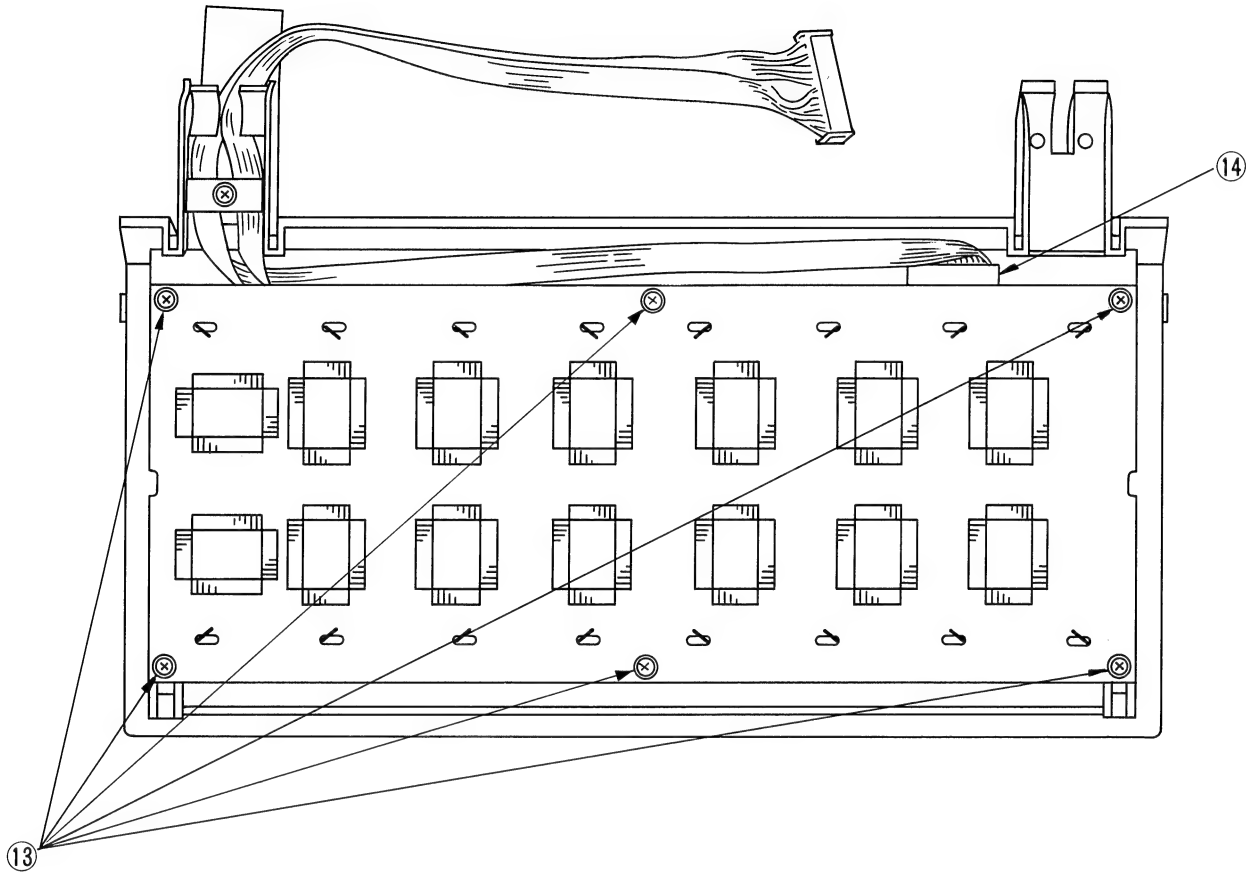
Note: Be sure that the E-rings are not lost. The shafts slide out easily if the LCD is open.

(4) Disengage the hooks ⑫ and remove the cover.



(5) Remove the six screws labeled ⑬

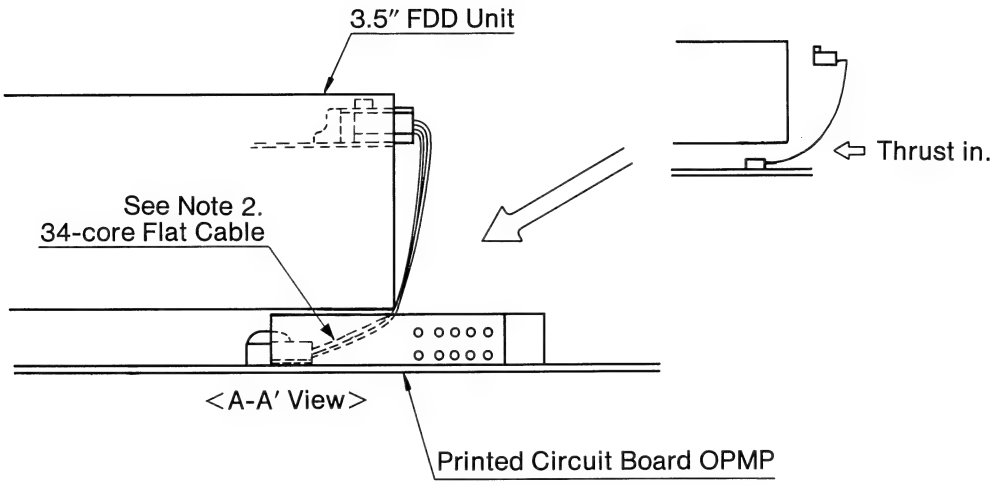
(6) Slide the LCD unit forward. Disconnect the connector ⑭ and remove the LCD unit.

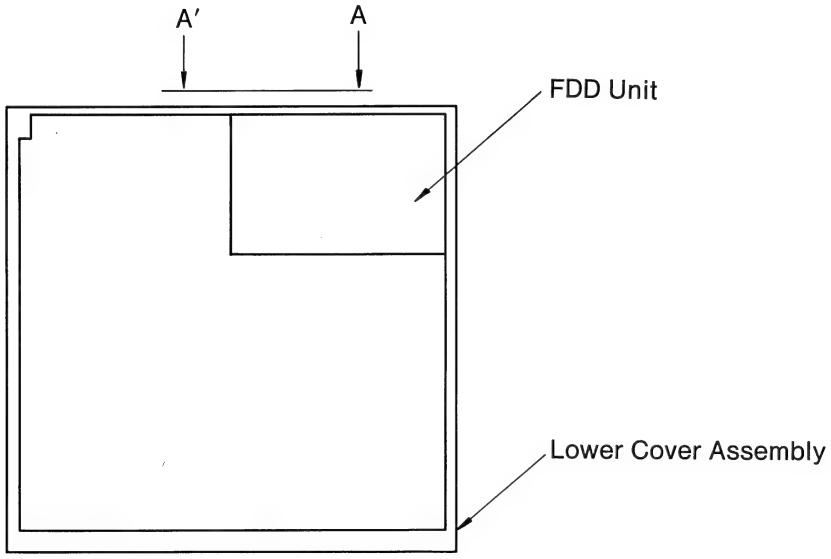


Note: Be careful not to scratch the display surface of the LCD unit.

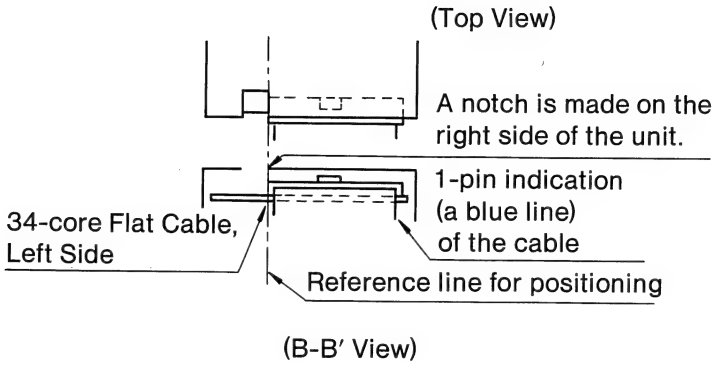
The assembly procedure is the reverse of disassembly.
Be careful when wiring the FDD unit.

Note (1): Take a wire connection route for the 34-core flat cable in a manner to thrust it under the FDD unit as illustrated below.

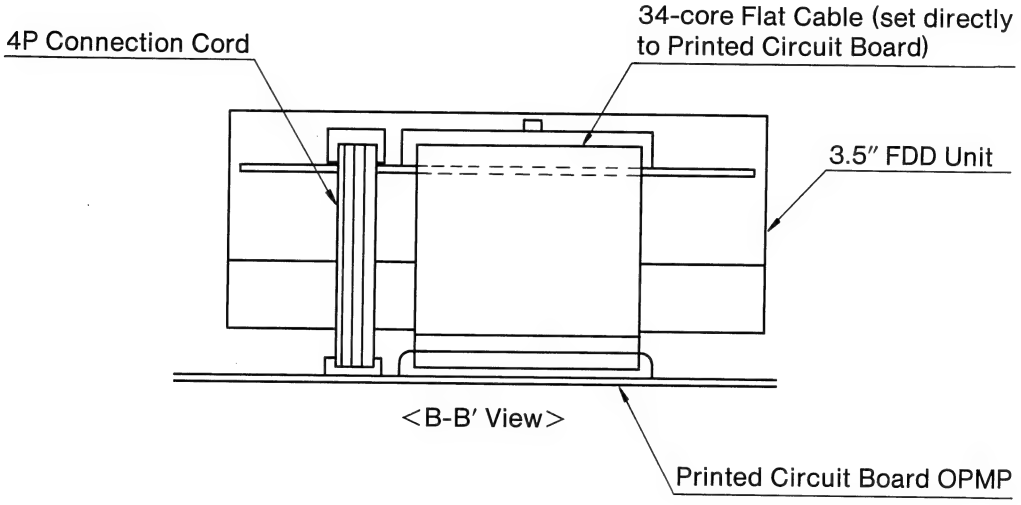


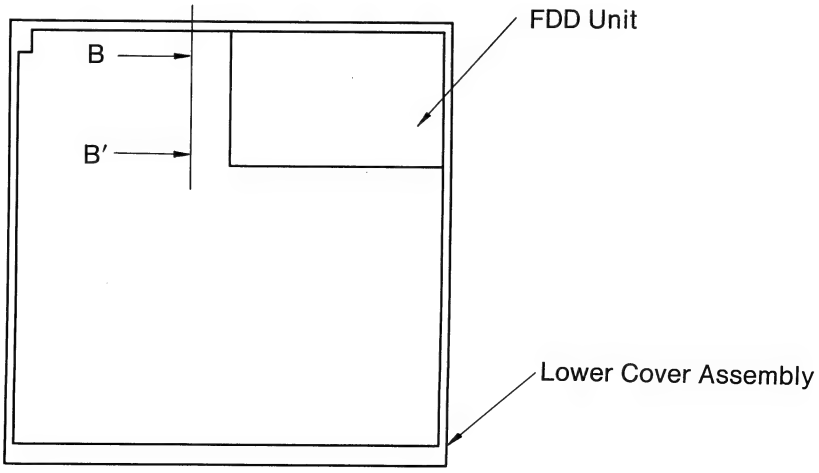


Note (2): In setting the 34-core flat cable, first align its location according to the figure below to avoid wrong insertion.
Note that the 1-pin indication (a blue line) of the cable is different from that of the FDD unit.



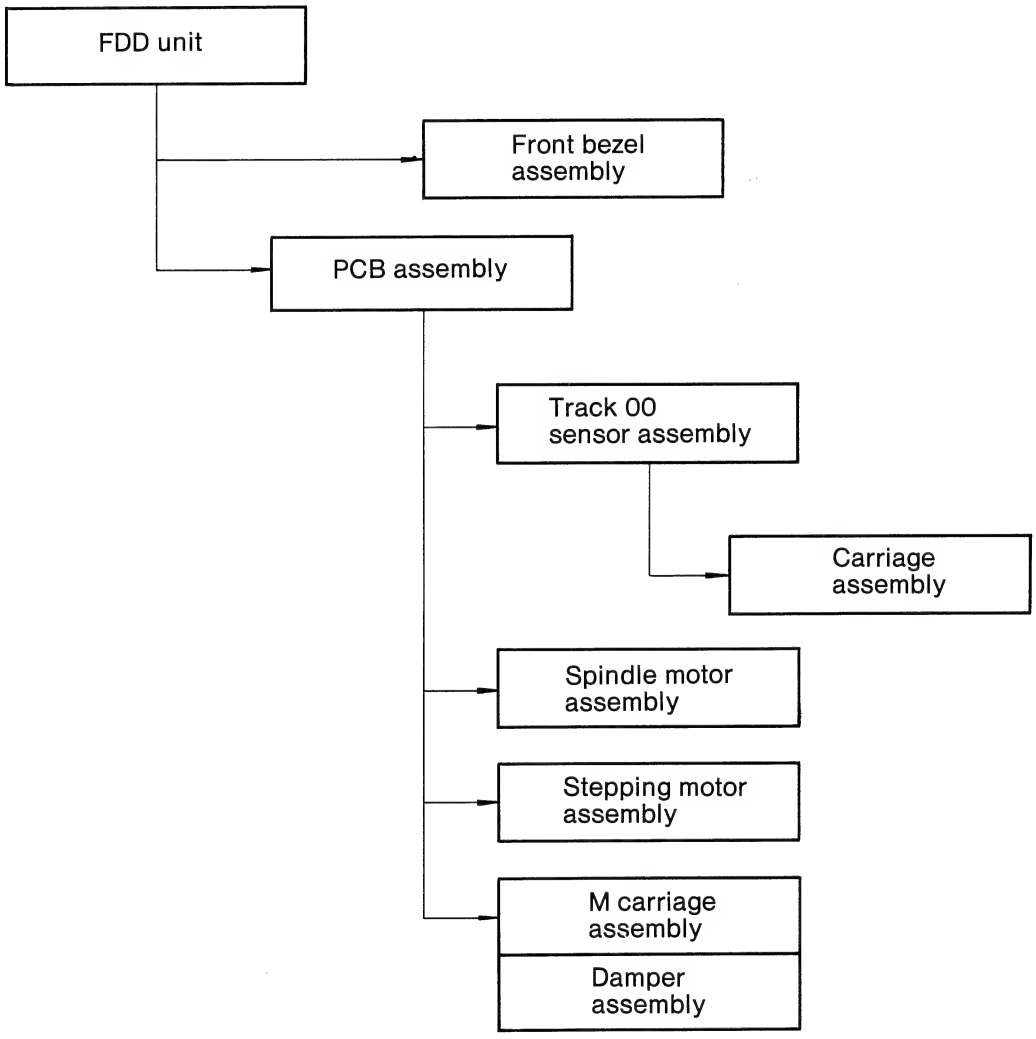
(B-B′ View)





3.2 FDD Unit

This section explains disassembly and assembly procedures for the components of the FDD unit. Calibration and function checking must be performed each time the FDD unit is disassembled.
The FDD unit consists of the following components:



3.2.1 Front Bezel Assembly (2)

(1) Remove the two screws labeled (52) from the top surface of the drive unit.
(2) Pull the front bezel assembly forward.

The assembly procedure is the reverse of disassembly. (Tightening torque must be at least 4kg-cm.)

Note: When assembling, be sure that the IN USE LED on the PCB assembly extends through the hole in the upper right corner of the front bezel.

Check
(1) Check that disks load and eject smoothly.
(2) Check that the front bezel shutter opens and closes.

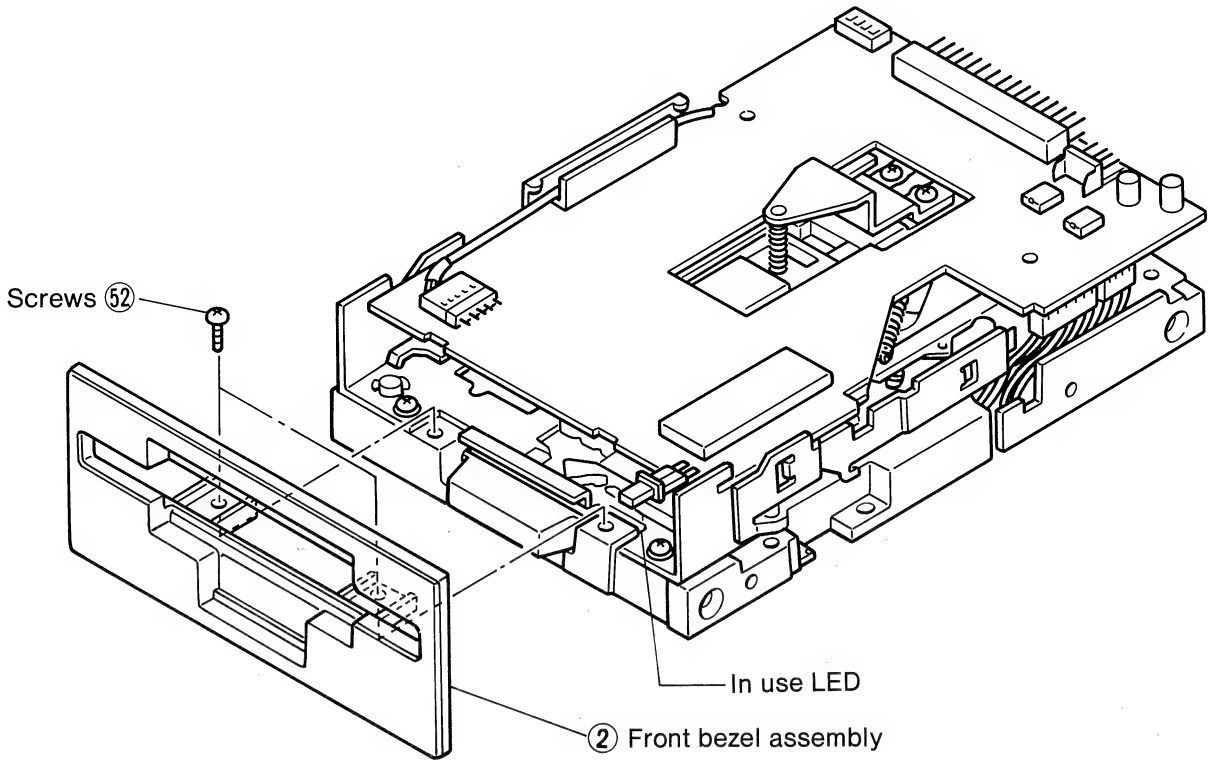


Figure 3-1. Front Bezel Assembly

3.2.2 PCB Assembly ③

Refer to the troubleshooting flowchart in section 6, the circuit diagram and the assembly diagram; repair or replace the PCB assembly ③, as necessary.

(1) Insert a disk to protect the mechanism.
(2) Remove the head connector CN3.
(3) Remove the two screws labeled ⑭ from the PCB assembly.
(4) Remove the motor connectors CN6 and CN5 and the sensor connector CN4.
(5) Slide the PCB assembly backward.
(6) Replace the faulty part in the PCB assembly, or replace the entire PCB assembly. Perform the offset calibration on the PCB assembly, as explained in **section 4.5.8** before reinstalling the PCB.

The assembly procedure is the reverse of disassembly. (Tightening torque must be at least 4kg-cm.)

Note: There must be a gap of at least 0.3mm between the PCB assembly ③ and the M carriage assembly ⑳.

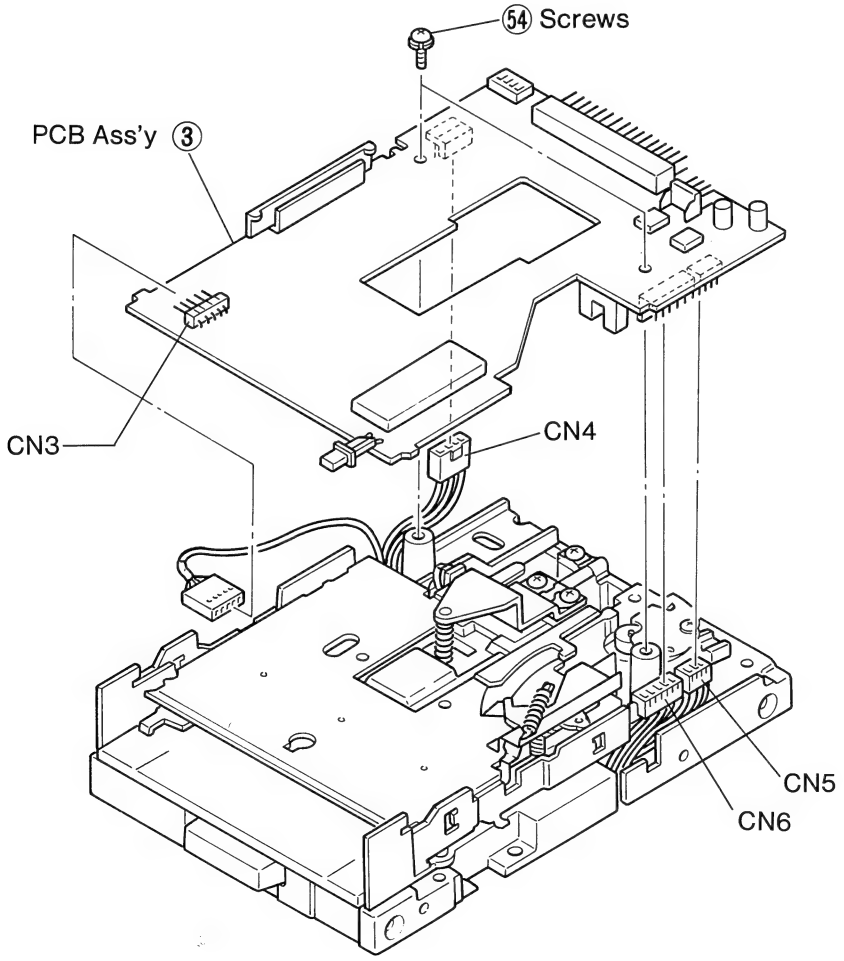


Figure 3-2. PCB Assembly

3.2.3 Track 00 Sensor Assembly (18)

(1) Remove the PCB assembly

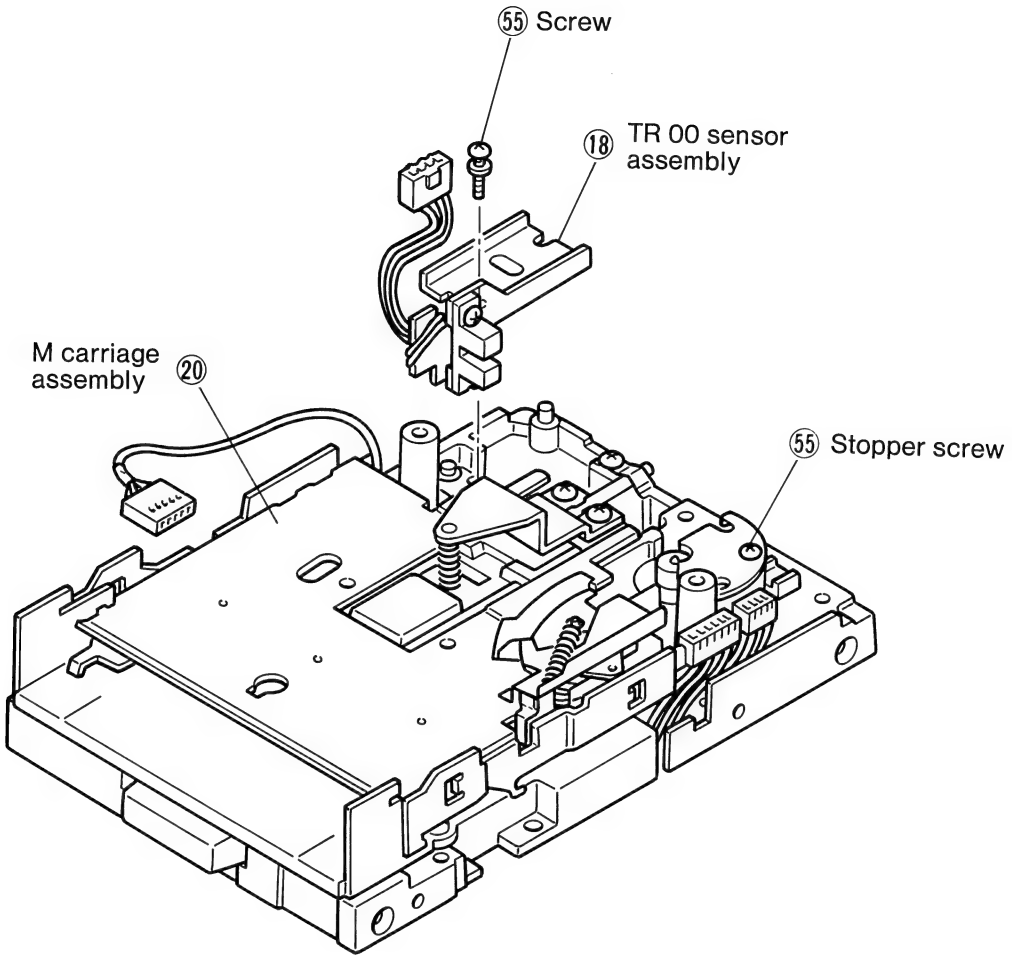


Figure 3-3. TR 00 Sensor Assembly

(2) Move the carriage assembly toward the inner tracks.
(3) Remove the screw (55) , then remove the track 00 sensor assembly.

The assembly procedure is the reverse of disassembly.

Note: Do not pinch the head cable which is held in place by the assembly.

Check
(1) Move the carriage assembly back and forth, checking that the cable moves freely.
(2) Calibrate track 00. (→ **section 4.5.5**)
(3) Calibrate the stopper. (→ **section 4.5.13**)

3.2.4 Carriage Assembly ⑪

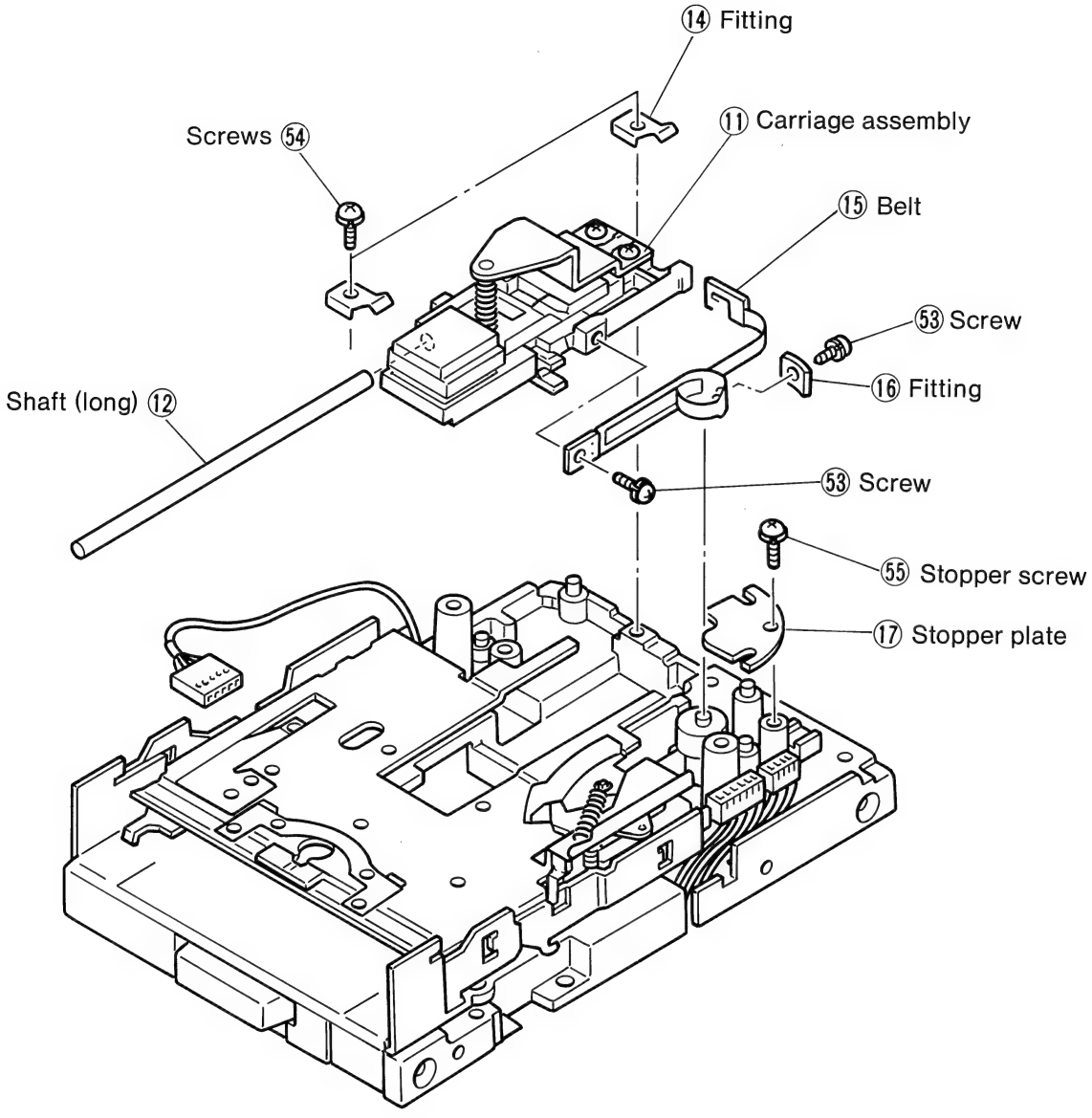


Figure 3-4. Carriage Assembly

(1) Remove the PCB assembly.
(2) Remove the TR 00 sensor assembly.
(3) Remove screw ⑤⑤ , then remove the stopper plate ⑰ .
(4) Remove screw ⑤③ from the rotor on the stepping motor, then remove the fitting ⑯ .
(5) Remove the belt ⑮ from the hook on the carriage assembly.

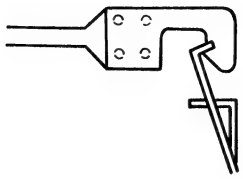


Figure 3-5. Steel Belt Assembly

(6) Remove the two screws labeled ⑤④ that secure the long shaft, then remove the fitting ⑭ .
(7) Remove the long shaft ⑫ from the carriage assembly by sliding it to the rotor.
(8) Lift the carriage assembly out.

The assembly procedure is the reverse of disassembly. Route the head cable as shown in Figure 3-6.

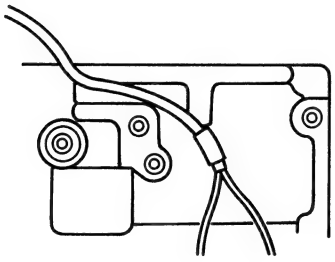


Figure 3-6. Sealed Wire Harness

Check
(1) Check the head track calibration. (→ **section 4.5.9**)
(2) Check the azimuth. (→ **section 4.5.10**)
(3) Perform a read/write check. (→ **section 4.5.11**)
(4) Perform a modulation check. (→ **section 4.5.12**)

3.2.5 Spindle Motor Assembly (5)

(1) Remove the PCB assembly.
(2) Turn the drive unit over, making sure the head does not hit the work surface.
(3) Remove screw (53) , then remove the leaf spring (7) and the WP lever (6).
(4) Remove the four screws labeled (56) , then remove the spindle motor assembly (5).

The assembly procedure is the reverse of disassembly.

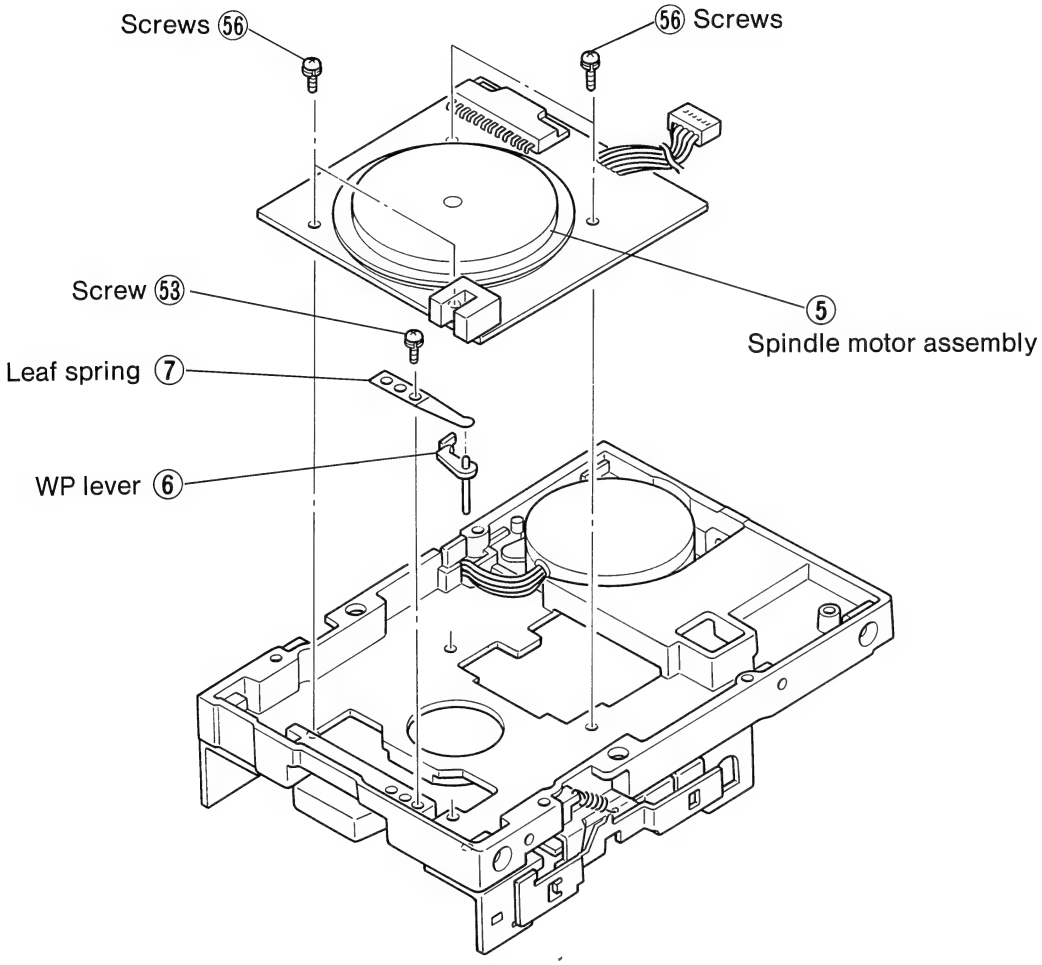


Figure 3-7. Spindle Motor Assembly

Check
(1) Insert a disk and check that the WP lever moves smoothly.
(2) Check the index period calibration. (→ **section 4.5.6**)
(3) Check the index timing calibration. (→ **section 4.5.7**)
(4) Check the head track calibration. (→ **section 4.5.9**)
(5) Check the azimuth. (→ **section 4.5.10**)
(6) Perform a read/write check. (→ **section 4.5.11**)
(7) Perform a modulation check. (→ **section 4.5.12**)
(8) Check the TR 00 calibration. (→ **section 4.5.5**)
(9) Check the stopper calibration. (→ **section 4.5.13**)

3.2.6 Stepping Motor (8)

(1) Remove screw (55), then remove the stopper plate (17).
(2) Remove two screws (53), then remove the fittings (16).
(3) Disengage the belt from the hook on the carriage assembly.
(4) Remove screw (55), then remove the fitting (9) and the stepping motor (8).
(5) Temporarily secure the new stepping motor (8) and the fitting (9) with screw (53).

The assembly procedure is the reverse of disassembly.
After performing the track calibration, tighten screws (53).

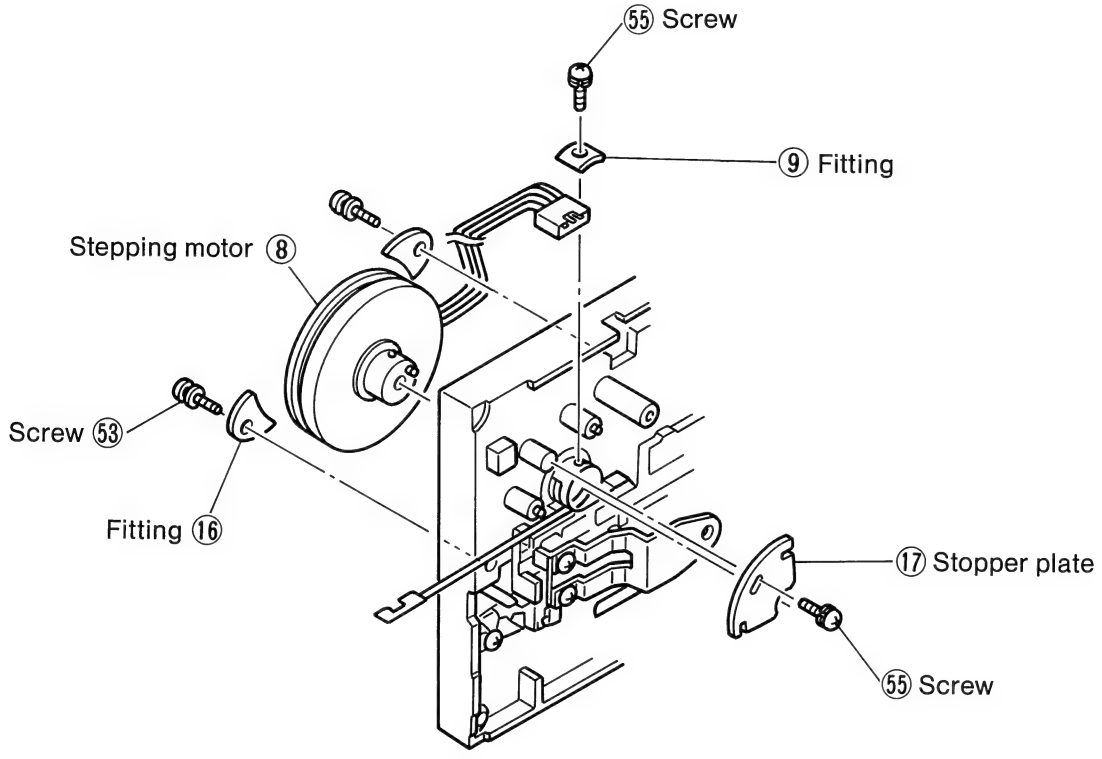


Figure 3-8. Stepping Motor Assembly

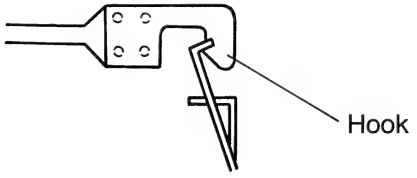


Figure 3-9. Steel Belt Assembly

Check
(1) Move the carriage assembly back and forth, checking that the action is smooth.
(2) Check the head track calibration. (→ **section 4.5.9**)
(3) Check the TR 00 calibration. (→ **section 4.5.5**)
(4) Check the stopper calibration. (→ **section 4.5.13**)

3.2.7 M Carriage Assembly (20)

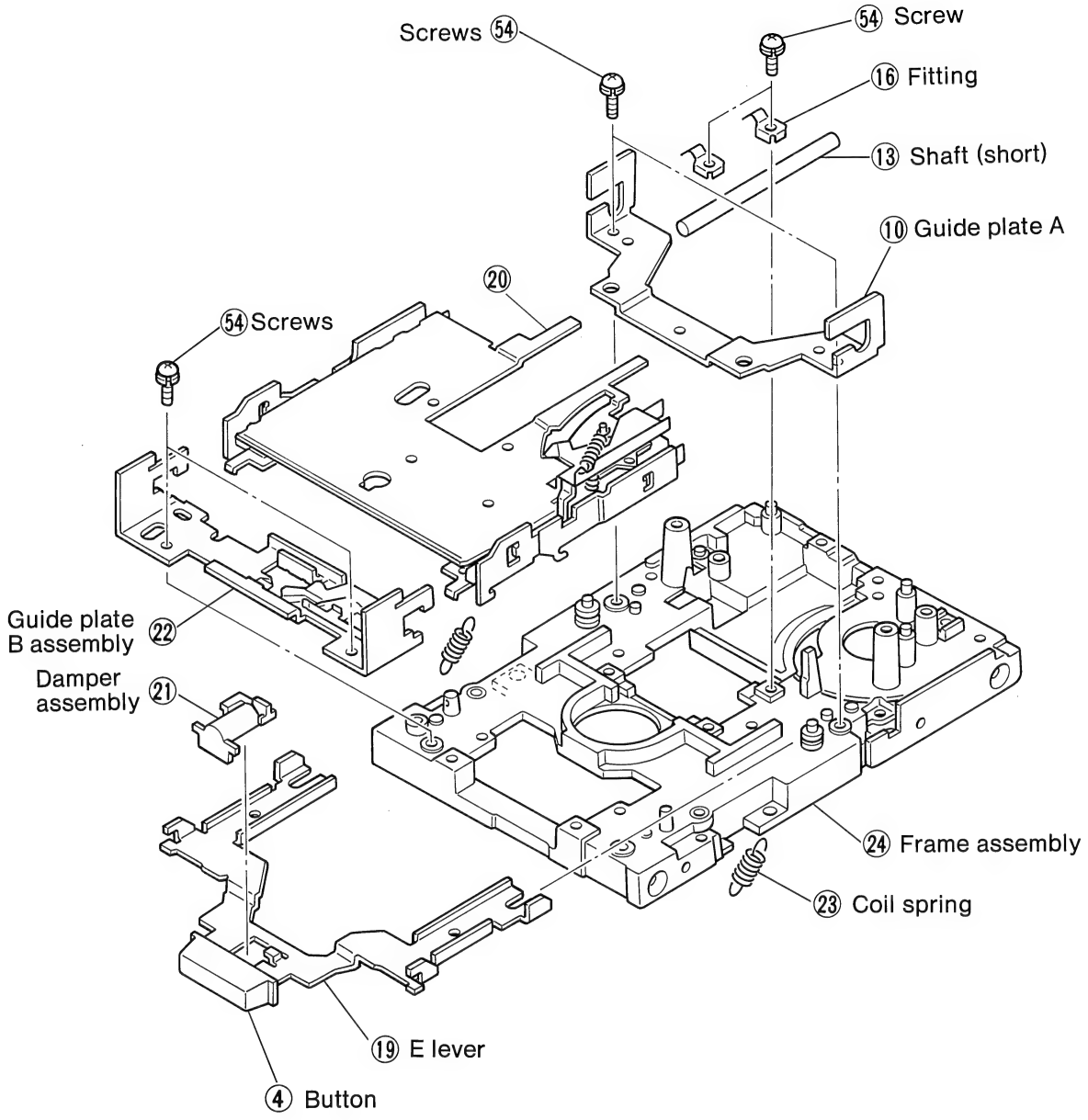


Figure 3-10. M Carriage Assembly

(1) Remove the left and right coil springs ㉓ .
(2) Insert a piece of soft paper between the head sections.

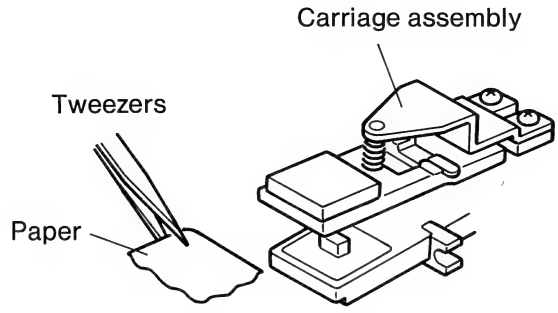


Figure 3-11. Head Carriage Assembly

(3) Remove the two screws labeled ㊹ , then remove the guide plate B assembly ㉒ together with the M carriage ⑳ .
(4) Remove the damper assembly ㉑ and E lever ⑲ .
(5) Before removing the guide plate A ⑩ from the frame, remove the M carriage assembly ⑳ (see Figure 3-4).
(6) When **reassembling**, insert the E lever into the axis guide on the frame.
(7) Set the E lever with the lever pushed in 5mm from the front panel.
(8) Set the damper assembly into the E lever after pulling out the damper assembly so that its extended length is 20mm.

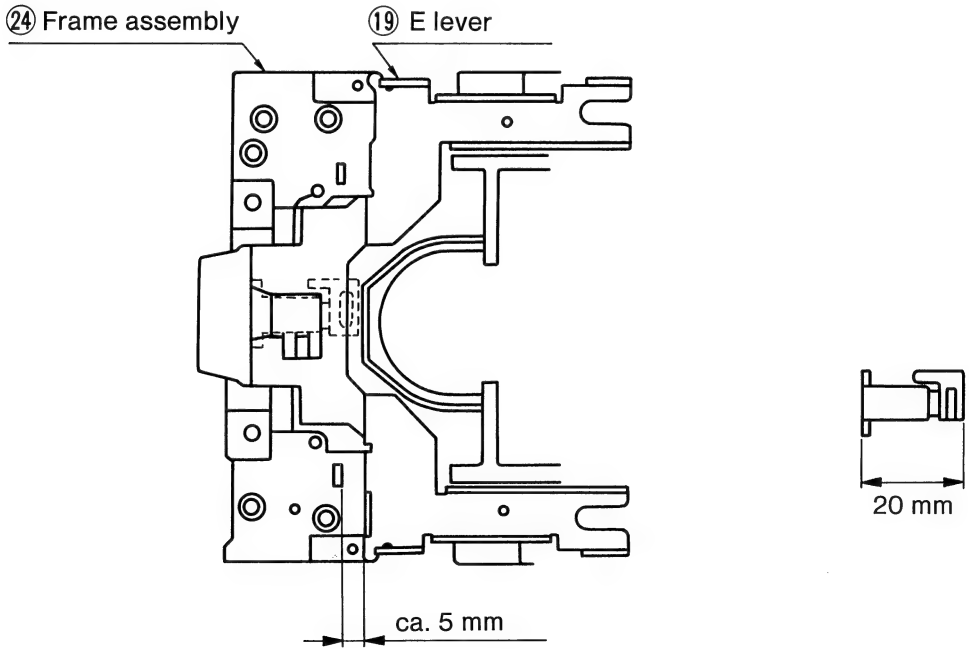


Figure 3-12. E lever Set

(9) Set the cam lever on the guide plate B assembly in the direction of the arrow.

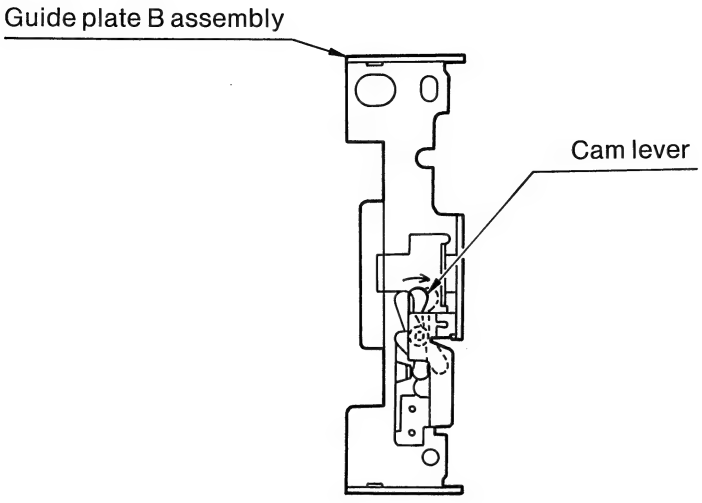


Figure 3-13. Lever Set

(10) With the guide plate B assembly installed on the M carriage assembly ⑳ , lower the M carriage assembly and install it onto the guide plate A.
(11) Secure with two screws ⑭ .
(12) Install the coil springs ㉓ .

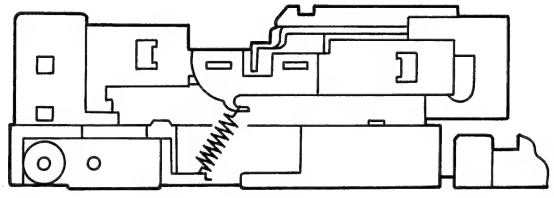


Figure 3-14. M Carriage Assembly

Check
(1) Load and eject a disk several times, checking the operation of the M carriage assembly.
(2) Perform a read/write check. (→ **section 4.5.11**)
(3) Perform a disk loading check. (→ **section 4.5.4**)

Section 4
MAINTENANCE AND ADJUSTMENTS

SECTION 4 — — MAINTENANCE AND ADJUSTMENTS

4.1 Cleaning

Remove dust and dirt by wiping the unit with a soft dry cloth. If the unit is very dirty, wipe with a cloth that has been dipped in a neutral detergent and well wrung out. Afterward use a dry cloth to blot up all moisture.

Do not use a flammable solvent such as benzene, thinner, isopropyl alcohol, etc., since such substances may damage painted surfaces. However, petroleum based benzene should be used to clean the LCD surface; a substance other than petroleum based benzene may discolor the LCD surface.

4.2 Modem Transmission Level Calibration

Two Tandy 600 computers, telephone lines and direct-connect Modem cables are necessary. The TELCOM application is available for calibration.

(1) Set the DIR/ACP switch to DIR for both Tandy 600 computers.
(2) Connect both Tandy 600 computers with telephone lines via direct connect Modem cables.

For the answering side:
(3) Select TELCOM, and press [ENTER].
(4) Select ANSWER sub-command, and press [ENTER] twice.

For the calling side:
(5) Select TELCOM, and press [ENTER].
(6) Select CONNECT sub-command, and press [ENTER].
(7) Press [TAB], type in the number to be dialed, and press [ENTER].

After dialing, both the Tandy 600 computers will then display "ONLINE."

For both sides:
(8) Press [SHIFT+ESC].

Both Tandy 600 computers will then display the command menu, while continuing to send a carrier tone. Now, the modem transmission level calibration is ready. Disconnect the direct telephone cable from both machines and:

(9) Disconnect the direct-connect Modem cable from both Tandy 600 computers.
(10) Connect a 600-ohm dummy load between pins 3 and 7 of the phone connector.
(11) Connect the level meter between pins 3 and 7 of the phone connector.
(12) Adjust VR3 so that the level meter reading is between −9 dBm and −11 dBm.

Test points

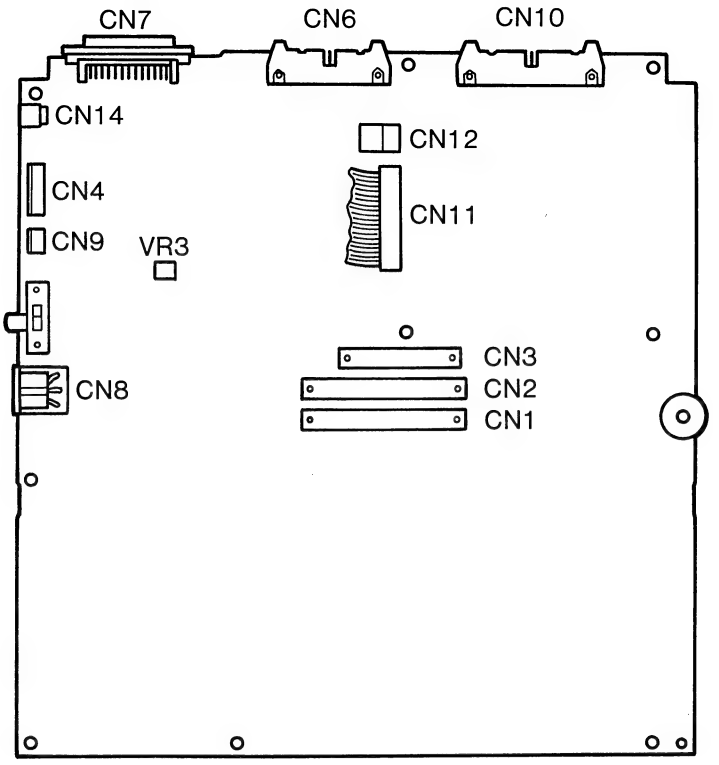


Figure 4-1. Test Point Position

4.3 FDD Controller Calibration

An oscilloscope and a frequency counter are used in this operation, which involves calibrating the VFO data separator that is built into WD2797.

(1) Remove the FDD unit.
(2) After confirming that T1 and T2 are short-circuited by 1 and 2, short-circuit T1 at 2 and 3.
(3) Turn the power on.
(4) Short-circuit 2 and 3 of T2 on the OPMP board with the power set to ON.
(5) Connect the frequency counter to CH7 (channel terminal). Rotate trimmer capacitor CV2 so that the frequency of CH7 is 237.5 ± 1 kHz.
(6) Connect the oscilloscope to CH6. Rotate control VR2 so that the pulse width is 500ns.
(7) Return T1 and T2 to the initial state—i.e., with 1 and 2 short-circuited.

Test points

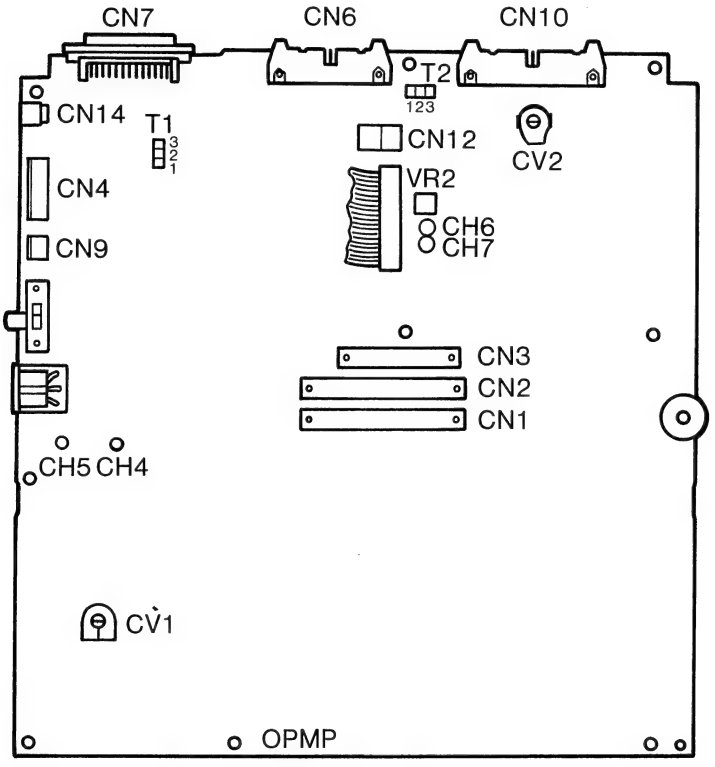


Figure 4-2. Test Point Position

4.4 Real Time Clock (RTC) Calibration

Connect the frequency counter to CH5 (channel terminal). Rotate trimmer capacitor CV1 so that the frequency of CH5 is 32,768.0 ± 0.2 Hz.

4.5 FDD Unit Calibration

4.5.1 Function check and calibration points

(1) Write protection
(2) Disk loading
(3) TR 00
(4) Index period
(5) Index timing
(6) Offset
(7) Head track
(8) Azimuth
(9) Read/Write
(10) Modulation
(11) Stopper

4.5.2 Test Points and Waveform

Test points

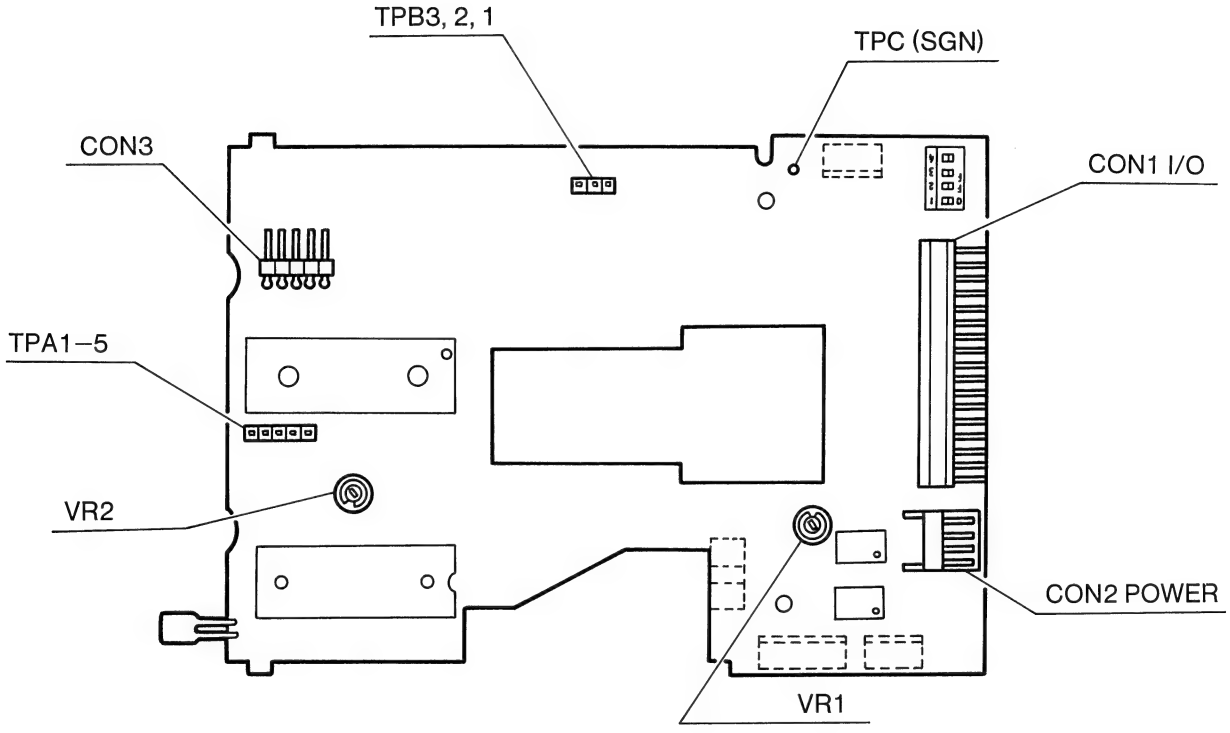


Figure 4-3. Test Point Position

(1) TPA-1 AMP
(2) TPA-2 AMP
(3) TPA-3 AMP
(4) TPA-4 AMP
(5) TPA-5 GND
(6) TPB-1 WP (WRITE PROTECT)
(7) TPB-2 M LOAD (DISK LOADING)
(8) TPB-3 TR 00
(9) Index timing VR2
(10) Offset VR1

Test pin output waveform

(1) TPA AMP waveform

TPA-1 AMP output waveform (measured using track 00):

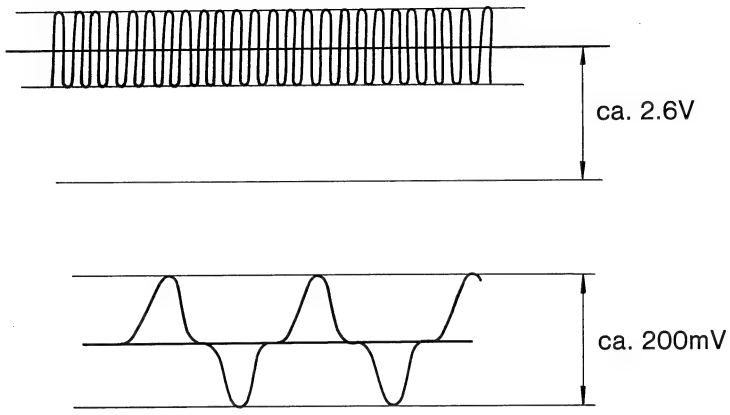


Figure 4-4. TPA-1 AMP Output Waveform

(2) TPB sensor output

TPB-1 WRITE PROTECT sensor	NON PROTECT → "HIGH"
TPB-2 DISK LOAD sensor	LOAD → "HIGH"
TPB-3 TRACK 00 sensor	TRACK 00 → "LOW"

Installation of motor extension cable for use in calibration

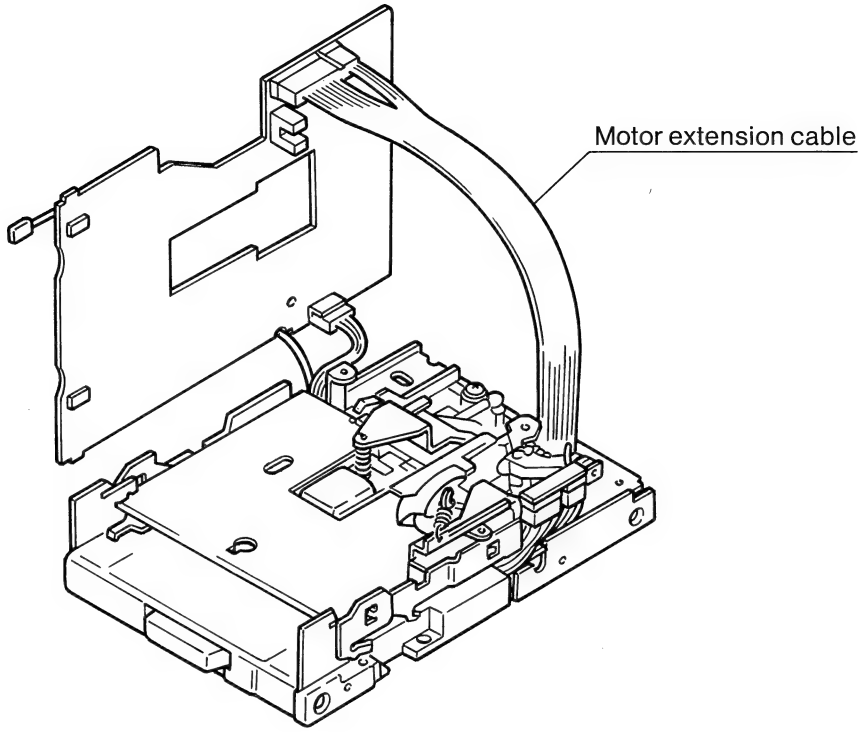


Figure 4-5. Adjusting Motor Extension Cable Installation Diagram

4.5.3 Write Protection

Service check

(1) Turn the power on.
(2) Insert a write-protected disk.
(3) Check that the write-protected lever does not move to the write enable position.
(4) Check TPB-1; OK if LOW is maintained.
(5) Insert a non-write-protected; the level should change from LOW to HIGH.
(6) If step 4 or 5 fails, replace the spindle motor assembly.
(7) OK if WRITE PROTECT signal from pin 26 on CN1 is LOW.
(8) If step 7 fails, repair or replace the PCB assembly.

4.5.4 Disk Loading

(1) Turn the power on.
(2) Insert a disk.
(3) OK if TPB-2 changes from HIGH to LOW.
(4) If step 3 fails, repair or replace the PCB assembly.

4.5.5 TR 00

Service check

(1) Turn the power on.
(2) Insert a disk.
(3) Seek to track 03, then to track 00.
(4) Check TPB-3. OK if the level changes from LOW to HIGH.
(5) If step 4 fails, replace or calibrate the TR 00 sensor assembly (see Calibration).
(6) OK if the signal level of pin 26 of CN1 changes from HIGH to LOW.
(7) If step 6 fails, repair or replace the PCB assembly.

Calibration

Note: A track 00 calibration following a seek error must be performed after the head track calibration.

(1) Loosen the one screw ㊺ securing the track 00 sensor assembly ⑱. Loosen the stopper screw ㊺ (see Figure 3-3).
(2) Attach the motor extension cable and turn the power on (see Figure 4-5).
(3) Check the sensor current draw: Install an ammeter between TPB-2 and GND, and check that the current flow is at least 100 microamperes and that the dark current is no more than 2 microamperes.
(4) Measure the AMP output (test pin TPA-1) with an oscilloscope (use the CE disk, see section 4.5.9, Track calibration).
(5) Set the DIRECTION SELECT to either HIGH or LOW. Enter the STEP signal until a signal for track 40 is output.
(6) After detecting a signal from track 40, set DIRECTION SELECT to HIGH. Enter the STEP signal 40 times to move the head carriage to track 00.
(7) Measure the test pin (TPB-3) on the PCB assembly with an oscilloscope.
(8) By means of the DIRECTION SELECT and STEP signal, calibrate the track 00 sensor assembly so that the test pin (TPB-3) output at the position (range A) indicated in the figure below is LOW.
(9) Tighten screw ㊺ after the calibration is completed.

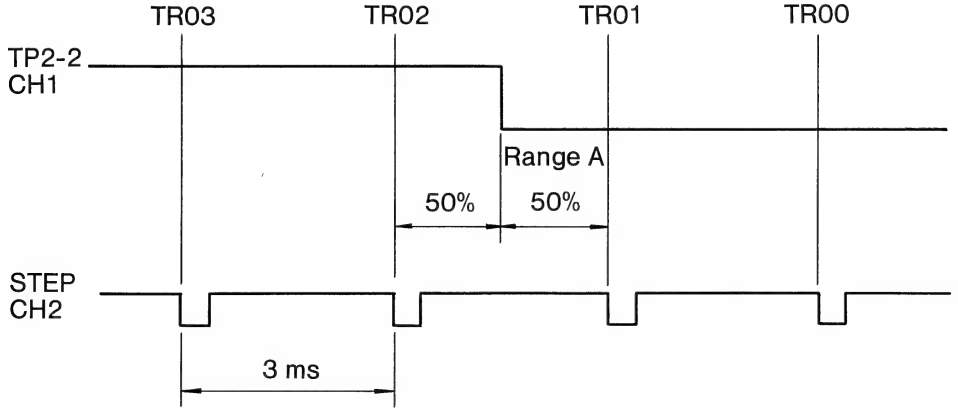


Figure 4-6. Track 00 Sensor Position Adjusting Waveform

INPUT COUPLING MODE	CH1 CH2	DC DC
VERT MODE		CH1
TIME/DIV.		5ms
VOLT/DIV.	CH1 CH2	2V 2V
TRIGGER MODE		CH2

4.5.6 Index Period

Service check

(1) Turn the power on.
(2) Set the MOTOR ON signal level to LOW.
(3) Insert a disk.
(4) Measure the INDEX SIGNAL (I/O CN 8P) with an oscilloscope. Using a counter, also measure the time interval. OK if the time interval is between 197 and 203 msec.

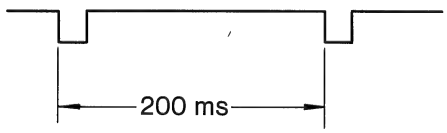


Figure 4-7. INDEX SIGNAL Adjusting Waveform

INPUT COUPLING MODE	DC
VERT MODE	CH1
TIME/DIV.	50ms
VOLT/DIV.	1V
TRIGGER/SOURCE	CH1
TRIGGER MODE	NORM

If the INDEX SIGNAL is not output, do the following:

(5) Insert a disk.
(6) Set the MOTOR ON signal to LOW, and turn the spindle motor.
(7) Check pin 3 of CN6 of the circuit board assembly in this condition.
(8) If the INDEX SIGNAL is being output, repair or replace the circuit board assembly.
(9) If the INDEX SIGNAL is not being output, replace the spindle motor assembly.

Spindle motor RPM

Perform the calibration by rotating the VR on the spindle motor board (see Figure 4-9). Measure the INDEX pulse inverter, and set to 200 ±1ms.

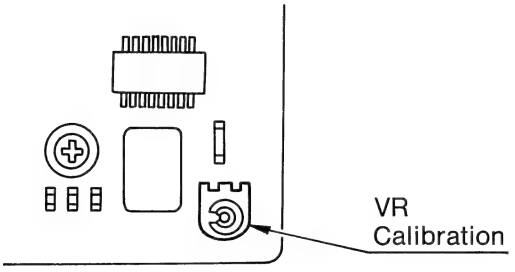


Figure 4-8. Position of Spindle Motor Adjusting VR



RPM decreased (time interval increased)



RPM increased (time interval decreased)

Figure 4-9. Spindle Motor Adjusting VR Turning Method

4.5.7 Index Timing

Service check

(1) Insert a CE disk.
(2) Set the MOTOR ON signal to LOW.
(3) Seek to track 40.
(4) Measure the outputs of INDEX (I/O CN 8P) and AMP (test pin TP1-4) with an oscilloscope.
(5) Calibrate the VR index.

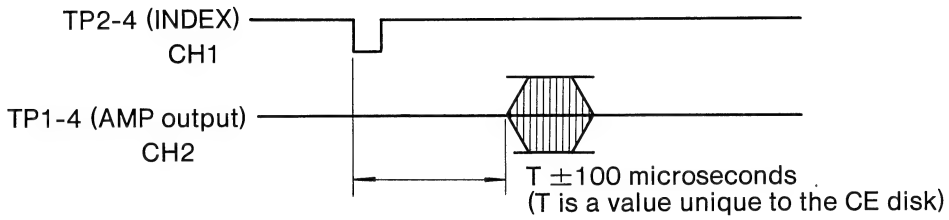


Figure 4-10. INDEX TIMING Adjusting Waveform

INPUT COUPLING MODE	CH1 CH2	DC AC
VERT MODE		CHOP
TIME/DIV.		5ms
VOLT/DIV.	CH1 CH2	2V 50mV
TRIGGER SOURCE		CH1
TRIGGER MODE		NORM

(6) Seek to track 00 and to track 79, and check that the timing for every 40 tracks is Tms +500ns, −300ns.

Calibration

Same as the Service check.
Calibrate the VR index of the PCB assembly so that (5) of the previous section is met.

4.5.8 Offset

Calibration

The offset is calibrated without the PCB assembly installation. Mount the PCB assembly on the offset calibration fixture (connect CN1, CN2 and CN3 to the fixture). Using an oscillator, input a 125 kHz sinusoidal waveform to the fixture (see the note below). Check the output of the fixture (RDD) using an oscilloscope (see Figure 4-11). Calibrate VR1 so that the value of A (signal variation) is zero.

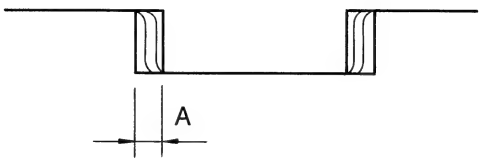


Figure 4-11. Offset Adjusting Waveform

Note: The 125 kHz sinusoidal waveform input by the oscillator must satisfy the following conditions:

Accuracy: 125 kHz ±2%;
Input level: Must be such that the output at the PCB assembly test pin (TPA-1) is 200mV (o-p) with the test pin connected to the calibration fixture.

4.5.9 Head Track

Track check

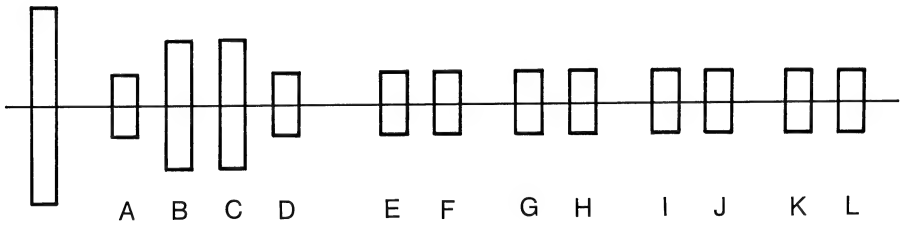
(1) Read the OFF track disk; OK if there is no error.
(2) Perform a read check using tracks 00, 01, 02, 03, 40, 76, 77, 78 and 79.

Track calibration

(1) Connect an oscilloscope.

CH1 INDEX I/O CN 8P CH2 AMP output TPA-1	INPUT COUPLING MODE	CH1 CH2	DC AC
	VERT MODE		CH2
	TIME/DIV.		5ms
	VOLT/DIV.	CH1 CH2	2V 50mV
	TRIGGER SOURCE		CH1
	TRIGGER MODE		NORM

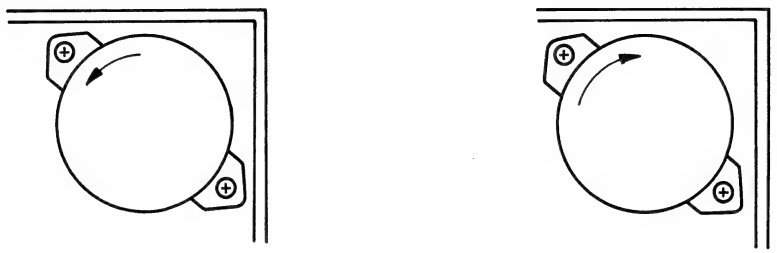
(2) Turn the power on.
(3) Insert a CE disk.
(4) Loosen the two screws ⑮ that secure the stepping motor.
(5) Seek from track 00 toward track 40.
(6) Check waveforms E through L, as shown in Figure 4-12.



$$\frac{E+G+I+K}{F+H+J+L} > 0.6 \quad \text{or} \quad \frac{F+H+J+L}{E+G+I+K} > 0.6$$

Figure 4-12. Track Adjusting Waveform

(7) Seek toward track 79, then return to track 40.
(8) OK if step 6 is satisfied.
(9) Waveform E is increased when rotation is counterclockwise ((a) in Figure 4-13).
Waveform F is increased when rotation is clockwise ((b) in Figure 4-13).



(a) (b)

Figure 4-13. Step Motor Adjusting Waveform

(10) Repeat steps 5 through 7.
(11) Tighten the two screws labeled ⑮ when the conditions shown in step 6 are satisfied.
(12) Repeat steps 5 through 7 and check.
(13) Insert and remove the CE disk.
(14) Repeat steps 5 through 8 and check.

4.5.10 Azimuth Check

Azimuth check

The measurement method is the same as shown in section 4.5.9.

(1) Seek from track 00 toward track 40.
(2) Check waveforms, A, B, C and D, as shown in Figure 4-14.
(3) OK if the azimuth is within ±30' (see Figure 4-15).

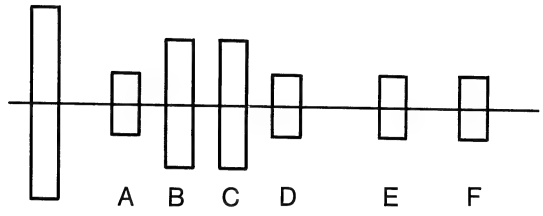


Figure 4-14. Azimuth Adjusting Waveform

Relationship between Azimuth and Pattern

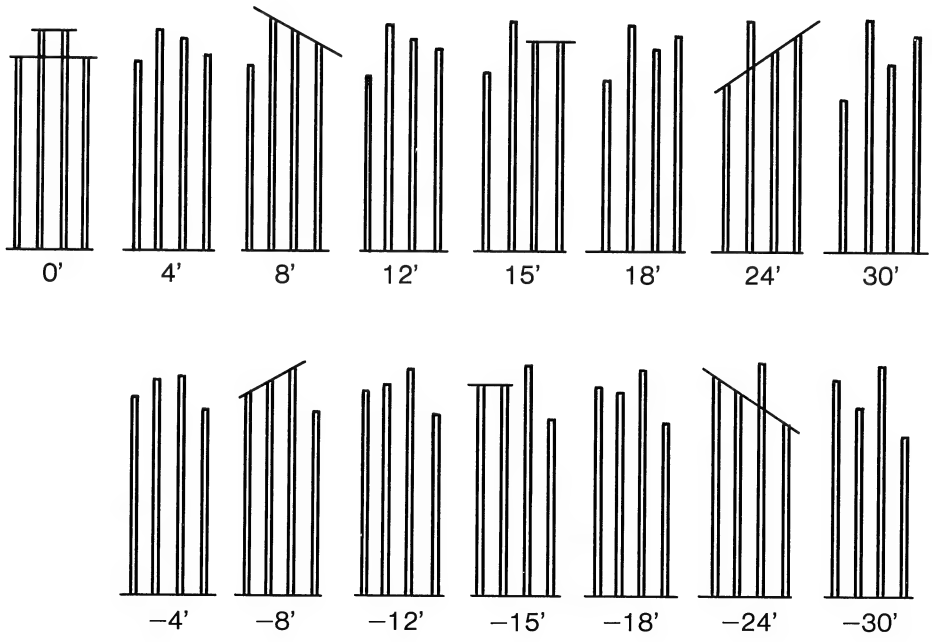


Figure 4-15. Relationship between Azimuth and Pattern

4.5.11 Read/Write

Read/Write check

(1) Remove the CE disk and load the inspection disk.
(2) Connect an oscilloscope.
(3) Turn the power on.
(4) Seek to track 79 and write data.
(5) Seek to track 00, then seek to track 79.
(6) Check the read waveform (see Figure 4-16).

CH1	INDEX I/O CN 8P	INPUT COUPLING MODE	CH1 CH2	DC AC
		VERT MODE		CH2
CH2	AMP output TPA-1	TIME/DIV.		5ms
		VOLT/DIV.	CH1 CH2	2V 50mV
		TRIGGER SOURCE		CH1
		TRIGGER MODE		NORM

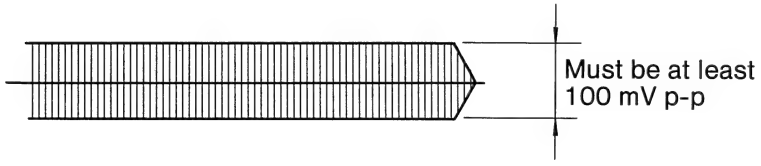


Figure 4-16. Read Waveform Diagram

(7) OK if AMP output is at least 100mv p-p.

4.5.12 Modulation

Modulation check

(1) Seek to track 79, then write and read using 2F and the inspection disk.
(2) Check the read waveform (see step 6 in section 4.5.11).
(3) Check that [(A-B)/(A+B)] × 100 ≦ ±8; see the Figure 4-17 for the definitions of A and B.

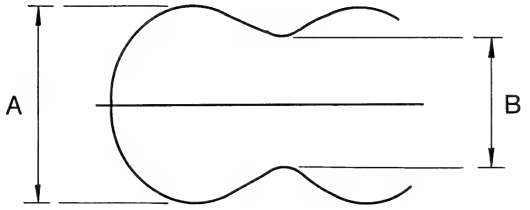


Figure 4-17. Modulation Check Waveform Diagram

4.5.13 Stopper

Stopper calibration

(1) The stopper must always be calibrated when the track 00 sensor assembly is adjusted.
(2) Seek the carriage assembly to track 00.
(3) Insert a stopper calibration gauge (t = 0.12) between the stopper plate and the stop pin, and tighten the screw ⑮ (tightening torque of at least 5kg-cm).

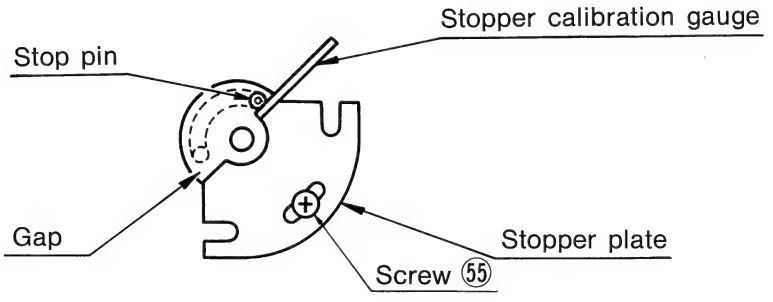


Figure 4-18. Stopper Adjustment

Check

(1) Seek from track 00 to track 79 and then back to track 00.
(2) Check that the stop pin does not hit the stopper.

Section 5
OPERATION

SECTION 5 – – OPERATION

5.1 Overview

5.1.1 Block Diagram

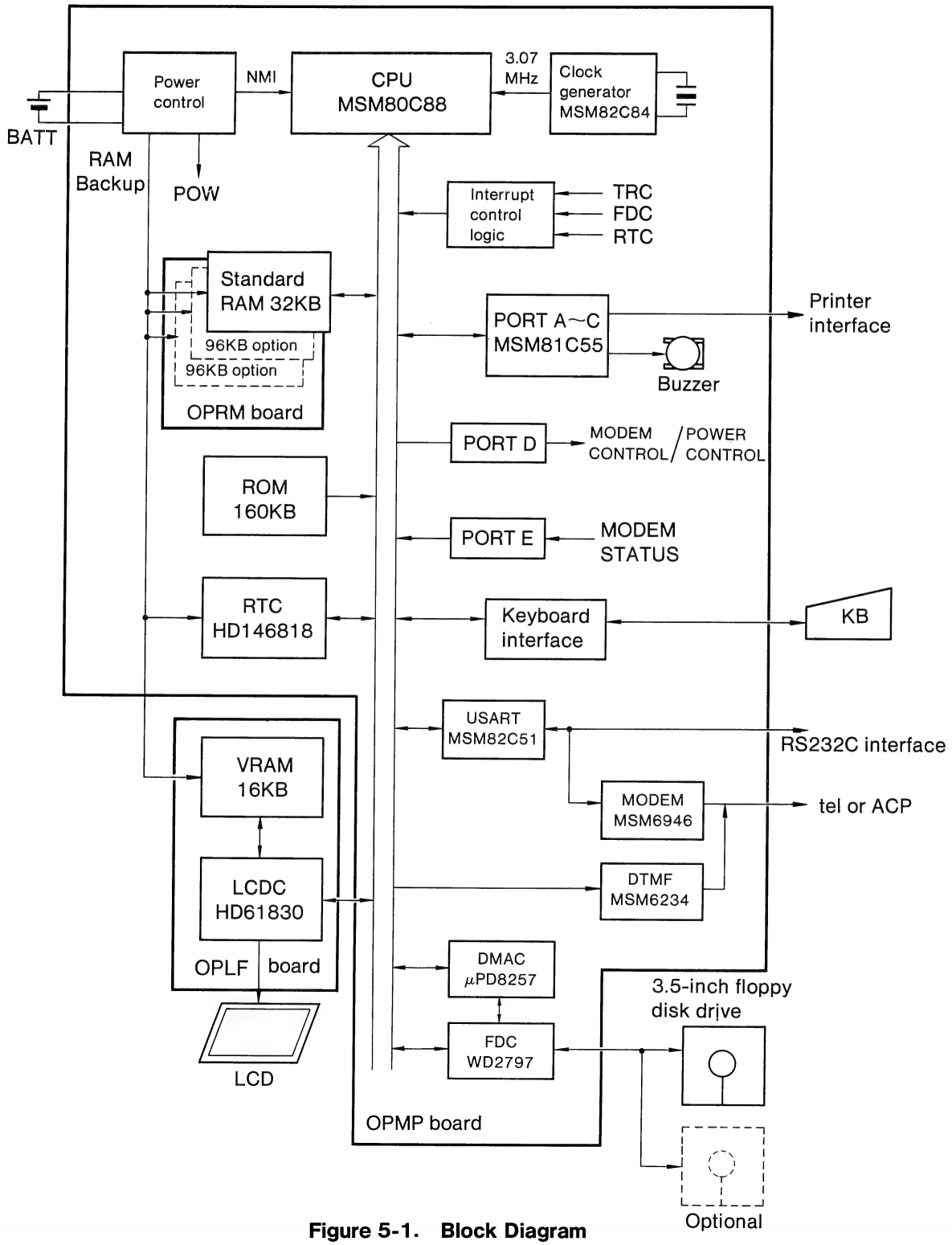


Figure 5-1. Block Diagram

5.1.2 Description of Blocks

The TANDY 600 is comprised of a main board (OPMP board), the LCD controller board (OPLF board), keyboard (OPKK board) a 3.5-inch floppy-disk drive and various options.

The following are brief descriptions of the functions of each of the components:

(1) Main Board (OPMP board)

– **CPU (MSM80C88)** The central processing unit that controls all functions.

– **Clock generator (MSM82C84)** Generates the clock timing for the CPU and all peripheral circuits; also controls the ready signal for all I/Os.

– **PIO (MSM81C55)** A parallel I/O port with an interval timer that controls the buzzer, keyboard, the timer, and the parallel interface for the printer.

– **USART (MSM82C51)** A general-purpose asynchronous serial interface.

– **MODEM (MSM6946)** Performs modulation and demodulation of serial data.

– **DTMF (MSM6234)** A dual tone, multi-frequency generator.

– **DMAC (μPD8257)** Controls DMA transfer between the storage and floppy-disk drive.

– **FDC (WD2797)** FDD controller with VFO and data separator.

(2) LCD Controller Board (OPLF board)

– **LCDC (HD61830)** Controls the display on the LCD unit and the video RAM.

(3) Keyboard (OPKK Board) Non-interrupt type XY matrix keyboard.

(4) 3.5-inch floppy-disk drive unit A single-sided, double-density floppy-disk drive with an unformatted capacity of 500KB.

(5) OPRM board An optional memory with a 96KB capacity.

5.2 CPU

5.2.1 CPU (MSM80C88)

The MSM80C88 is a 16-bit, 8-bit external data bus, low-power-consumption microprocessor sharing the same internal architecture as the 8086 microprocessor.

The MSM80C88 is equipped with a 20-bit address bus that can access a 1-megabyte memory area, an 8-bit I/O and storage data bus. The microprocessor can be used either in the minimum mode, which is suitable for a small system, or in the maximum mode, suitable for a large system. The microprocessor is configured in the TANDY 600 in the minimum mode.

5.2.2 Clock Generator (MSM82C84)

The peripheral circuits of the clock generator are shown in Figure 5-2. A 9.216 MHz quartz oscillator is connected to the X1 and X2 terminals of the 82C84.

The 82C84 divides the standard frequency (9.216 MHz) by three and feeds the resulting 3.07 MHz signal to the CPU to be used as CLK. The 82C84 also divides the same standard frequency by six and feeds the resulting 1.53 MHz signal to the peripheral circuits to be used as the PCLK.

CLK = 3.07 MHz
PCLK = 1.53 MHz

When the power is turned on, the CPU and the peripheral circuits are reset by the 82C84 using the $\overline{\text{RESET SO}}$ signal. When an I/O command to the KB, PRINTER or LCD is executed by the CPU, an INWAIT signal is output. The signal is first synchronized by the 82C84 and is then fed to the CPU's READY terminal.

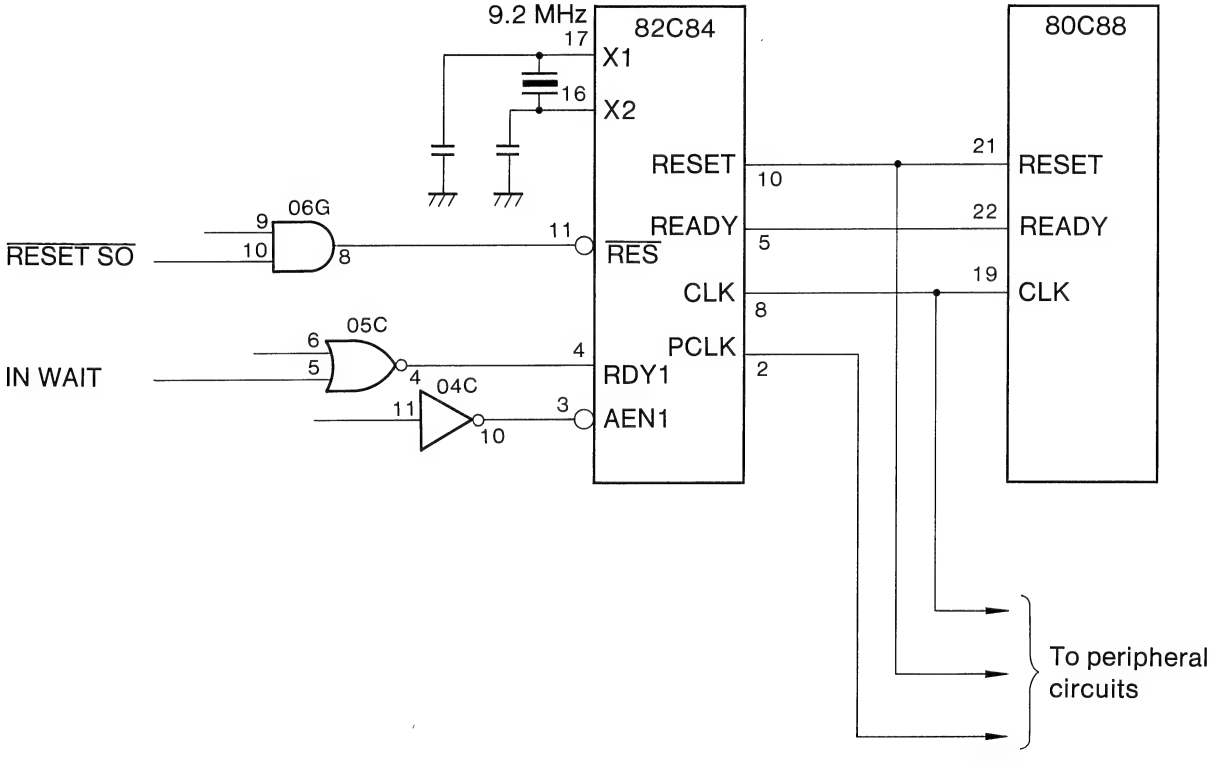


Figure 5-2. 82C84 and Peripheral Circuits

5.2.3 READY Control

The READY signal from the MSM80C88 is used for two purposes: (1) synchronizing the I/O (HD61830 LCD), unlike the CPU; and (2) delaying the KB STROBE and PR STROBE signals.

Figures 5-3a and 5-3b show the READY control circuit diagram and timing chart.

A logical OR from the $\overline{\text{LCDC1SEL}}$, $\overline{\text{LCDC2SEL}}$, $\overline{\text{KB STROBE}}$ and $\overline{\text{PR STROBE}}$ is fed to 05E D F/F. The CPU negative-phase clock is fed to the D F/F terminals of 05E. A logical OR from the $\overline{\text{IRD}}$ and $\overline{\text{IWR}}$ is fed to the preset terminal.

Therefore, when $\overline{\text{IRD}}$ or $\overline{\text{IWR}}$ is LOW, each D F/F is preset and its operation is started. An IN WAIT signal for one or two clocks is generated by taking a NOR between $\overline{\text{LCDC1SEL}}$, $\overline{\text{LCDC2SEL}}$, $\overline{\text{KB STROBE}}$, $\overline{\text{PR STROBE}}$ and 05C, and an OR of 05D.

1 WAIT	An LCDC-related I/O command is executed. An I/O command for KB STROBE is executed.
2 WAIT	An I/O command for PR STROBE is executed.

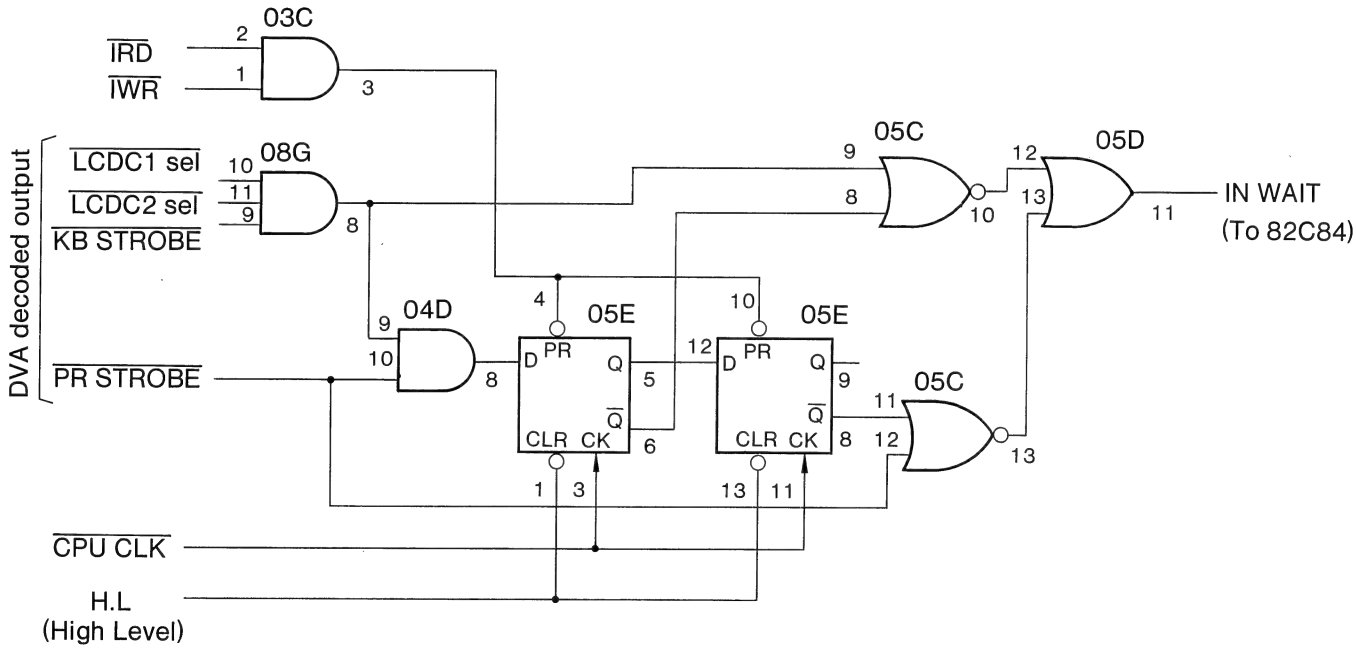


Figure 5-3a. READY Control Circuit

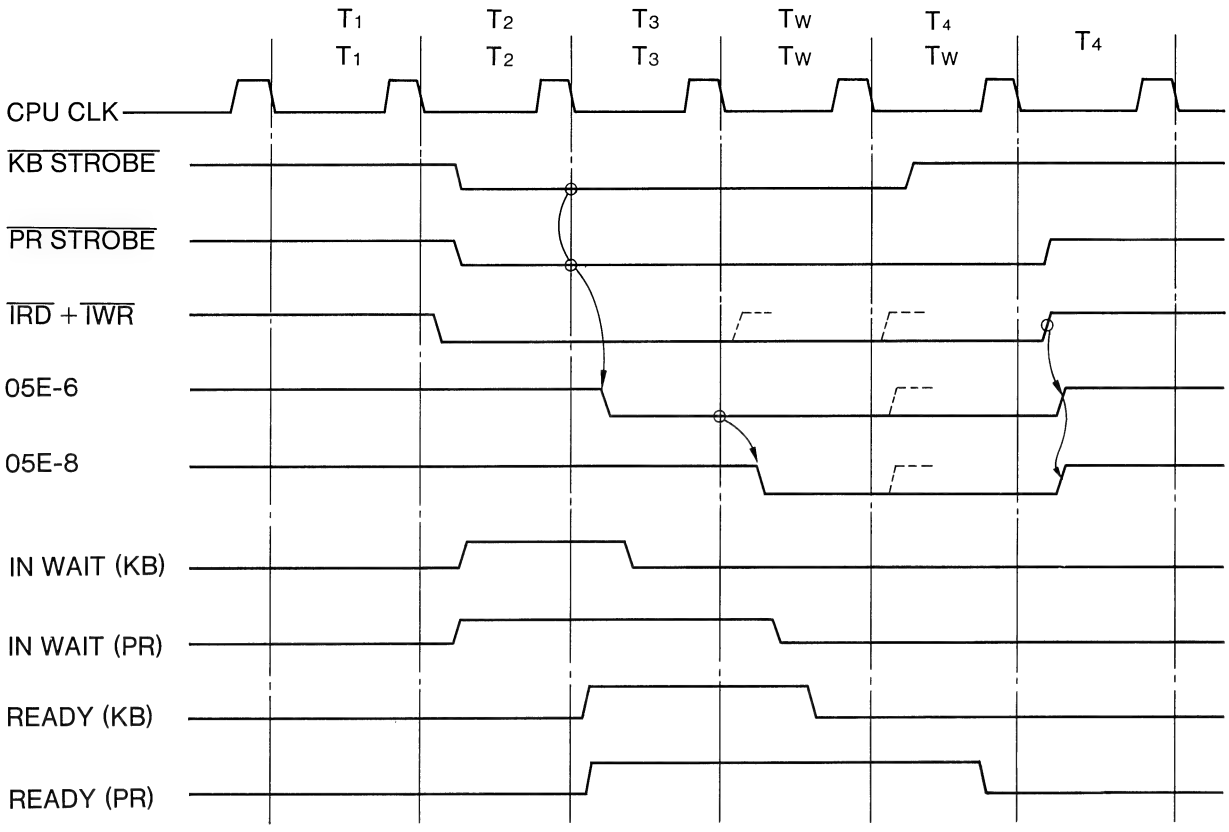


Figure 5-3b. READY Control Timing Chart

5.3 Storage

The largest storage capacity that can be installed on this device is 224KB of RAM and 160KB of ROM.

Type	Capacity	IC name	Capacity /chip	Number used
Standard RAM (installed on OPMP board)	32KB	HM6264LP-15	8KB	4
Optional RAM (×2) (installed on OPRM board)	96KB	HM6264LFP-15	8KB	12
ROM (installed on OPMP board)	160KB	HN613256	32KB	5

Table 5-1. Memory and Capacity

5.3.1 Memory Map

The memory map (Figure 5-4) shows the location on the board of the IC and the corresponding memory chip-select signal.

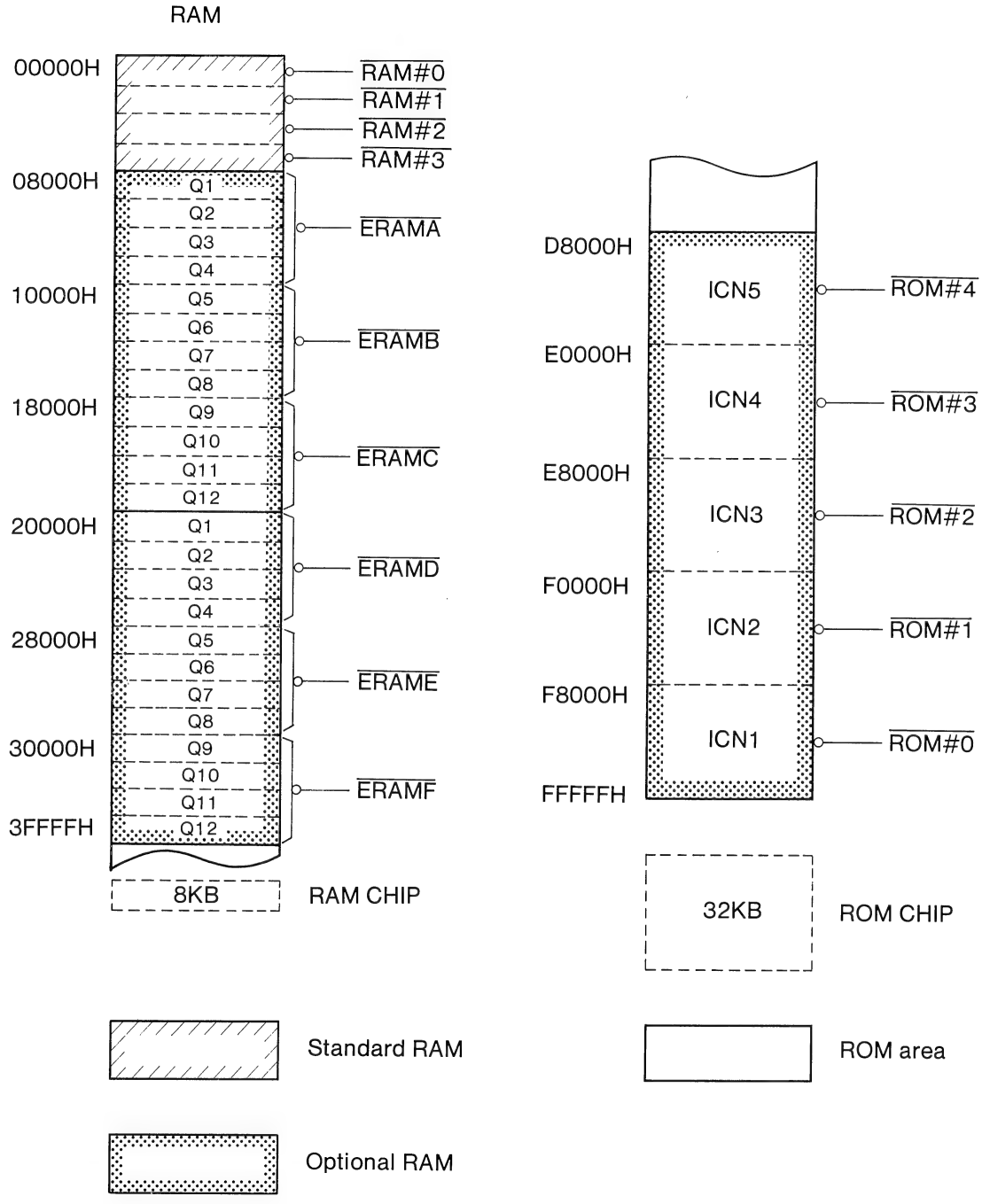


Figure 5-4. Memory Map

5.3.2 Memory Address Decoding

With the standard RAM, the memory address is decoded in 8KB units. With the optional RAM and ROM chips, decoding is done in 32KB units. Refer to the memory address decoding circuit diagram shown in Figure 5-5. When a RAM address (00000H – 3FFFFH) is output to SA19-0, both SA19 and SA18 are 0, and 09F pin 3 becomes "LOW". Since the SIO/M signal is "LOW" in memory access, 09H operates. Consequently, either 08E pin 4-7 or 09H15 pin 11 become "LOW". While, this signal is used as the chip select signal of each RAM. The 06G pin 6 becomes HIGH since A19 and A18 are both 1. This makes 07E valid. The SIO/M signal at this time is LOW.

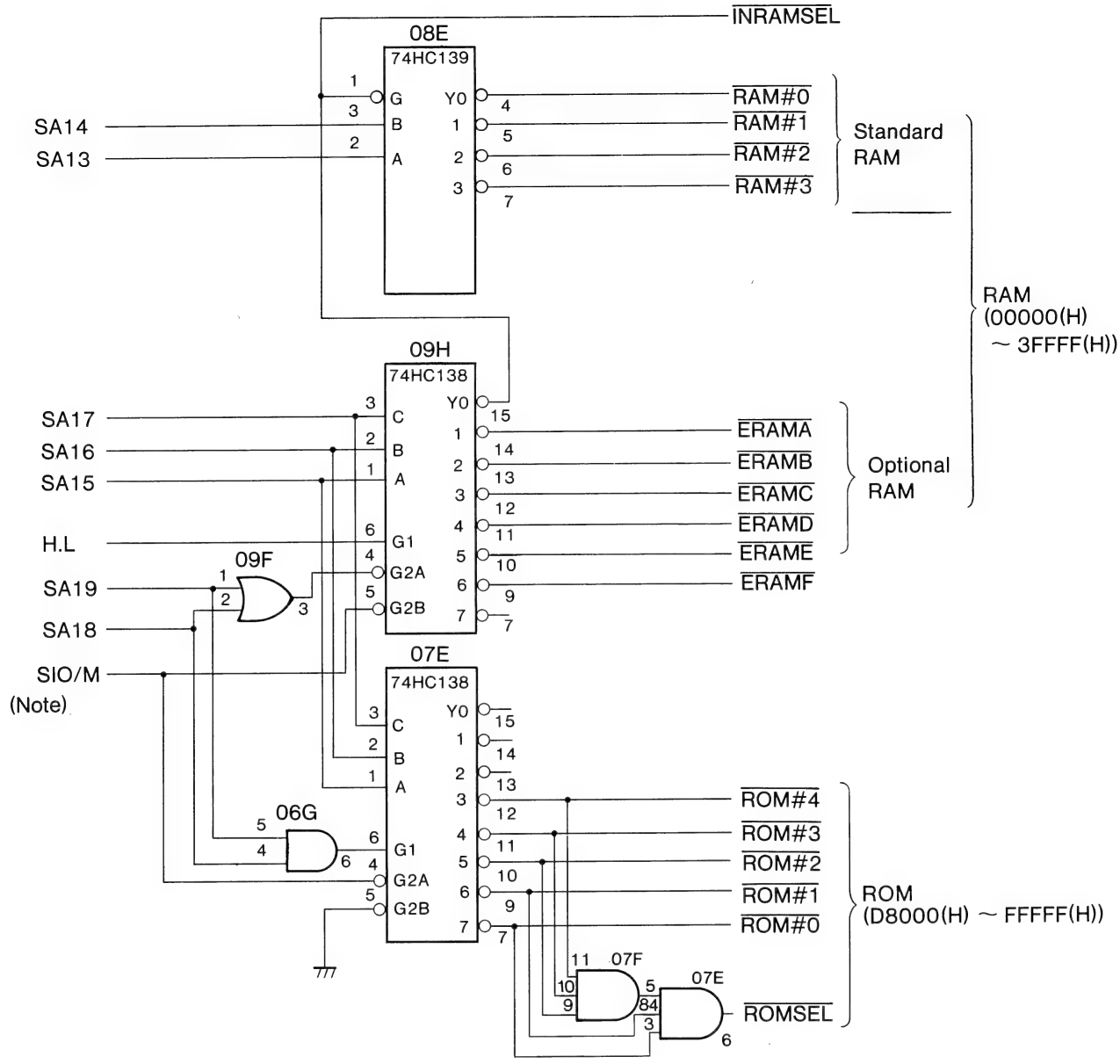
Therefore, one of the decoder outputs (07E pin 12-9, 7) and the $\overline{\text{ROMSEL}}$ signal will be LOW. The $\overline{\text{ROM \#0-\#4}}$ signals are used for ROM chip selection, and $\overline{\text{ROMSEL}}$ is used as a gate signal for the buffer between the ROM data output and SD7-0.

Note: See Figure 5-4 for the relationship between the address and the ROM and RAM chip selection signal.

Input Signal							Output														
							08E				09H						07E				
S19	S18	S17	S16	S15	S14	S13	4	5	6	7	14	13	12	11	10	9	12	11	10	9	7
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1			1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0			1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1			1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0			1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	0	1			1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	1	1	0			1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	0	1	1	1			1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1						1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0						1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	0			1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1			1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0			1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1			1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	0	0			1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1			1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	1	1	1	0			1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1			1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Note: 1 : High
0 : Low
Blank : Both 1 and 0 are allowed.
Input signals of 09H-5 pin and 07E-4p pin are 0.

Table 5-2. Function Table



Note: The SIO/M signal is HIGH during CPU I/O access, and is LOW during memory access.

Figure 5-5. Memory Address Decoder Circuit

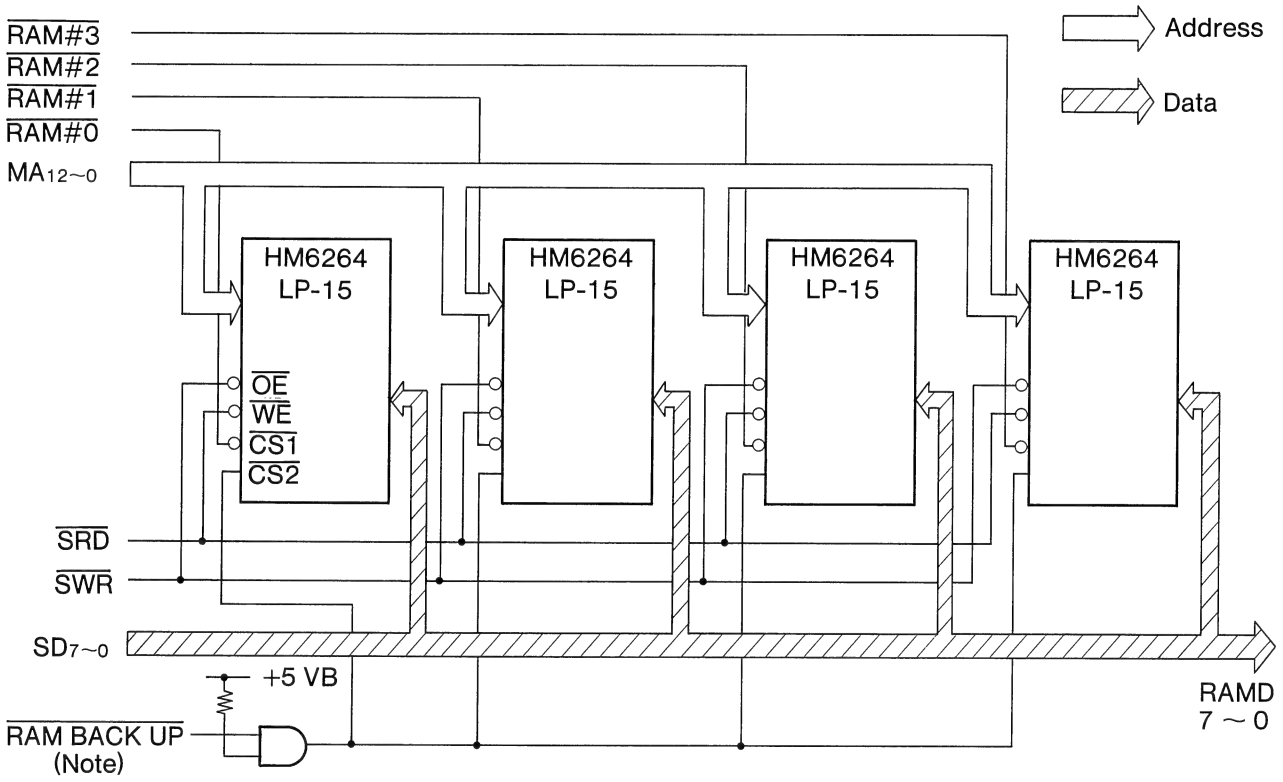
5.3.3 RAM

(1) Standard RAM

A block diagram for the standard memory is shown in Figure 5-6. Four HM6264LP-15 are used in the standard memory. The total storage capacity is 8KB×4.

One of the four RAMs is selected by the $\overline{\text{RAM \#0-\#4}}$ signal. The address of the RAM that is selected is specified by MA12-0. During a read operation, the $\overline{\text{SRD}}$ signal will have a low level. The data is read from RAMD7-0.

During a write operation, the $\overline{\text{SWR}}$ signal will have a low level, and the data is written onto the RAM from SD7-0.



Note: When power is off, the RAM BACKUP signal is set to LOW in order to retain the contents of the RAM.

Figure 5-6. Standard Memory Block Diagram

(2) Optional RAM (installed on OPRM board)

The block diagram for the optional RAM is shown in Figure 5-7. Up to two optional RAM cards can be installed on this device. Each card has a storage capacity of 96KB (HM6264LFP-15 8KB RAM chip ×12). As Figure 5-7 shows, 96KB of storage are arranged in three blocks of 32KB each stacked vertically. The three blocks are differentiated by the $\overline{32K\text{-}1}$, $\overline{32K\text{-}2}$, and $\overline{32K\text{-}3}$ signals.

Q13, Q16 (TC40H139F) decodes SA14 and SA13 and outputs a chip selection signal for each of the RAM chips. Just as with the standard RAM, the contents of the optional RAM are retained by setting the $\overline{\text{RAM BACKUP}}$ signal to LOW.

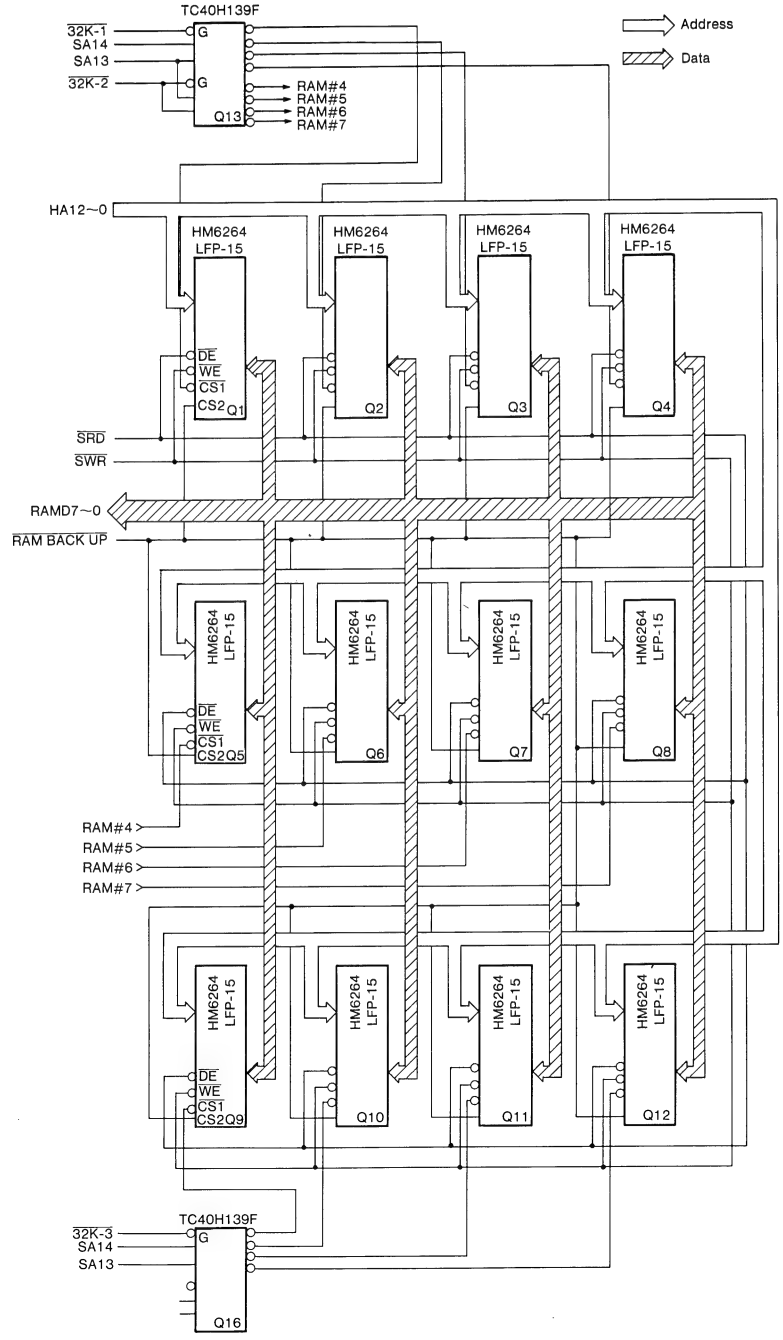


Figure 5-7. Optional RAM Block Diagram

5.3.4 ROM

A block diagram for the ROM is shown in Figure 5-8. The TANDY 600 has five ROMs (HN613256P 32KB mask ROMs) that are installed onto IC sockets. Any one of the five ROMs is selected by the $\overline{\text{ROM}}$ #0-#4 signal.

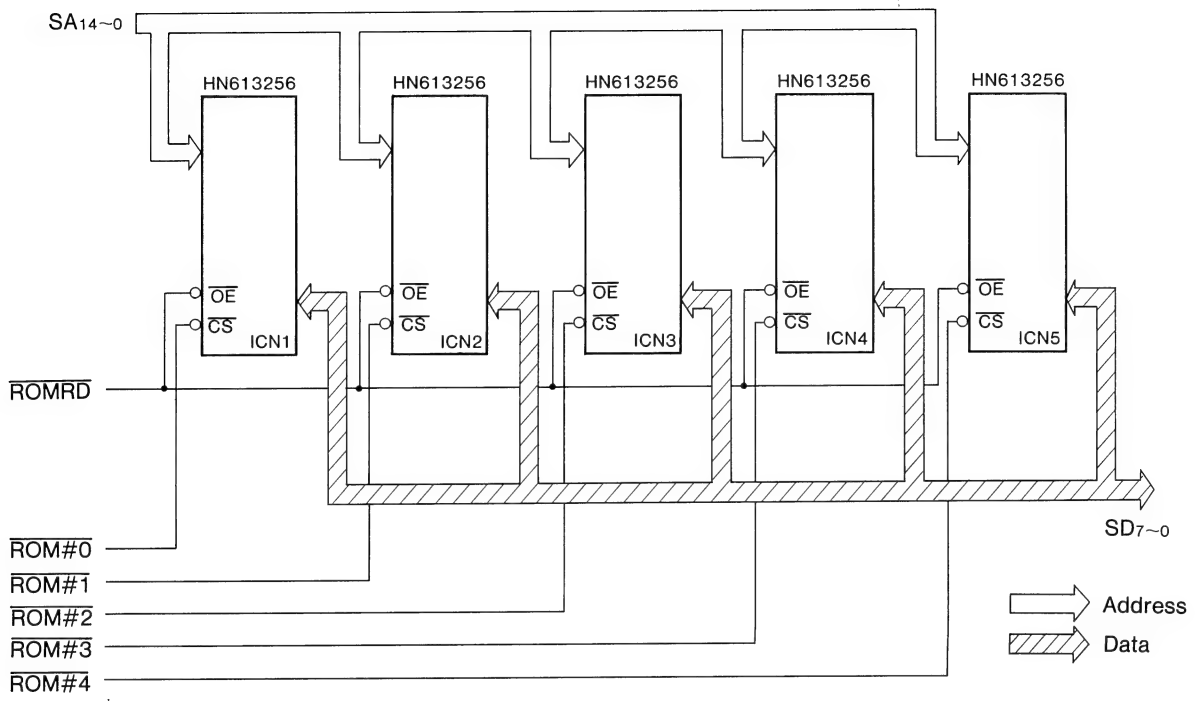


Figure 5-8. ROM Block Diagram

5.4 I/O

I/O commands from the MSM80C88 are used to control the I/O operation. The format of the I/O commands is as follows:

(1) Device address (DVA) = 16 bits
(2) Data = 8 bits
(3) OUT DX, AL/IN DX, AL

5.4.1 I/O Address Decoder and I/O Map

The TANDY 600's I/O includes FDC, DMAC, PORT A-E, LCDC, USART and RTC. Not all I/O addresses (16 bits) are decoded.

Refer to the I/O address decoder circuit diagram shown in Figure 5-9. LA15 and LA14 are decoded by 09G (74HC139) to output the basic select signals and the chip-select signals for various LSIs. Also, 08E (74HC139) and 08F (74HC138) are used for decoding various I/O control signals and select signals for external registers.

Refer to the I/O map shown in Table 5-2 for the relationship between the address and various I/O select signals and how the select signals are decoded.

Select signal	Block	I/O	Device address			
			A_{15} A_{12}	A_{11} A_8	A_7 A_4	A_3 A_0
$\overline{\text{FDB SEL}}$	FDC	I/O	0 0 X X	X	X 0 0 0	X X △ △
	DMC	I/O			X 0 0 1	△ △ △ △
	DMC peripheral	O			X 1 0 1 X 1 1 0	X
$\overline{\text{81C55 SEL}}$	PORT A-C	I/O	0 1 X X	X	X	X △ △ △
$\overline{\text{LCDC1 SEL}}$	LCDC1 (master)	I/O	8	X X X X	X X X △	X
$\overline{\text{LCDC2 SEL}}$	LCDC2 (slave)	I/O	9	X X X X	X X △ X	X
$\overline{\text{82C51 SEL}}$	USART	I/O	A	X X X X	X △ X X	X
$\overline{\text{PORT RD}}$	Various I/O or external registers	I	B	0 0 X X	X	X
$\overline{\text{DTMF SET}}$		O		0 0 0 X	X	X
$\overline{\text{TRC IPT CLEAR}}$		O		0 0 1 X	X	X
$\overline{\text{IPT MSK WR}}$		O		0 1 0 X	X	X
$\overline{\text{PORT WR}}$		O		0 1 1 X	X	X
$\overline{\text{PR STROBE}}$		O		1 0 0 X	X	X
$\overline{\text{KB STROBE}}$		O		1 0 1 X	X	X
$\overline{\text{TIM2 IPT CLR}}$		I		1 1 X X	X	X
$\overline{\text{RTC SEL}}$	RTC	I/O	1 1 X X	X	△	(00–3F)

Table 5-3. I/O Map

Note: X indicates that address decoding is performed; △ indicates that the particular device address is connected to an LSI address terminal.

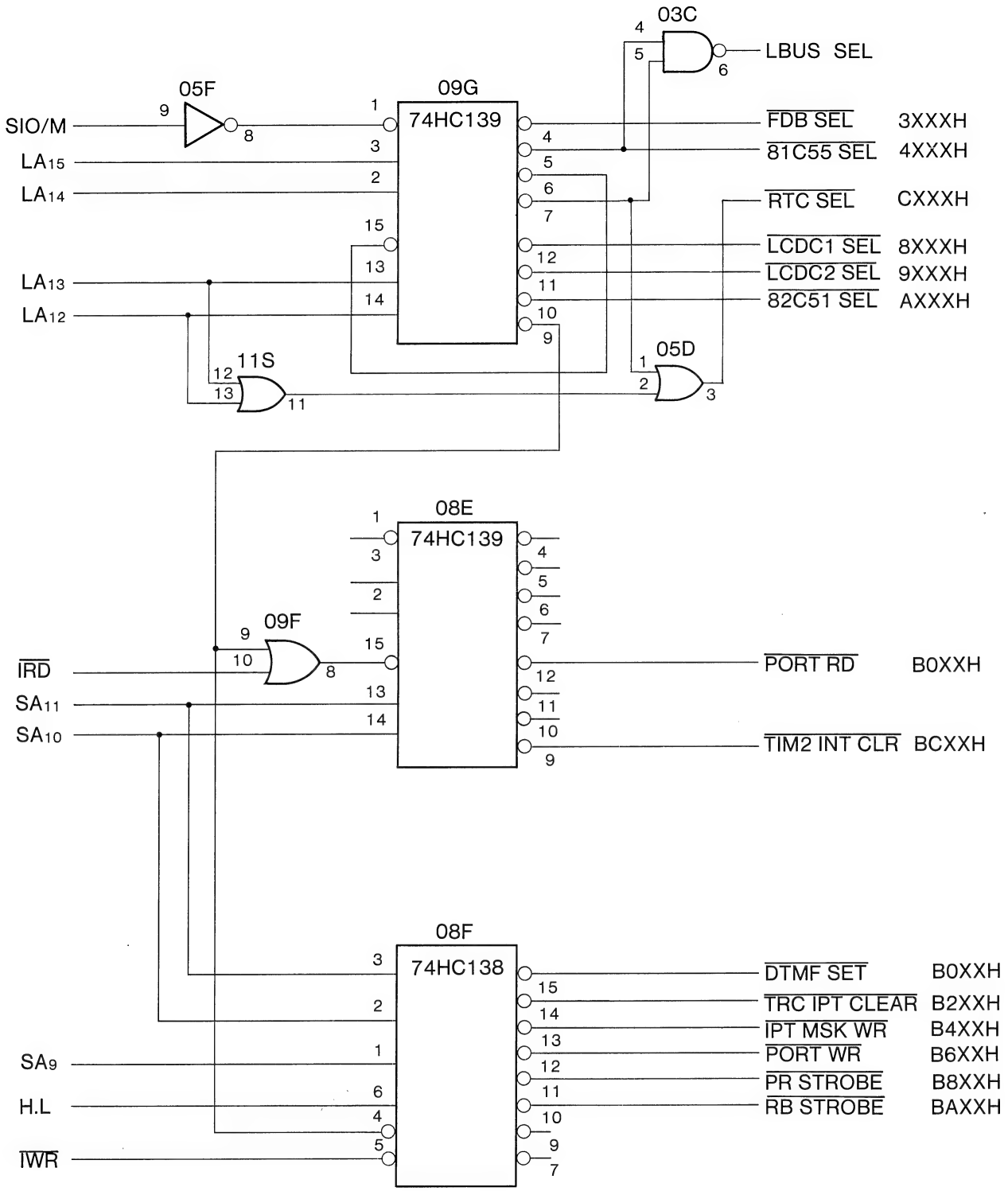


Figure 5-9. I/O Address Decoder Circuit

5.4.2 I/O Port

The TANDY 600 is equipped with five I/O ports for I/O control.

(1) Port A
Corresponds to PA7-0 for the MSM81C55. This port is an output port for data output to printers and for output of keyboard addresses (see Figure 5-10).

(2) Port B
Corresponds to PB7-0 for the MSM81C55. The KB CLR signal and the buzzer control signal are output from this port (see Figure 5-10).

(3) Port C
Corresponds to PC5-0 for the MSM81C55. This port is used as an input port for the KB STATUS signal or PR BUSY signal (see Figure 5-10).

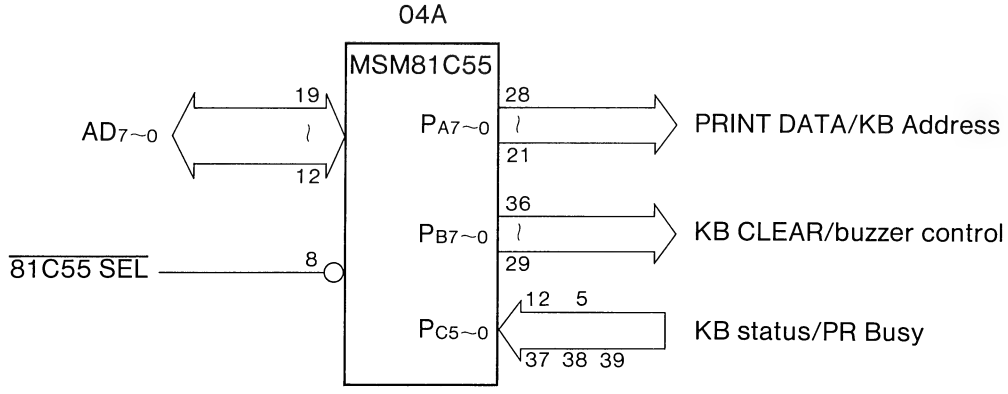


Figure 5-10. Ports A – C

(4) Port D
This port, which is assigned to external registers, is an output port for controlling the modem and power (see Figure 5-11).

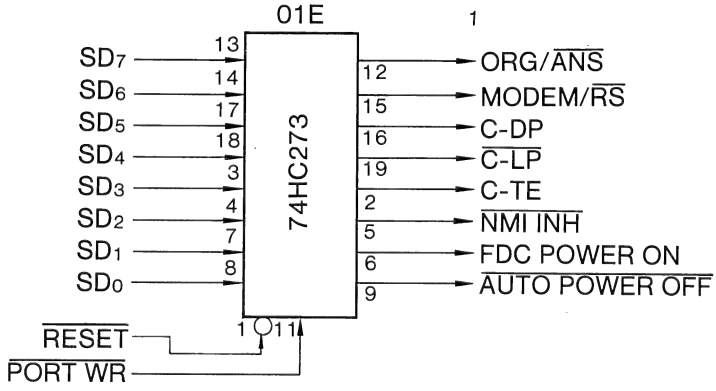


Figure 5-11. Port D

(5) Port E

This port, which is assigned to external registers, is used as an input port for sensing interrupts from lines (see Figure 5-12).

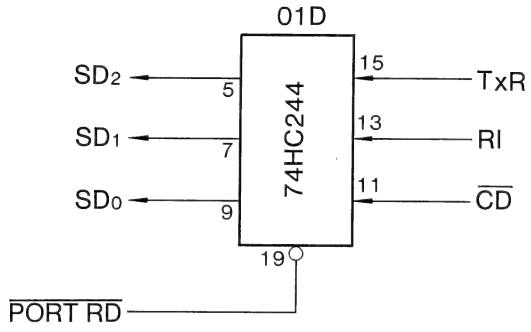


Figure 5-12. Port E

5.5 Interrupts

There are five interrupt request (INTR) levels with this device, one of which is not maskable NMI (non-maskable interrupt) and four are maskable.

Level	Interrupt type	Maskable	Interrupt vector
NMI	POWER LOW	NO	02
Level 1	RTC	YES	8F, 9F, AF, BF
Level 2	TRC	YES	CF, DF
Level 3	FDC	YES	EF
Level 4	81C55 timer	YES	FF

Table 5-4. Interrupt Level and Type

Interrupt device	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Interrupt vector
81C55 Timer 3	1	1	1	1	1	1	1	1	FF
FDC	1	1	1	0	1	1	1	1	EF
TRC	1	1	0	x	1	1	1	1	CF, DF
RTC	1	0	x	x	1	1	1	1	8F, 9F, AF, BF

Table 5-5. Interrupt Vector

5.5.1 Interrupt Levels

An NMI has the highest interrupt priority; level 4 has the lowest interrupt priority.

5.5.2 Interrupt Control

Refer to the interrupt control circuit diagram shown in Figure 5-13. A logical OR is taken between the $\overline{\text{RTC IPT}}$, $\overline{\text{TRC IPT}}$, $\overline{\text{FDC IPT}}$ and the $\overline{\text{TIM2 IPT}}$ interrupt signals and 07F to produce the IPT (interrupt request) signal. Also, the masking of each interrupt signal is controlled by the INT MASK REG and the 03D gate.

When the INTA (interrupt acknowledge) signal from MSM80C88 becomes LOW, the interrupt vector is output from 01D (74HC244) to SD6-4.

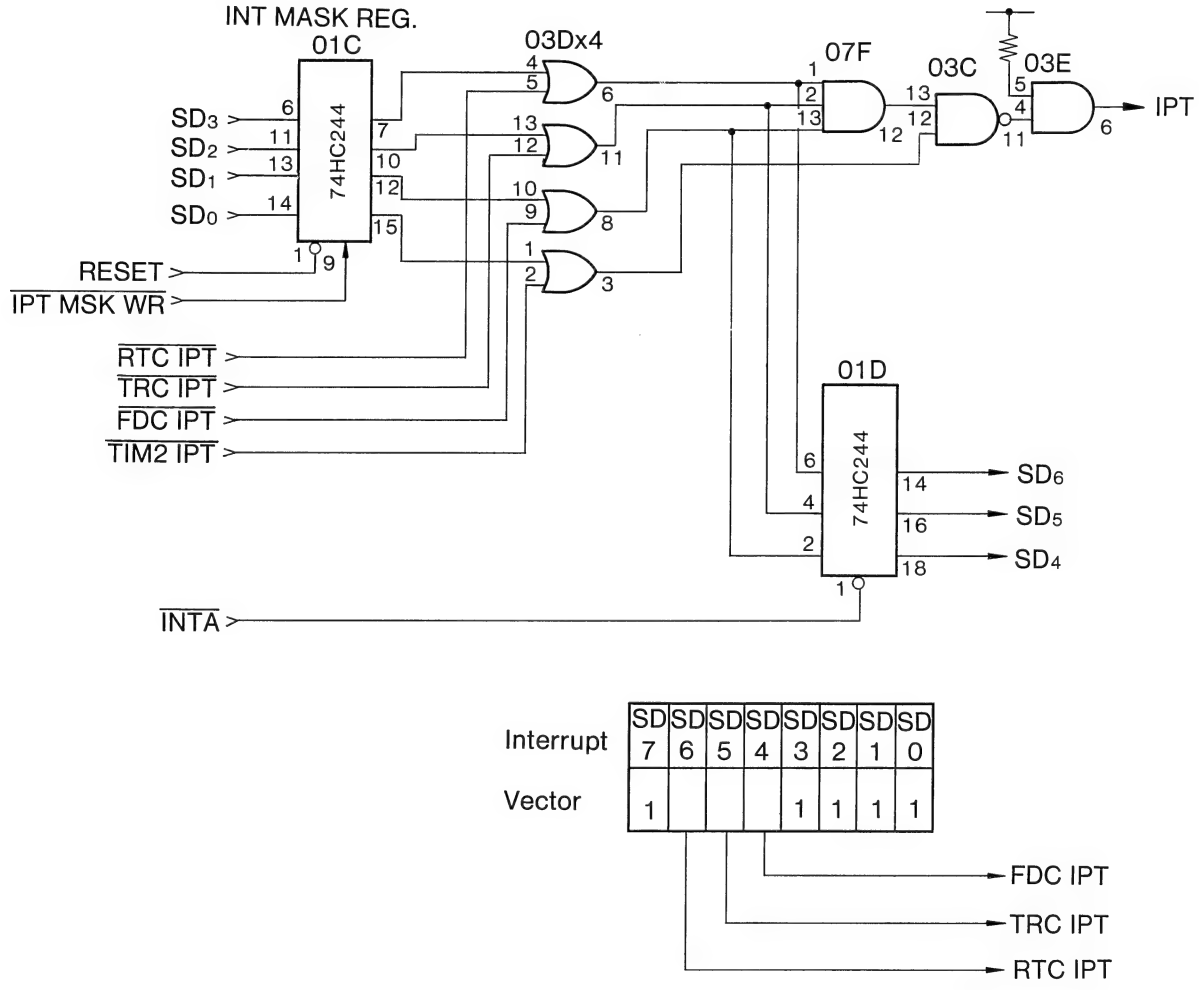


Figure 5-13. Interrupt Control Circuit

5.5.3 NMI (TRAP)

An NMI (non-maskable interrupt) is generated either when the power is shut off or when the voltage of the built-in battery drops below a certain level.

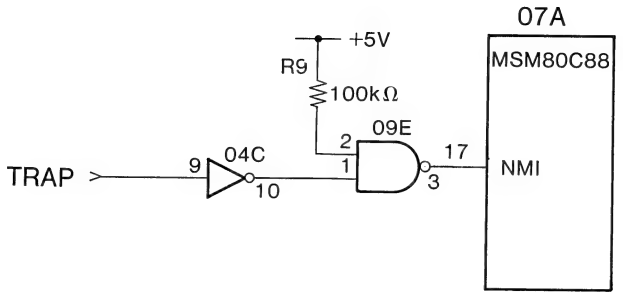


Figure 5-14. NMI Circuit

5.5.4 Level 1 (RTC IPT)

An RTC IPT interrupt is an interrupt issued from the real-time clock (RTC). There are three types of RTC IPT: alarm interrupt, periodic interrupt and update interrupt.

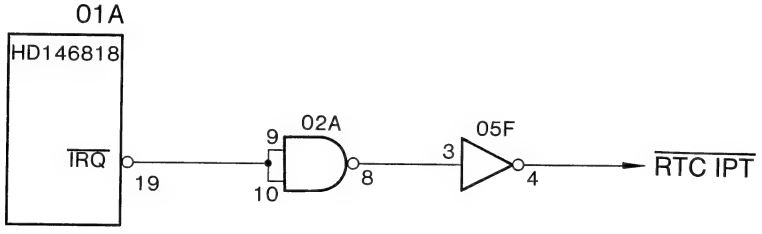


Figure 5-15. RTC Interrupt Generation Circuit

(1) Alarm interrupt Used for alarming the CPU wake-up, etc.

(2) Periodic interrupt Used for the system timer.

(3) Update interrupt Interrupts every 1 sec when set to the enable status.

5.5.5 Level 2 (TRC IPT)

The TRC IPT is an interrupt from the TRC (USART/MODEM). There are three events that trigger the TRC IPT interrupt: RxRDY (Rx ready), CD (carrier detect) and RI (ring indicator). These events are sensed by the IN PORT E command. The interrupt signal is cleared by the TRC IPT CLEAR command.

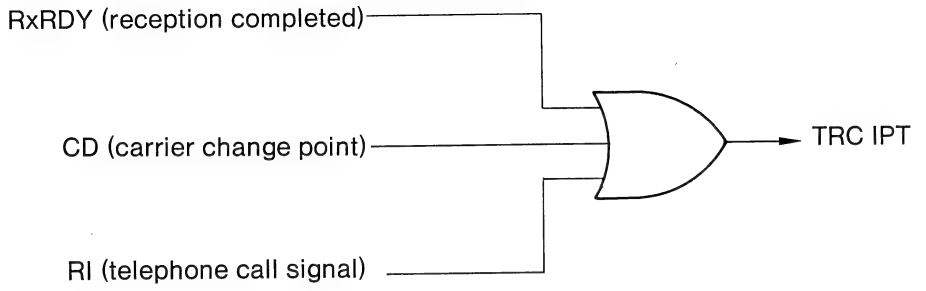


Figure 5-16. TRC Interrupt Generation Circuit

5.5.6 Level 3 (FDC IPT)

This is a command termination interrupt from the FDD controller. The interrupt signal is cleared by reading the FDC status register.

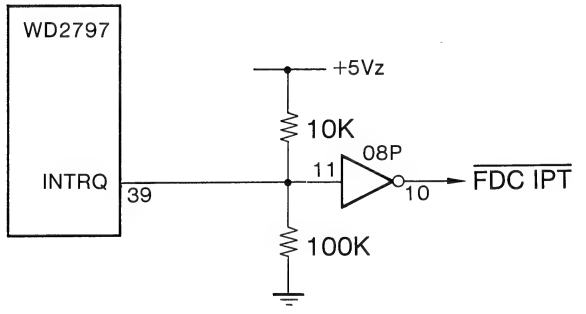


Figure 5-17. FDC Interrupt Generation Circuit

5.5.7 Level 4 (81C55 Timer IPT)

This is an 81C55 timer interrupt (1.30208 s – 10.666ms). With this interrupt, the rising edge of the timer TC (terminal count) is used as the interrupt signal and the interrupt signal is cleared by the 81C55 TIMER IPT CLEAR command.

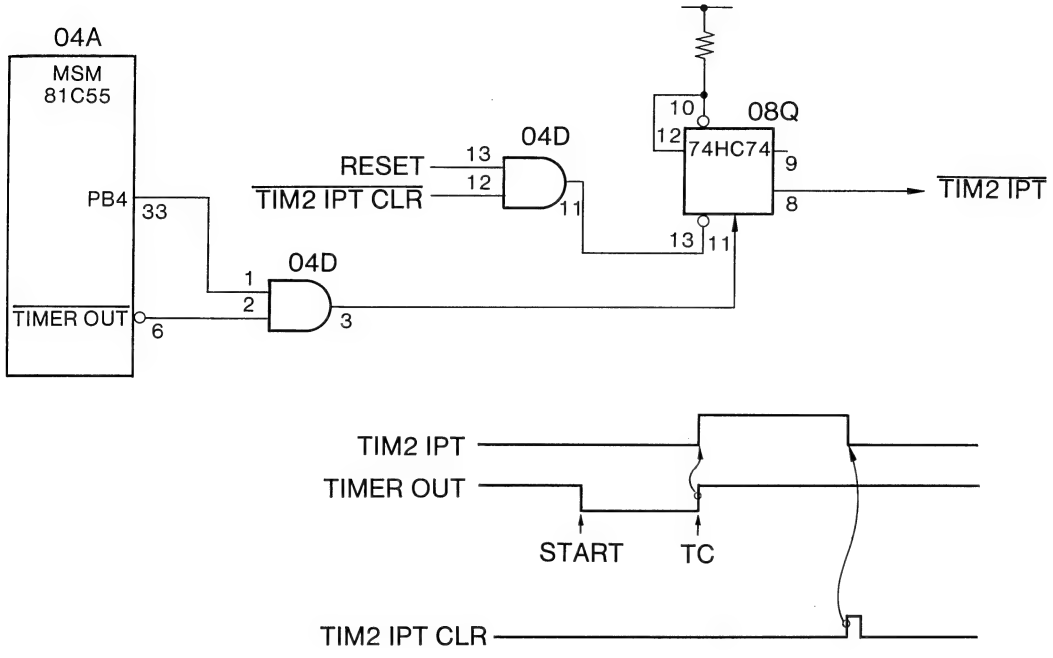


Figure 5-18. 81C55 Interrupt Generation Circuit and Timing Chart

5.6 Keyboard

The keys on the keyboard can be either of a capacitive key switch-type or the mechanical key switch-type. The key entry circuit depends on the type.

5.6.1 Capacitive Key Switch

The input circuit and timing chart for capacitive key switches are shown in Figure 5-19.

(1) Outputs the X-select or Y-select.
(2) Sets the KB CLEAR signal to LOW and the Q5 latch circuit to operable status.
(3) Outputs the $\overline{\text{KB STB1}}$ signal.
(4) A differential waveform is output to pin 3 of Q2 (MSM4051) since key A is depressed. No waveform is output when the switch is set to OFF.
(5) Converts to the TTL level at Q4 (271C) and latches the KB status signal at Q5.
(6) Sets the KB CLEAR signal to HIGH and clears the KB status signal.

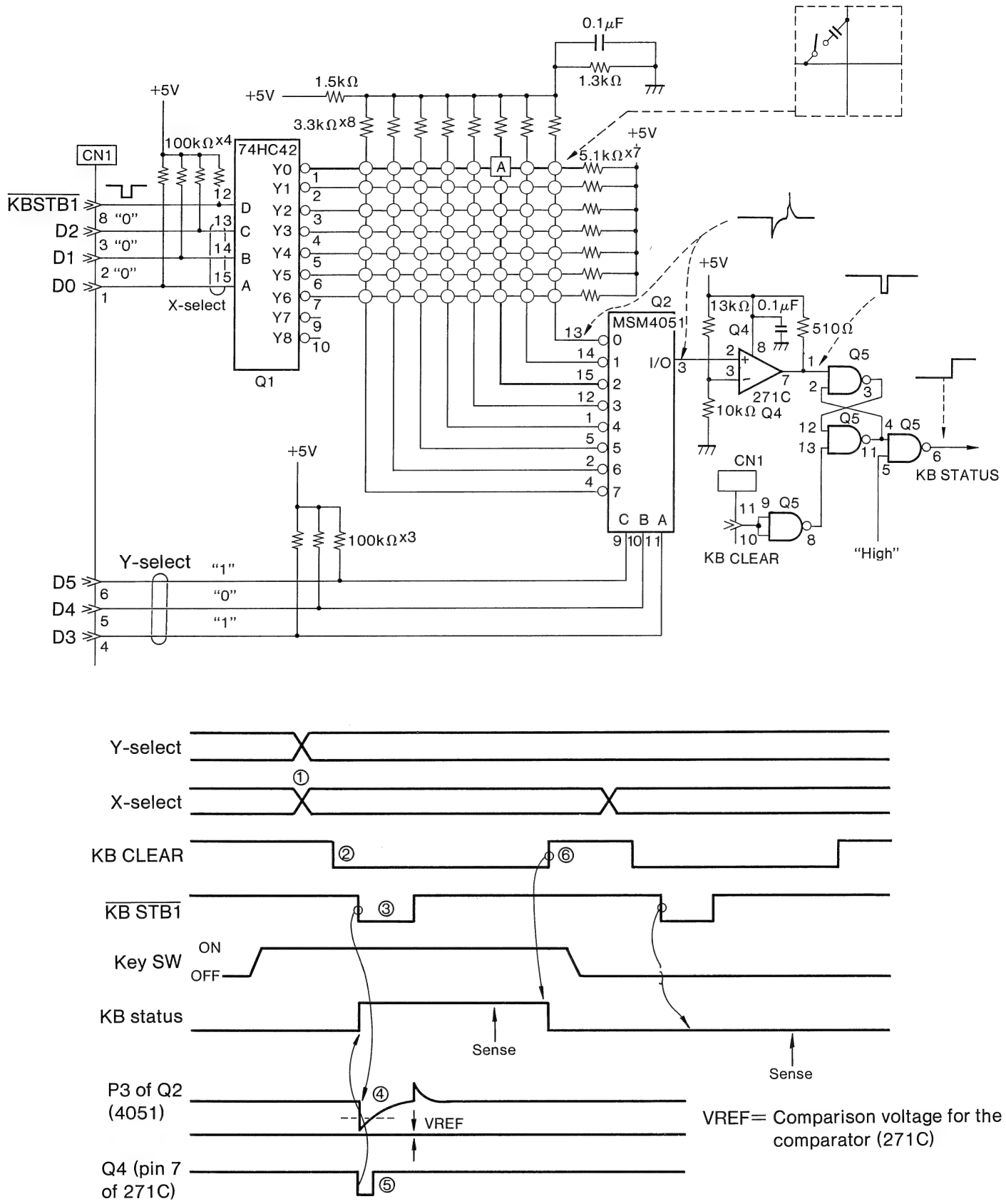


Figure 5-19. Capacitive Key Input Circuit and Timing Chart

5.6.2 Mechanical Key Switch

The input circuit and the timing chart for the mechanical keys are shown in Figure 5-20. When the Y-select and X-select (KB address) are fed to Q1 (74HC42) and Q3 (MSM4051), and the key switch specified by the KB address is set to ON, the KB status is set to HIGH. If the key switch specified by the KB address is set to OFF, the KB status is set to LOW.

Since mechanical key switches generate chattering of approximately 13ms, sensing is performed twice to enter one key status.

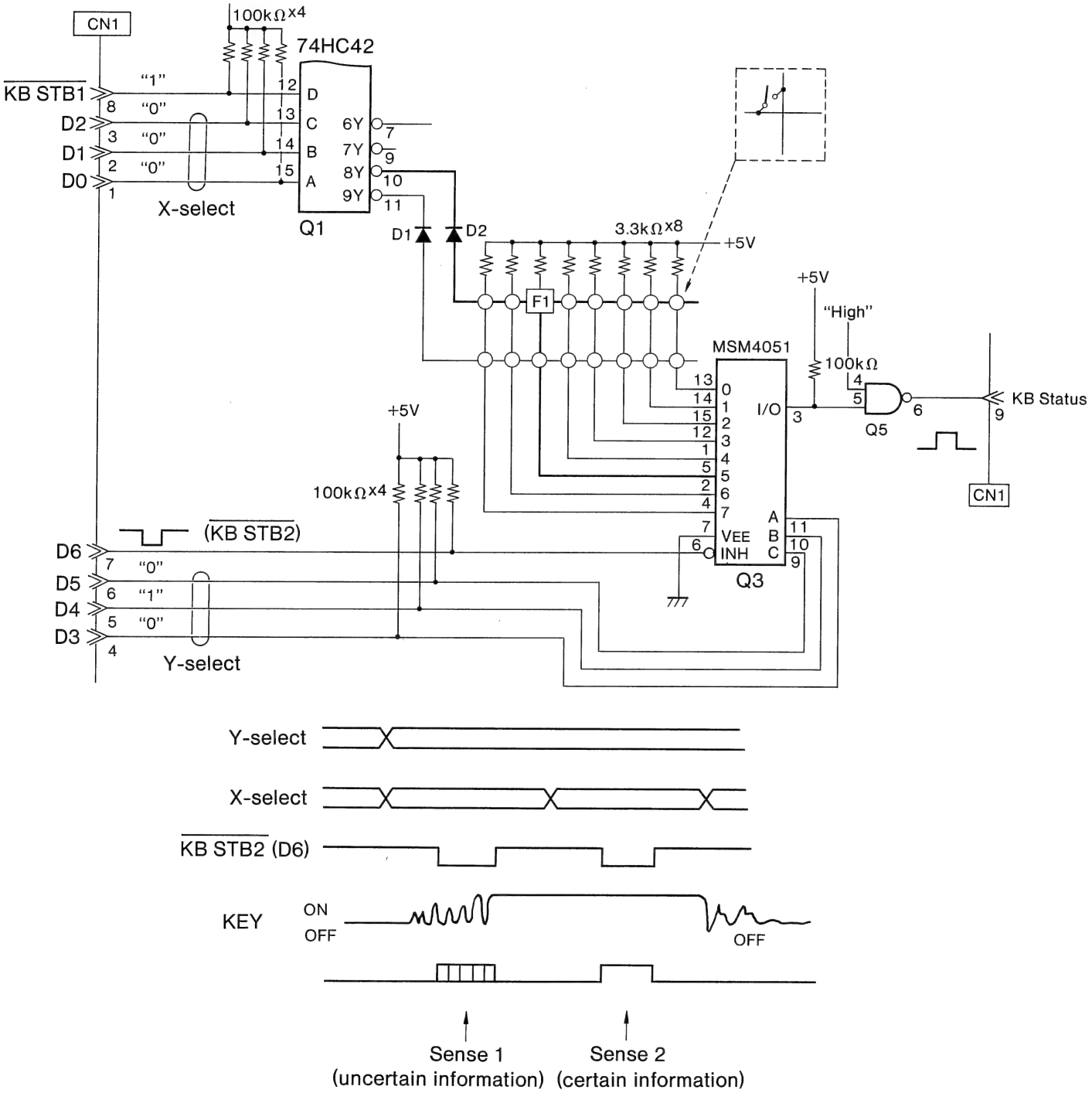


Figure 5-20. Mechanical Key Input Circuit and Timing Chart

5.6.3 Capacitive Key Design and Operation

Depressing a capacitive key causes a capacitance change in the capacitor between two electrodes. This change is used to detect the switch's ON/OFF status (see Figure 5-21). A reset spring exerts a counterforce that pushes the key back up when the pressure is released. A sponge creates a tight contact between the fixed electrode and the moving electrode, and prevents interference by the key when the key is pressed.

When a key is pressed, the moving electrode and the fixed electrode contact each other, forming a capacitor with a capacitance of .45 – 55pF between electrode Y and X. When a negative pulse is entered with the key depressed, a differential waveform is output to electrode X via the capacitor. This differential waveform is detected by the comparator. While the key is not being depressed, no differential waveform is being output.

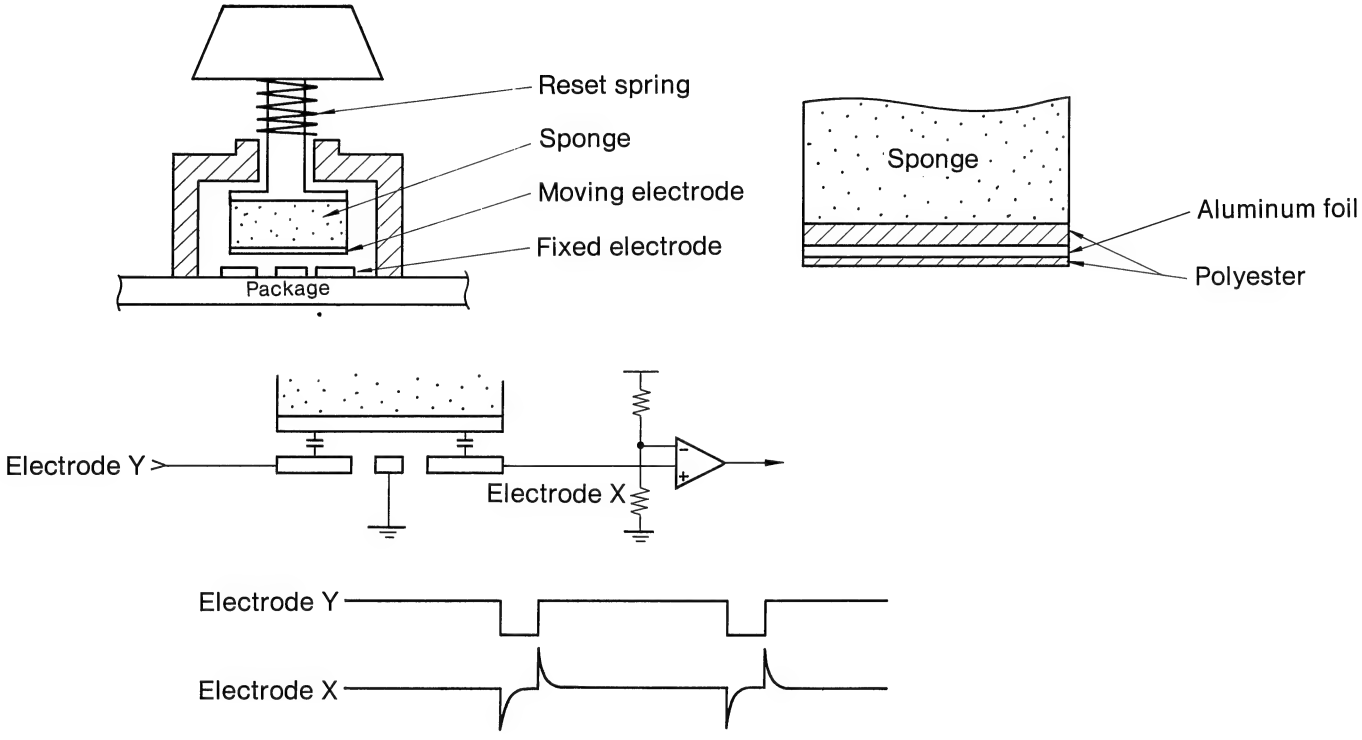


Figure 5-21. Capacitive Key Design and Timing Chart

5.7 Floppy-Disk Drive (FDD)

5.7.1 FDD Peripheral Circuitry

One 3.5-inch floppy-disk drive is standard; one optional FDD can be added.

As Figure 5-22 shows, WD2797 is used as the FDD controller. Data transmission from the FDD is performed in the DMA mode and is controlled by μPD8257.

To minimize power consumption, power is supplied to the FDD block only when the FDD is accessed. The power supply is program controlled.

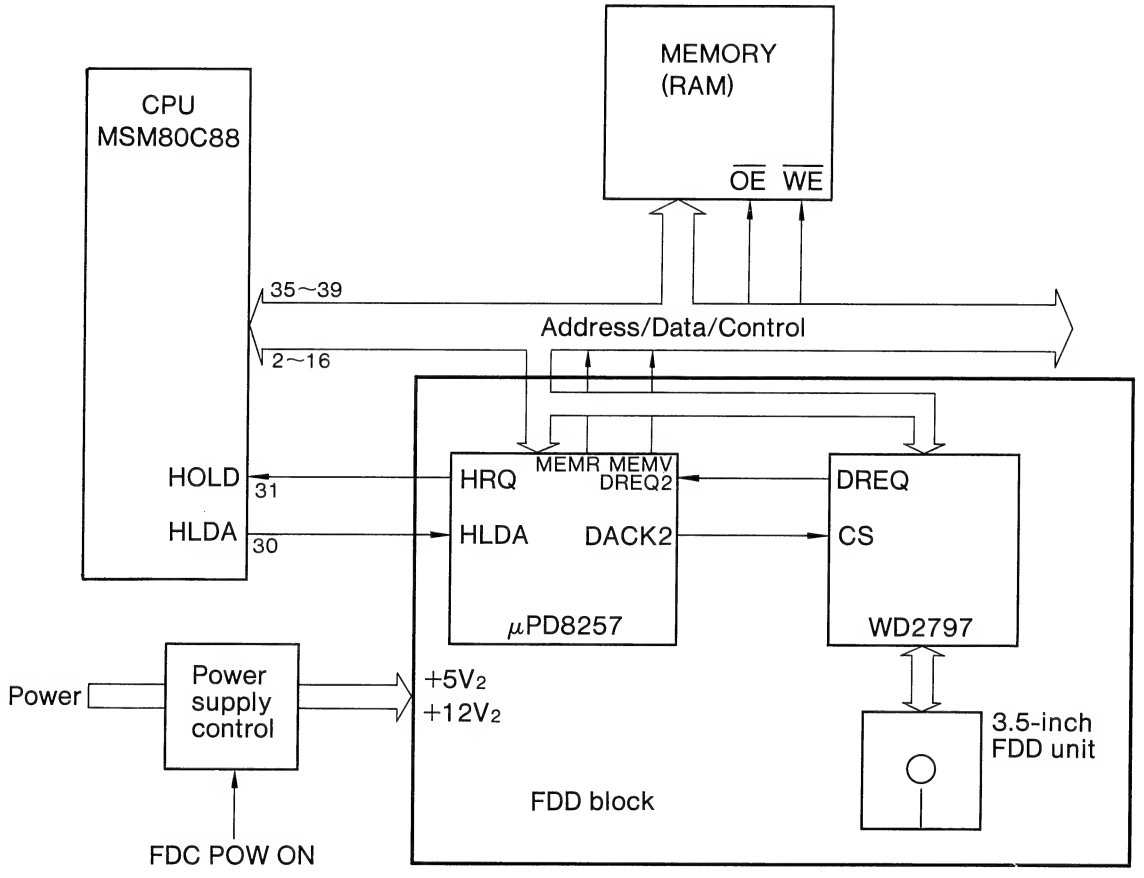


Figure 5-22. FDD and Peripheral Circuitry Block Diagram

5.7.2 FDD Control Program General Flowchart

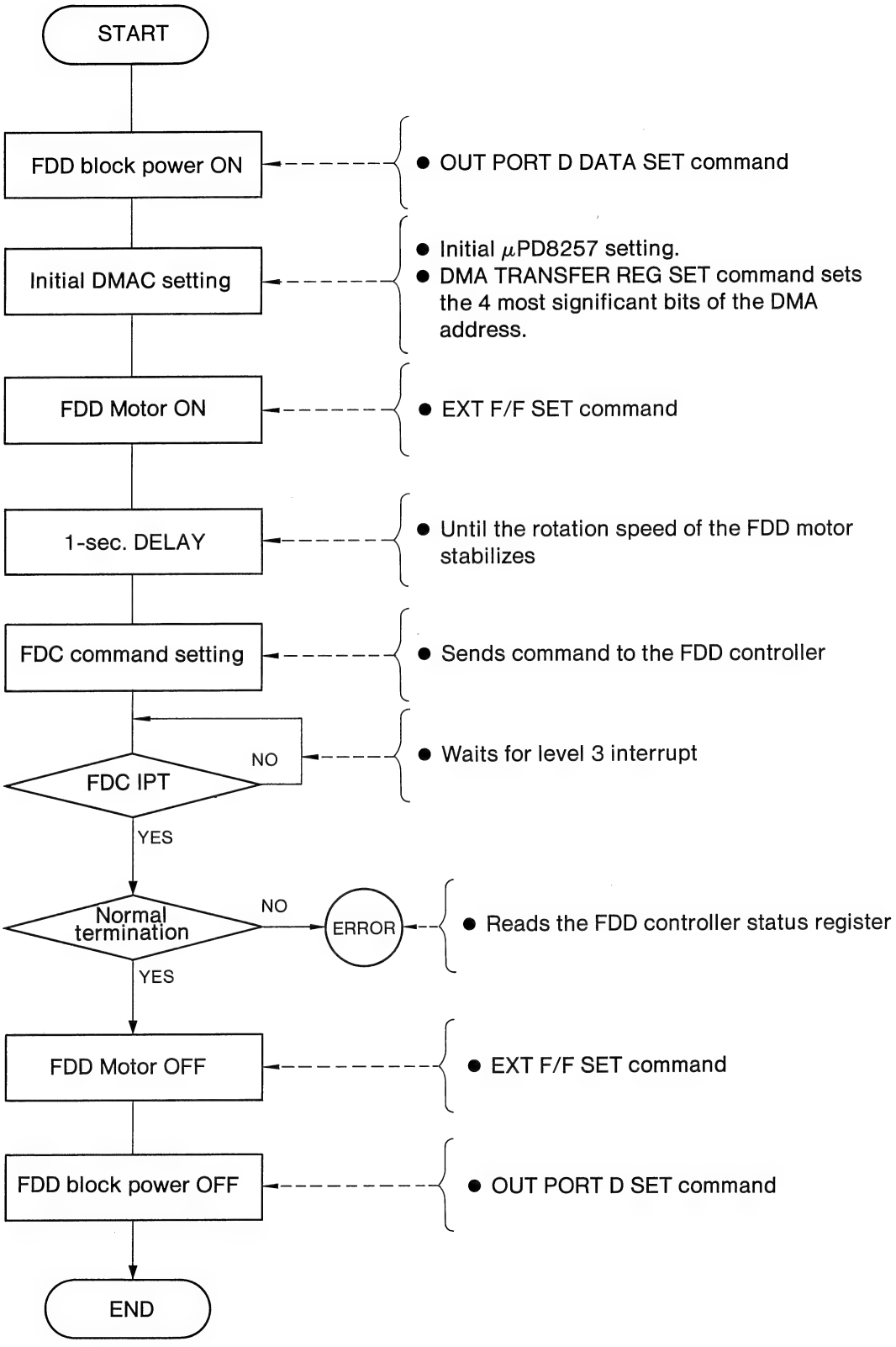


Figure 5-23. FDD Control Program General Flowchart

5.7.3 DMA Control

All data transmission between FDC and the host is performed in the DMA (direct memory access) mode. μPD8257 and its peripheral circuitry for controlling DMA is explained in this section.

A block diagram for DMAC and peripheral circuitry is shown in Figure 5-24.

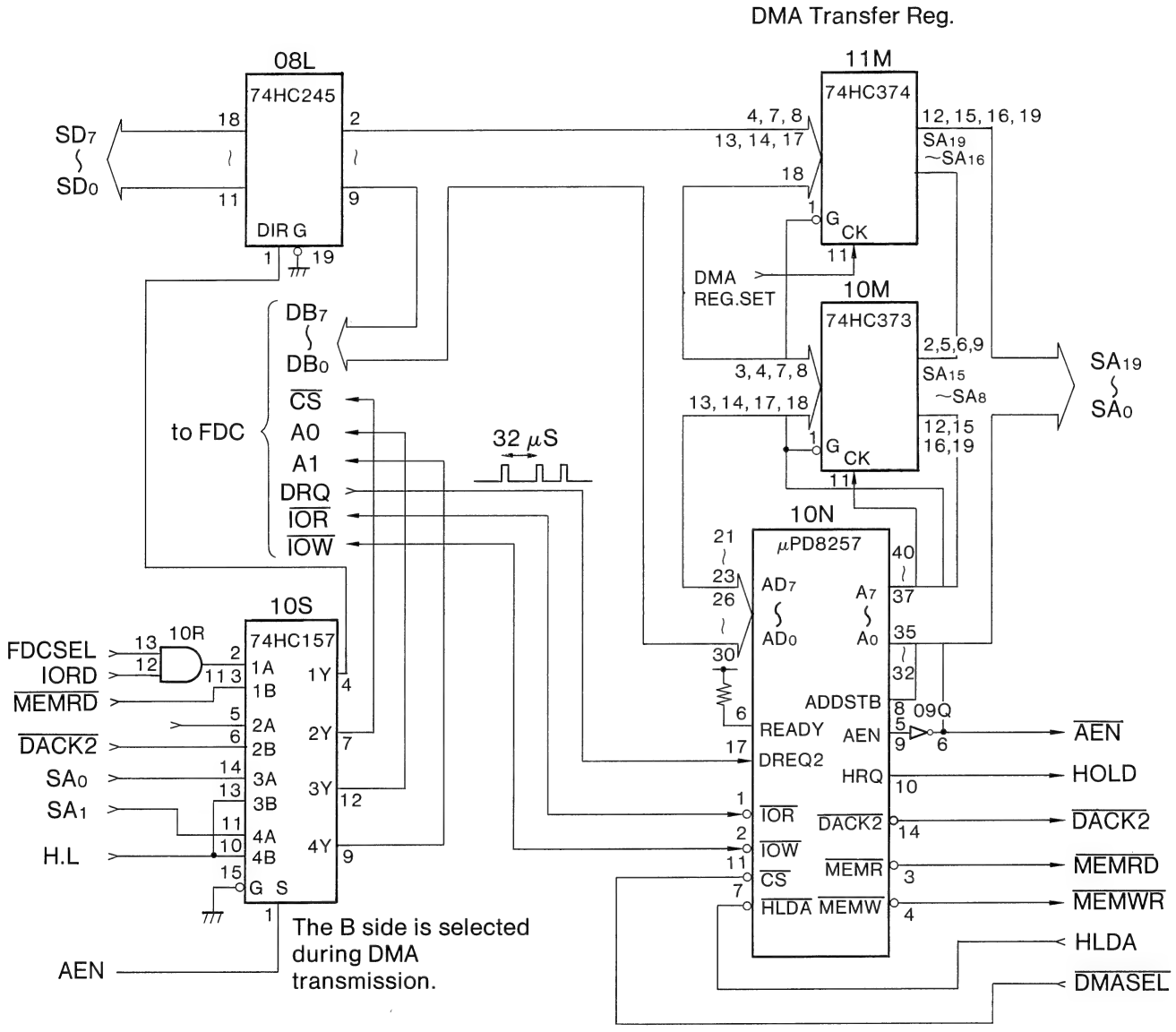


Figure 5-24. Block Diagram of DMAC and Peripheral Circuitry

A data request (DREQ signal) from the FDD controller is entered to the DREQ2 terminal on μPD8257. When the DREQ2 signal is HIGH, μPD8257 sets the HRQ (hold request) terminal to HIGH, and issues a bus request to the CPU. Upon receiving the bus request from the HOLD terminal, the CPU sets the bus on hold status. The CPU notifies μPD8257 that the bus is on hold status by setting the HLDA signal to HIGH.

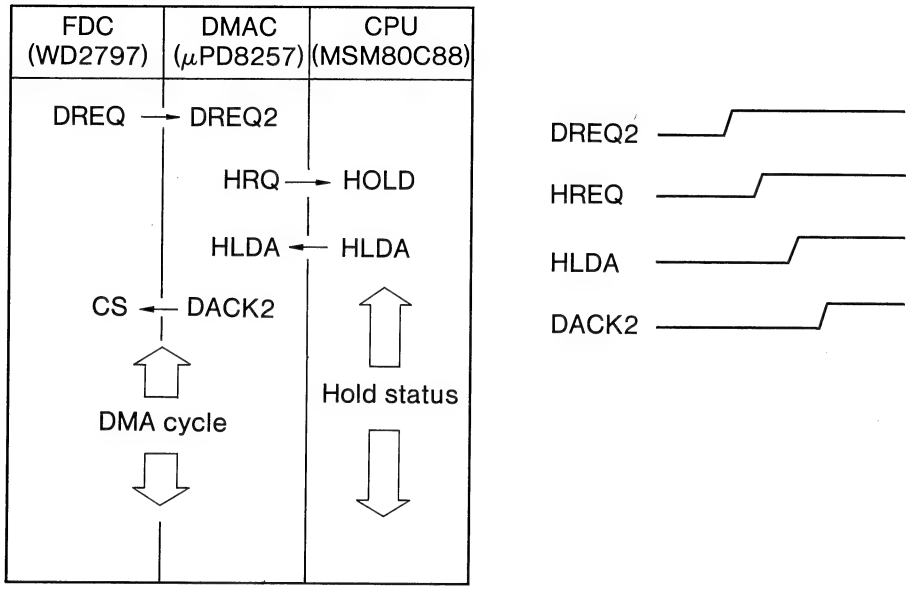


Figure 5-25. DMA Transmission Start Sequence

The above operation passes control of the bus from the CPU to μPD8257. μPD8257 can now perform a DMA transmission between FDC and storage. A timing chart for DMA transmission (FDC storage) is shown in Figure 5-26.

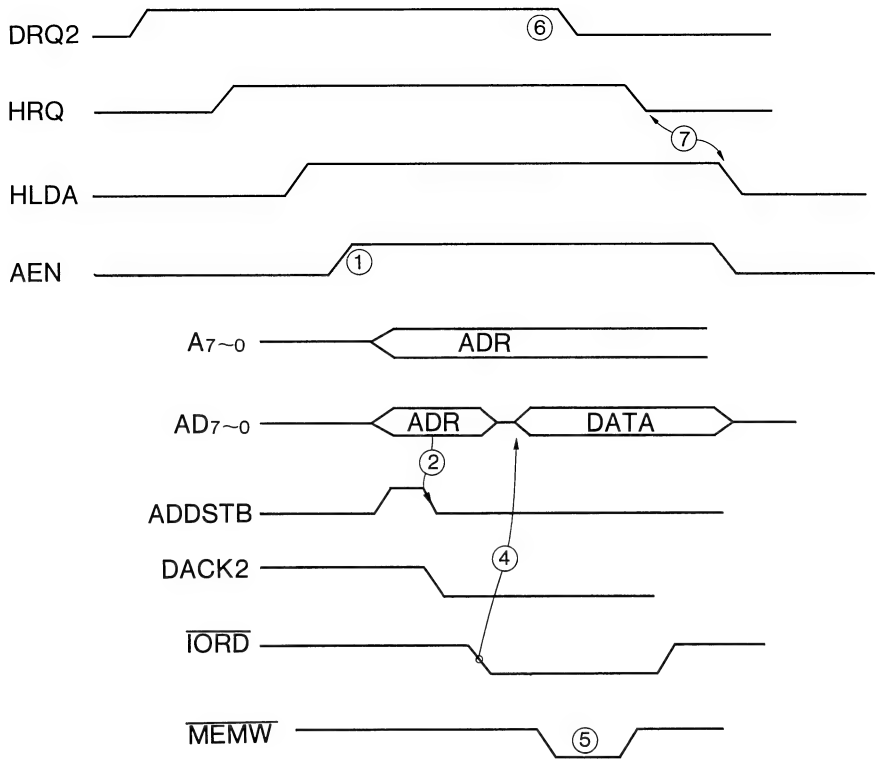


Figure 5-26. DMA Operation Timing Chart

(1) The AEN signal from μPD8257 is set to HIGH when μPD8257 is in the DMA cycle. The AEN signal disables all devices not involved in DMA.
(2) The address (A15-8) that is multiplexed into AD0-7 by the ADDSTB signal is latched at 10M (74HC373).
(3) The memory address for DMA transmission is 20 bits, consisting of the address that is latched at 10M (74HC373), A7-0 from μPD8257 and the 11M (74HC374) DMA transfer register.

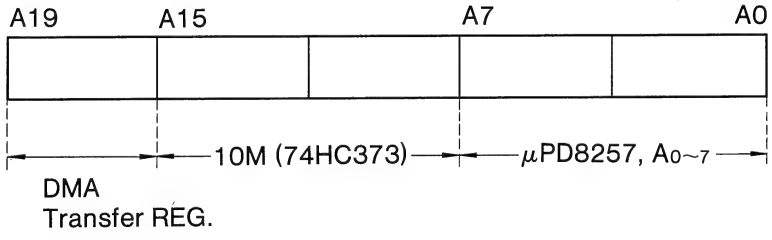


Figure 5-27. DMA Transmission Address Constitution

(4) When the $\overline{IOR}$ signal from μPD8257 changes to LOW, the contents of the FDC data register (data read from FDD) are output to SD0-7. A HIGH level signal is entered to A0 and A1 of FDC from 10S (74HC157).
(5) The data in SD0-7 is written into the storage by means of the $\overline{MEMW}$ signal from μPD8257.

(6) Since DMA transmission has been completed, the DREQ signal from FDC is set to LOW.
(7) The HRQ is then set to LOW. The CPU turns the HLDA signal to LOW and then the control for the bus is passed to the CPU.
(8) FDD generates a data request (DREQ signal) every 32μs. For each DREQ, 1 byte of DMA data is transmitted.

5.7.4 FDD Control

WD2797 controls the 3.5-inch FDD. Besides the logic for controlling the FDD, WD2797 is equipped with write, compensation and data separator logic. WD2797 and its peripheral circuitry are explained in this section.

(1) CPU Interface

The CPU interface for WD2797 is shown in Figure 5-28. A 2 MHz clock is generated by OSC (CX-046C). The period is divided in two by 08Q (74HC74) and the resulting 1 MHz clock is supplied to the CLK terminal on WD2797.

The $\overline{MR}$ terminal on WD2797 is the master reset terminal. A low-level signal (10ms) is fed to this terminal when the power is on. The $\overline{WE}$, $\overline{RE}$ and $\overline{CS}$ terminals are used as the control terminal when reading from or writing to the WD2797 internal registers. Terminal A0 or A1 is used to select the particular internal register. The DREQ terminal is a data request signal generated every 32μs during DMA transmission.

WD2797 sets the INTRQ terminal to HIGH when the command is executed. (INTRQ is a level 3 interrupt to the CPU.)

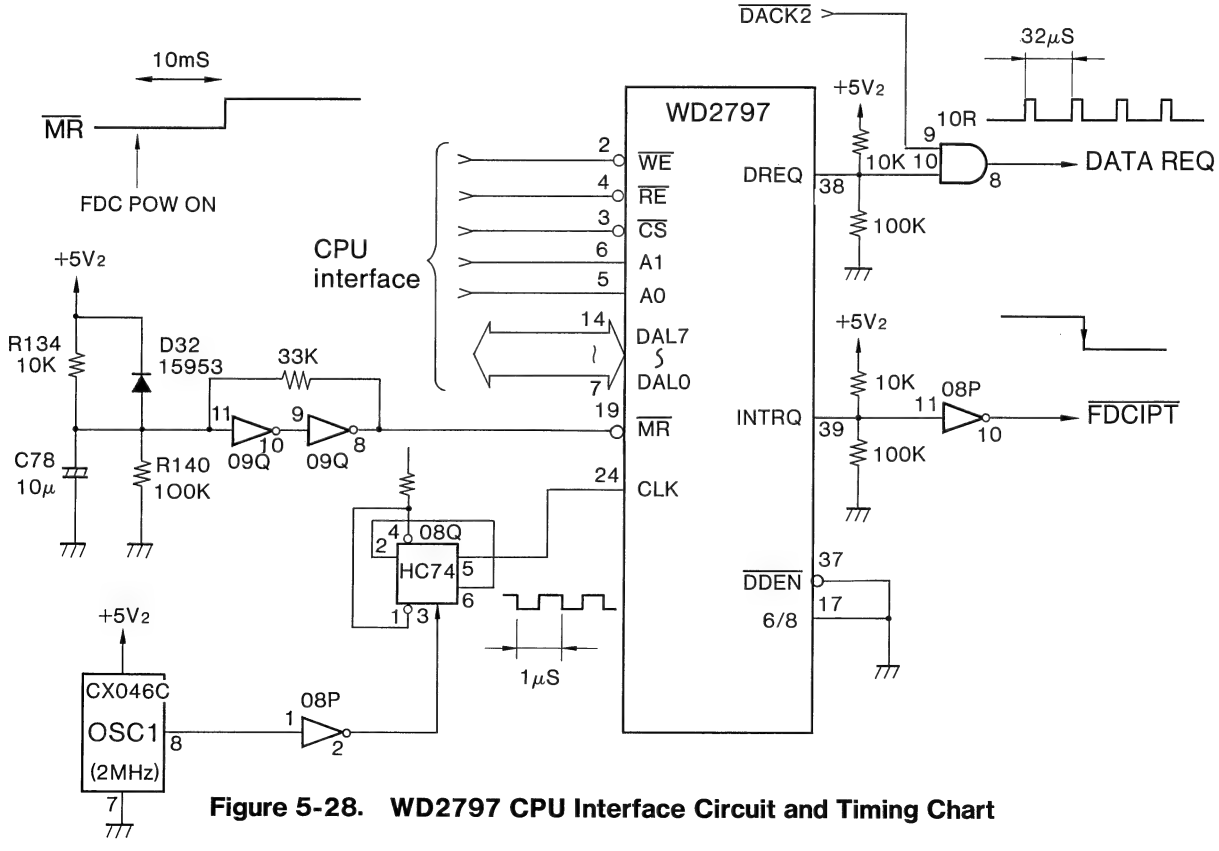
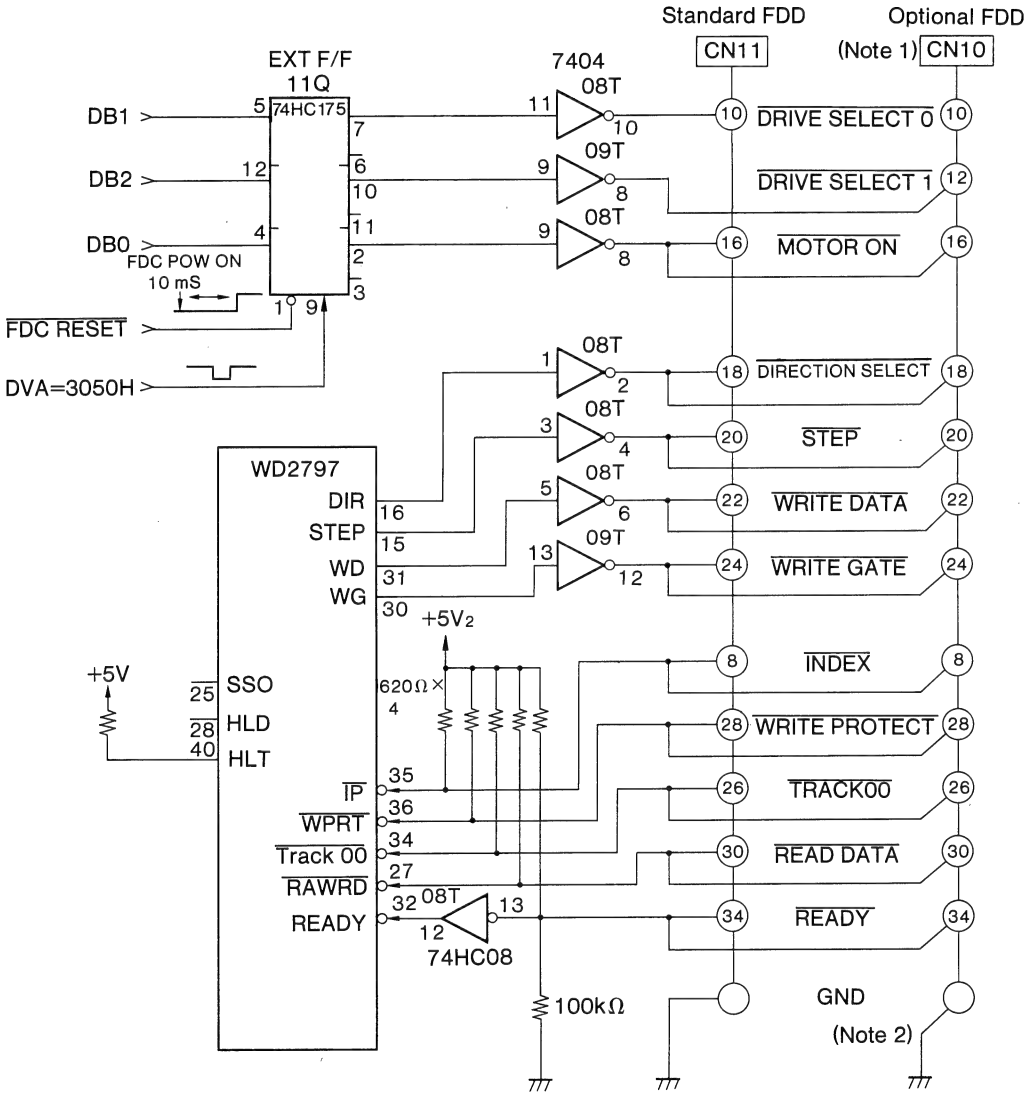


Figure 5-28. WD2797 CPU Interface Circuit and Timing Chart

(2) FDD Interface

The FDD interface circuitry is shown in Figure 5-29. 11Q (74HC175) is a bistable trigger circuit that latches the MOTOR ON or the DRIVE SELECT signal from the FDD unit. It is set by the EXT F/F SET command.

The FDD control signal output from EXT F/F or WD2797 is driven by 7404 (TTL) and is sent to the FDD unit. The FDD control signal for the input system is pulled up using 620 ohms. CN11 is a standard FDD connector. CN10 is an optional FDD connector. Refer to section 4 on FDD units for more information on the FDD interface signal.



Note 1: CN10 and CN11 are connectors located on the OPMP board.

Note 2: Pins 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31 and 33 are used as the ground.

Figure 5-29. FDD Interface Circuit Diagram

(3) VFO and Data Separator

The FDD uses the VCO and data separator that are built into the WD2797. The built-in VCO and the data separator are calibrated using the resistors and the capacitors connected to the PUMP and RPW terminals on the WD2797.

See section 4.2 for a detailed discussion of the calibration procedure.

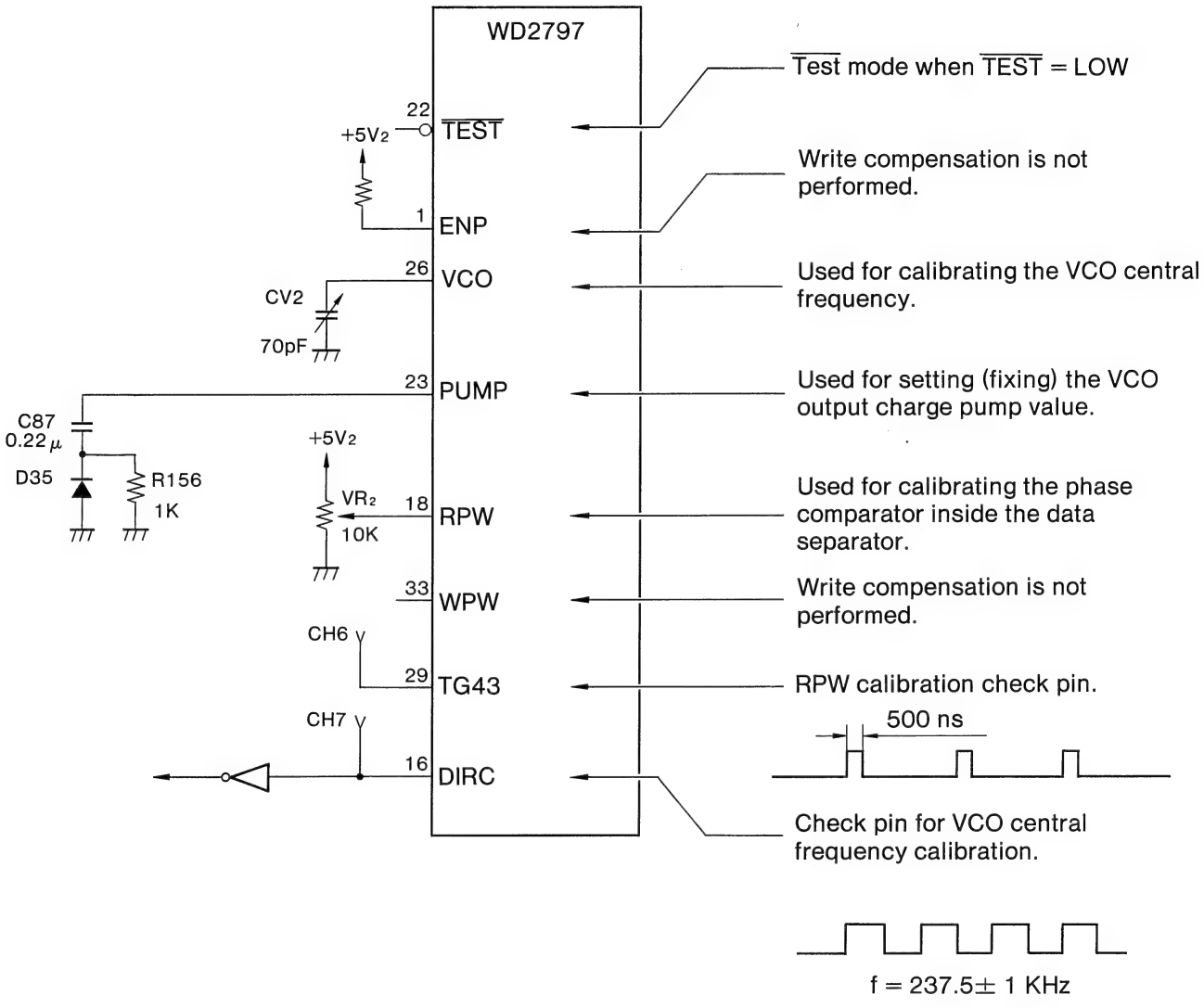


Figure 5-30. WD2797 VFO and Data Separator

(4) FDD Block Power Supply

There are two power supplies to the FDD block: a 5V power is continuously supplied to the FDD block, and a $5V_2$ power is supplied to the block only when the FDD is accessed. The parts involved in supplying the latter 5 are shown below:

Ref. No.	Description	Remarks
08S	WD2797	FDD controller
	CX-046C	2 MHz OSC
10N	μPD8257	DMA controller
08T, 09T	7404	FDD interface driver
	Pull-up resistance	

Table 5-6. Supplied $+5V_2$ Part

5.7.5 Floppy-Disk Drive Unit

Interface Signals

(1) Signal Connector Pin Array (CN1)

Return Pin No.	Signal Pin No.	Signal Name	Input/Output
1	2	N.C. (RESERVE)	
3	4	IN USE	Input
5	6	DRIVE SELECT 4	Input
7	8	INDEX	Output
9	10	DRIVE SELECT 1	Input
11	12	DRIVE SELECT 2	Input
13	14	DRIVE SELECT 3	Input
15	16	MOTOR ON	Input
17	18	DIRECTION SELECT	Input
19	20	STEP	Input
21	22	WRITE DATA	Input
23	24	WRITE GATE	Input
25	26	TRACK 00	Output
27	28	WRITE PROTECT	Output
29	30	READ DATA	Output
31	32	(SIDE ONE SELECT) N.C.	
33	34	READY	Output

Table 5-7. Signal Connector Pin Array

(2) Input Signals

(a) DRIVE SELECT 1-4

When a drive-select pin level is set to LOW, the drive corresponding to the signal is selected and the I/O line is activated, thus enabling a read/write operation.

The drive that responds to a DRIVE SELECT 1-4 signal is determined by the setting of the DIP switch (DS1-DS4) on the drive.

DIP switch DS1 is set when the unit is shipped from the factory. To use a different select line, the DIP switch settings must be changed.

(b) MOTOR ON

The spindle motor is activated when this signal level becomes LOW.

(c) DIRECTION SELECT

This signal specifies the direction of movement of the read/write head when a STEP pulse is received:

HIGH: Toward the periphery (STEP OUT)
LOW: Toward the center (STEP IN)

(d) STEP

Each time a LOW pulse (STEP signal) is received, the read/write head moves by one track in the direction specified by the DIRECTION SELECT signal.

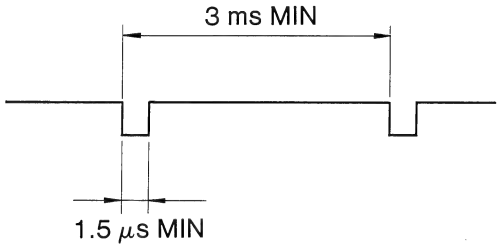


Figure 5-31. STEP Signal Waveform

(e) WRITE DATA

This signal represents the data that is to be recorded on the disk. Each time the level changes from HIGH to LOW (or vice versa), the direction of the current flow to the read/write head is reversed to record a data bit. Data recording is possible only when the WRITE GATE signal is LOW.

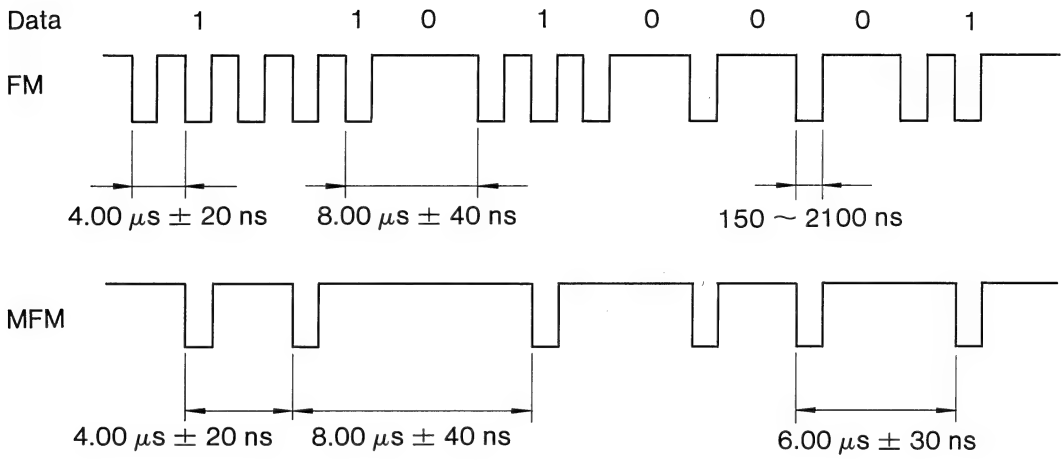


Figure 5-32. Data Write Timing

(f) WRITE GATE

Data can be recorded on a disk only when this signal level is LOW.

Data reproduction or a seek operation is enabled when this signal level is HIGH.

(g) IN USE

The IN USE LED for the drive selected by the DRIVE SELECT signal is lit only if this signal level is HIGH. If this signal level is LOW, the IN USE LEDs for all the drives that are connected, are lit regardless of the DRIVE SELECT signal.

(3) Output Signals

(a) INDEX

The rising edge of this signal represents the disk rotation reference position. This signal level is HIGH when there is no diskette in the drive unit.

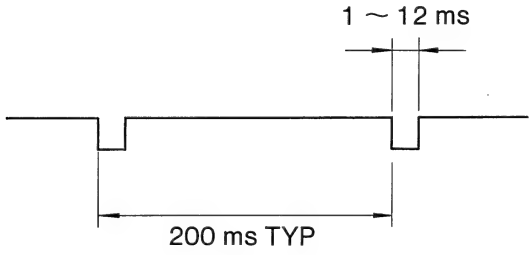


Figure 5-33. INDEX Signal Waveform

(b) TRACK 00
A LOW level for this signal indicates that the read/write head of the drive selected is at TRACK 00.

(c) WRITE PROTECT
This signal indicates whether or not the diskette loaded in the drive is write-protected:

LOW: Write-protected
HIGH: Write-enabled

(d) READ DATA
This signal represents the pulse signal obtained by wave-shaping the analog signal read from the diskette. This signal includes the clock and the data.

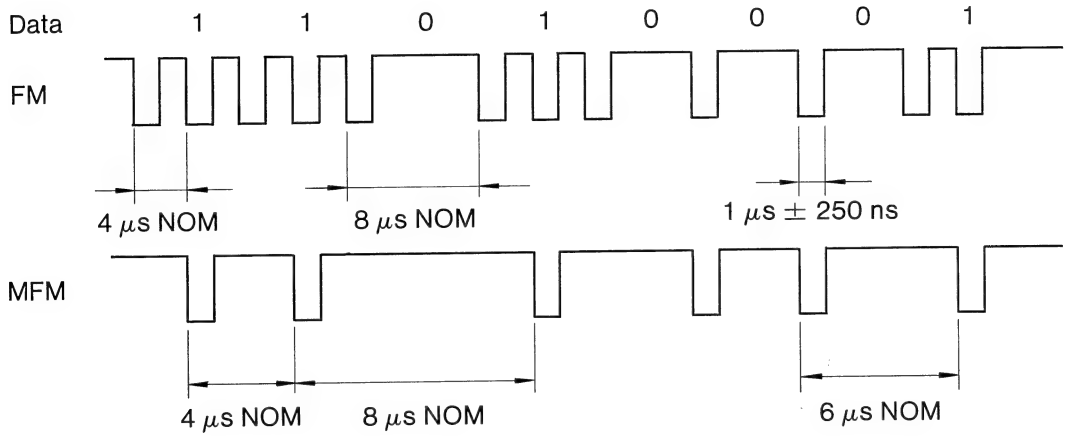


Figure 5-34. Data Read Timing

(e) READY
A LOW level of this signal indicates that a read/write access operation is possible for the selected drive.

This signal level becomes LOW and access becomes possible when all the following conditions are met:

(i) +5V DC and +12V DC power are supplied.

(ii) Two INDEX pulses were detected after the disk rotation has started.

(iii) A diskette is loaded.

(4) Control Timing

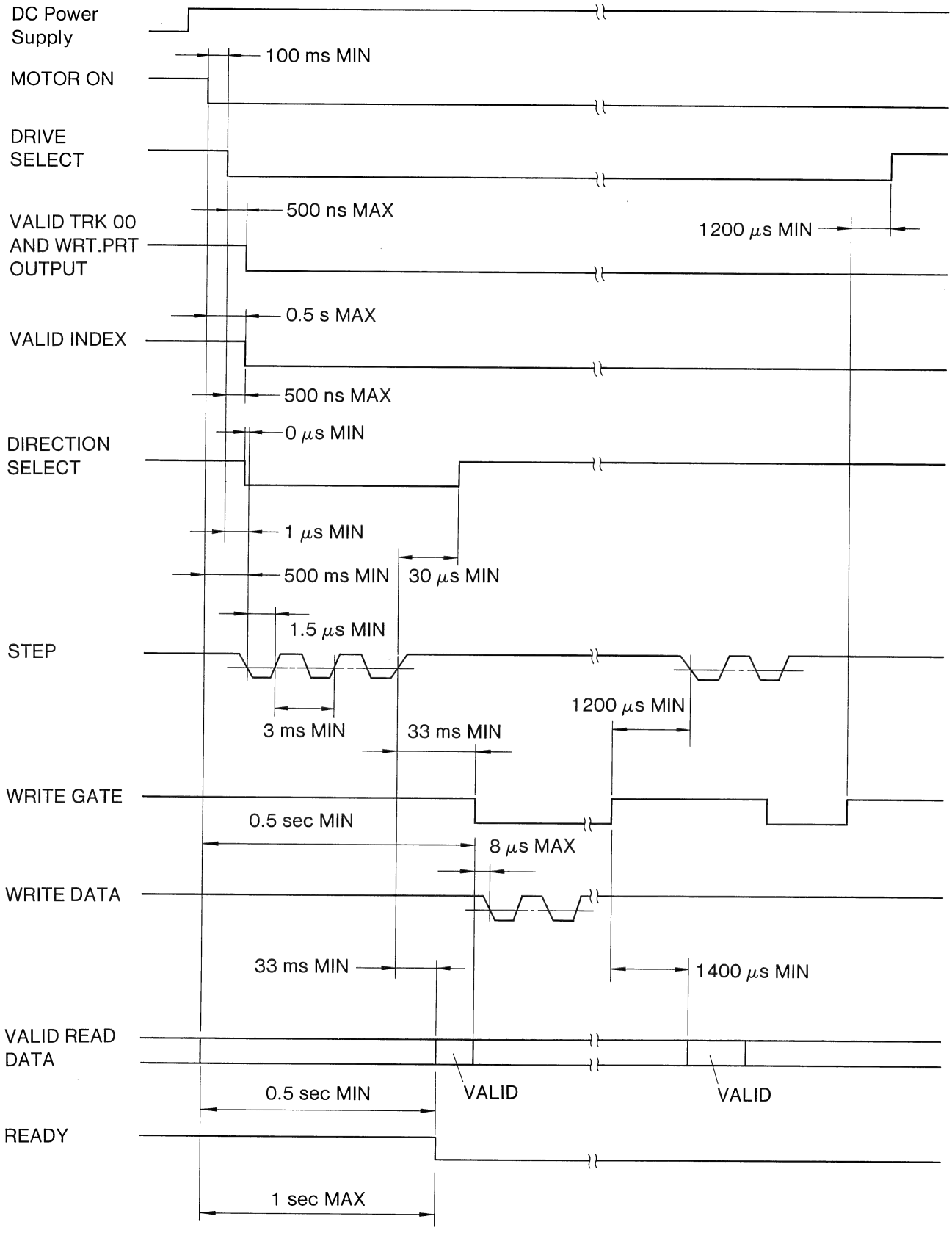


Figure 5-35. Control Timing

(5) Power Supply Interface

+12V DC and +5V DC power are used. +12V DC drives the spindle motor and the stepping motor; +5V DC is used to power the read amplifier logic circuit.

Pin Number	Power Supply
1	+5V DC
2	+5V Return
3	+12V Return
4	+12V DC

Table 5-8. Power Supply Connector Pin Array (CN2)

(6) DIP Switches

(a) DS1-DS4

If two or more drives are to be connected, set the SELECT NO for each of the drives using these DIP switches. For example, if DS2 is set to ON for a drive, that drive will be selected and be accessible when the DRIVE SELECT 2 signal is LOW.

(b) LED display (red)

The LED display lights when that device is selected by the DRIVE SELECT signal or when the IN USE signal level is LOW.

(7) Control CPU Process Flowchart

The process flowchart of the control CPU is shown in Figure 5-36.

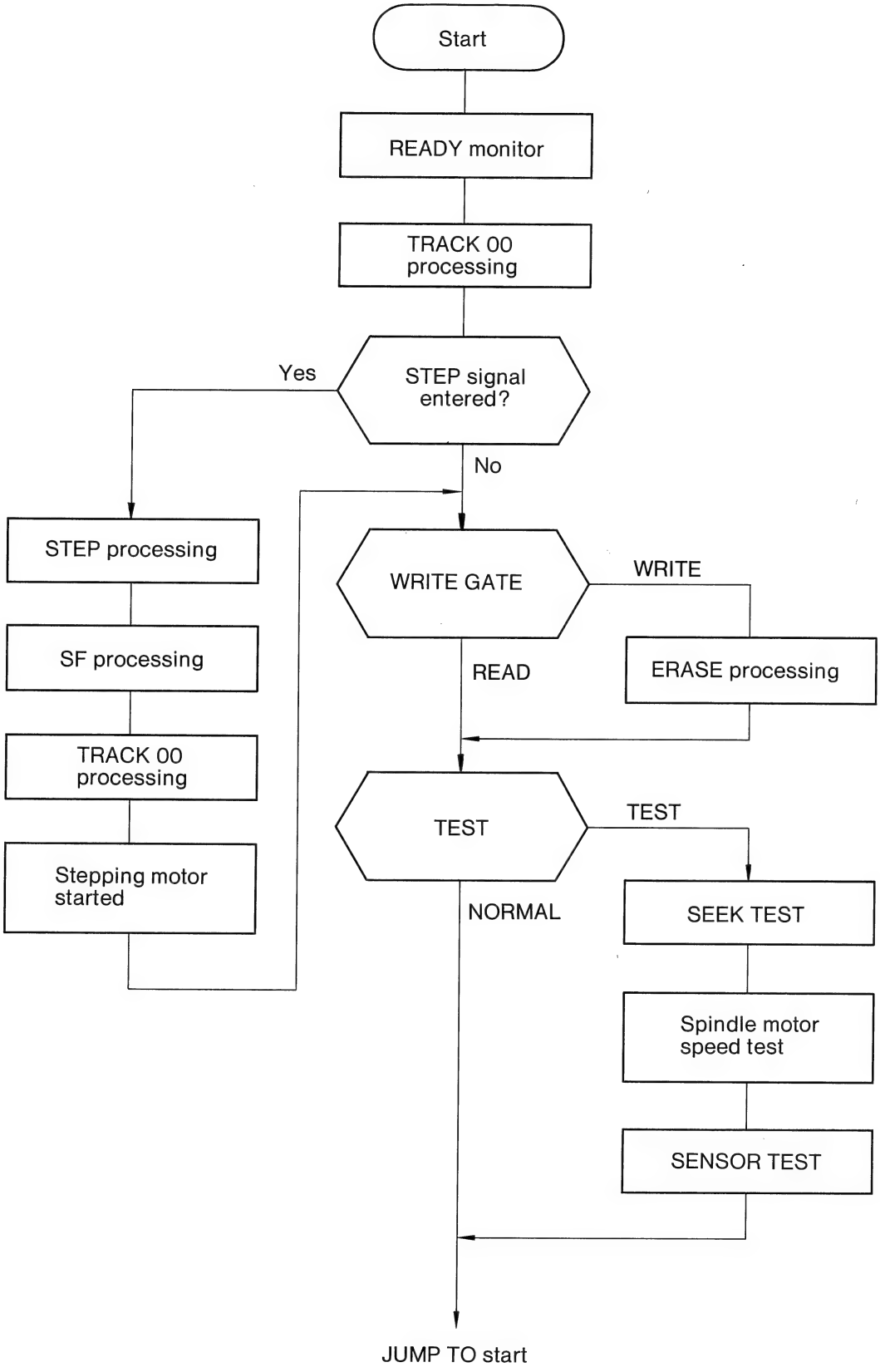


Figure 5-36. Control CPU Process Flowchart

5.8 Printer Interface

The printer interface circuit conforms to the Centronics standard.

As shown in Figure 5-37, the BUSY1 signal for the printer is read from PC1 on the 81C55. Since the printer is not busy when the BUSY1 signal is LOW, the printer data is output from PA0 through PA7 on the 81C55. After the data is output, the $\overline{\text{PR STROBE}}$ signal is output. The printer uses the $\overline{\text{PR STROBE}}$ signal to receive data, then sets the BUSY1 signal to HIGH (printer busy). The BUSY1 signal is changed to LOW when the printer is ready to receive the next data.
The CPU sends the next data to the printer when the BUSY1 signal becomes LOW.

The BUSY2 signal is the inverse of the BUSY1 signal.

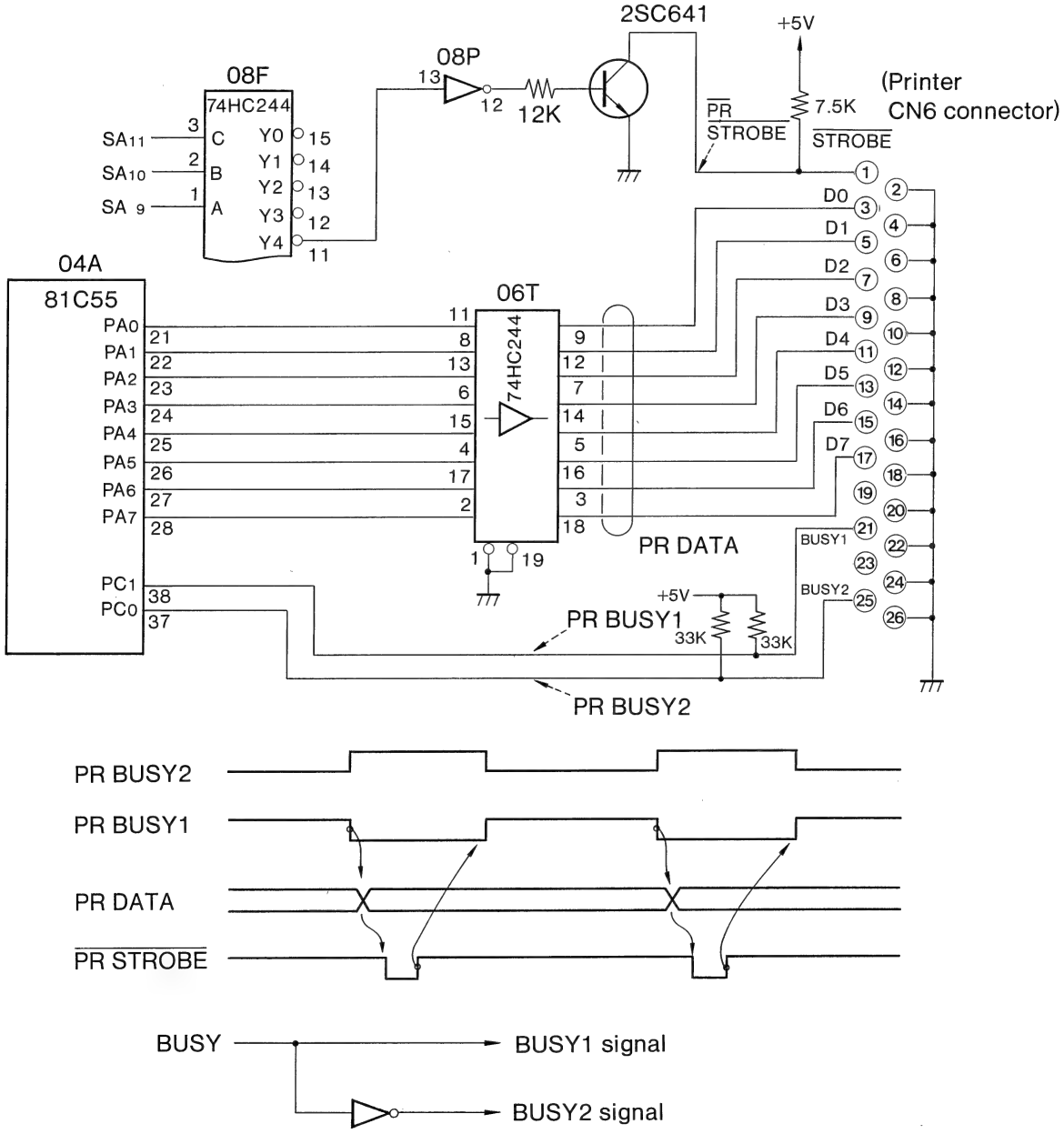


Figure 5-37. Printer Interface Circuit Diagram and Timing Chart

5.9 LCD

5.9.1 Configuration

As shown in Figure 5-38, the LCD block on the TANDY 600 is comprised of the LCD unit and OPLF board (LCD controller).

The LCD unit is divided into four planes whose display is controlled by signal lines D1, D2, D3 and D4. The LCD controller OPLF board controls two LCDCs (HD61830), one as a master and the other as a slave. The left plane of the LCD is controlled by the master HD61830, and the right plane is controlled by the slave HD61830.

When the LCD (VRAM) is accessed by the CPU, the CPU sends separate commands and parameters to the master and the slave LCDC.

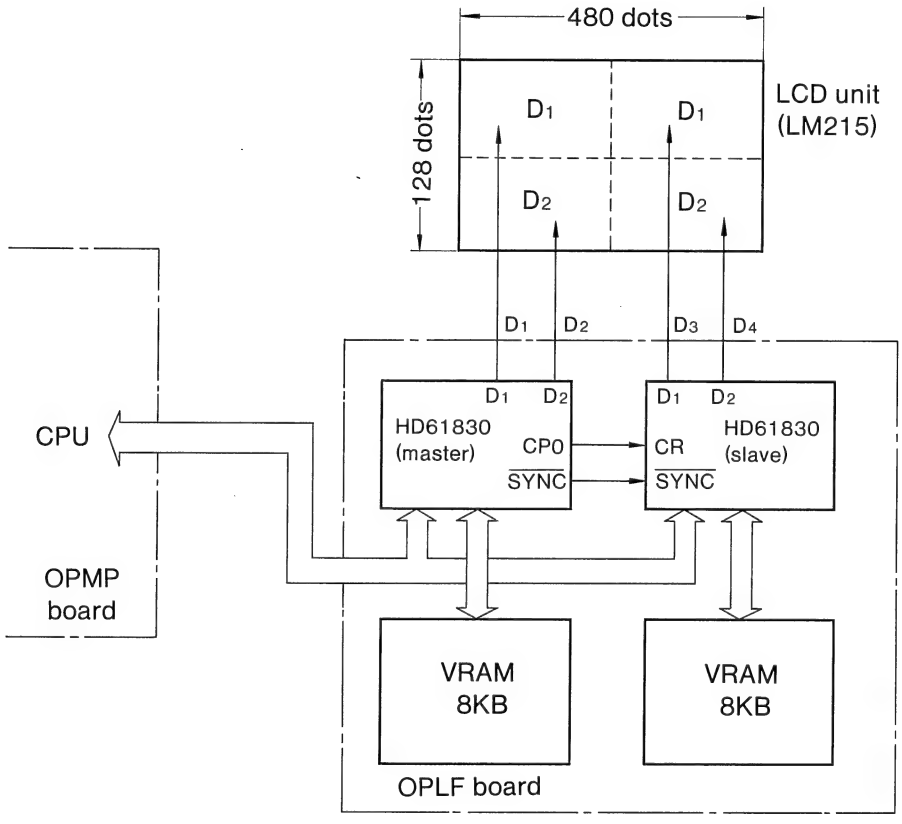


Figure 5-38. LCD Block Diagram

5.9.2 LCD Controller (HD61830)

(1) CPU Interface

The CPU interface circuit of the HD61830 is shown in Figure 5-39. The clock divides PCLK into two at 05A. The HD61830 is reset when the RES terminal level is Low.

Data bus (DB_7 through DB_0), chip select ($\overline{CS}$), enable (E) and read/write (R/$\overline{W}$) serve as the interface between the CPU and the HD61830.

$\overline{LCDC1SEL}$ is connected to the master $\overline{CS}$ terminal, and $\overline{LCDC2SEL}$ is connected to the slave $\overline{CS}$ terminal.

The signal specifying the data transmission direction is input through the R/$\overline{W}$ terminal.

Data reading is possible when the level of the E terminal is HIGH. The falling edge of the E terminal level is used as the data write timing.

The data register is selected when the RS terminal is HIGH and the instruction register is LOW.

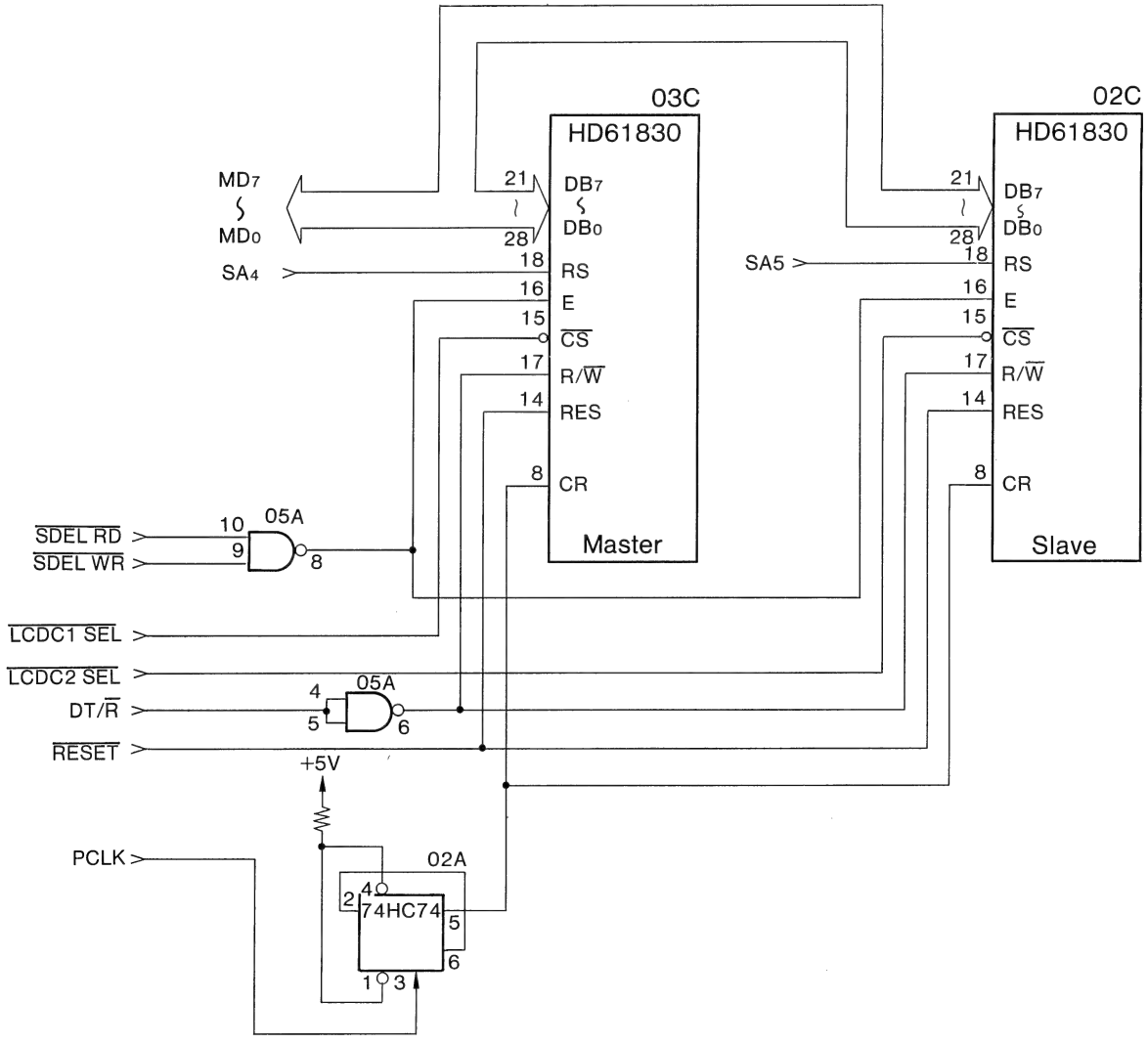


Figure 5-39. HD61830 CPU Interface Circuit Diagram

(2) HD61830 – VRAM Interface

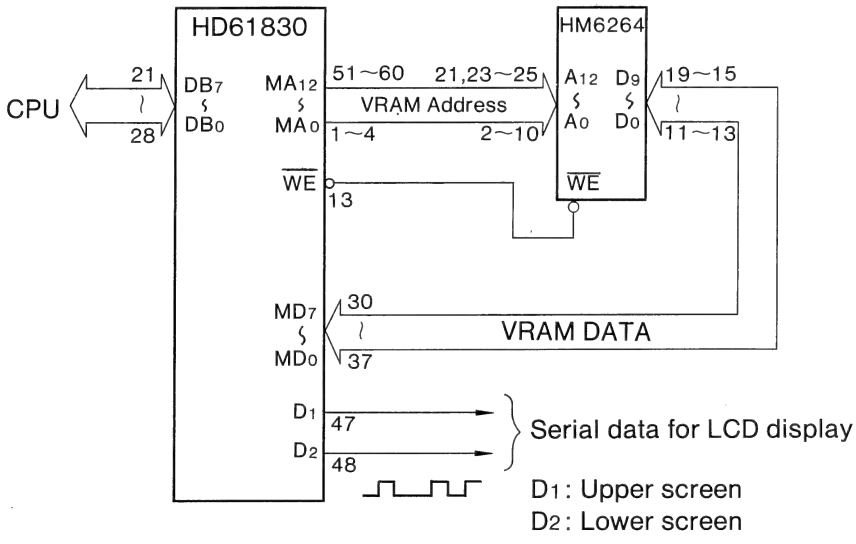
The circuit diagram for the HD61830 and VRAM and the timing chart are shown in Figure 5-40.

HD61830 accesses VRAM for two reasons: refresh the screen for display purpose, or enable the CPU to access VRAM for display, etc.

HD61830 processes both types of access on a time-sharing basis. A VRAM address that is output from MA12 through MA0 of 02C or 03C (both HD61830) is input to A12 through A0 of 01C or 04C (both HM6264LP). If the $\overline{WE}$ signal level is HIGH, the VRAM data is output from D0 through D7 of HM6264LP. HD61830 then reads the data from MD7 through MD0.

If the VRAM is accessed for refreshing a screen, the data is parallel/serial converted, and serial data for display use is output from D1 and D2. If the VRAM is accessed for use by the CPU, the VRAM data is directed to the data output register located within the HD61830.

The rising edge of the $\overline{WE}$ signal is the timing used by the HD61830 for writing data to VRAM.



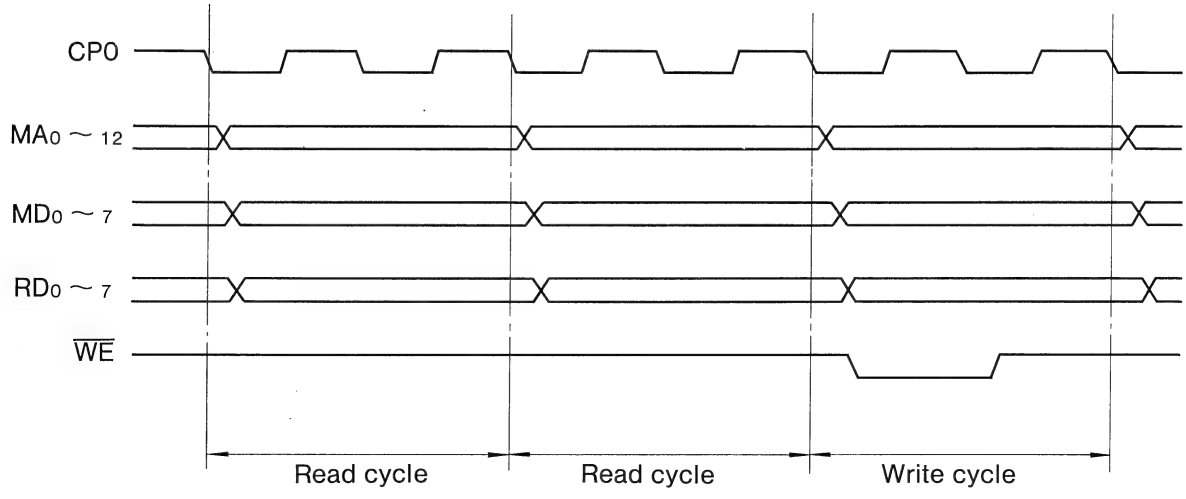


Figure 5-40. HD61830 VRAM Interface Circuit Diagram and Timing Chart

(3) LCD Unit Interface

The interface circuit and the timing chart for the HD61830 LCD unit are shown in Figure 5-41.

As the timing chart shows, data output from pins D1 and D2 of the HD61830 is synchronized to the CL2 signal.

The LCD unit inputs the D1 and D2 signals to a 240-bit shift register using the CL2 signal as the timing. After 240 bits have been received in the shift register, the data for one line is latched using the falling edge of the CL1 signal as the timing, and the data is displayed on the LCD.

FLM is a synchronization signal that is generated every time a screen is scanned. The LCD driving voltage is changed to an alternating current using the MB signal.

V_{EE} and Vo are reference voltages for the LCD that are created in the OPMP board.

Signal	Function
CL1	Signal used for latching display data
CL2	Clock used when shifting display
FLM	Frame signal (display synchronization)
MB	Signal used for converting LCD drive voltage to AC
D1	Serial display data for upper screen
D2	Serial display data for lower screen
Vo	−6.9V (normal)
V_{EE}	−10V (normal)

Table 5-9. LCD Interface Signals

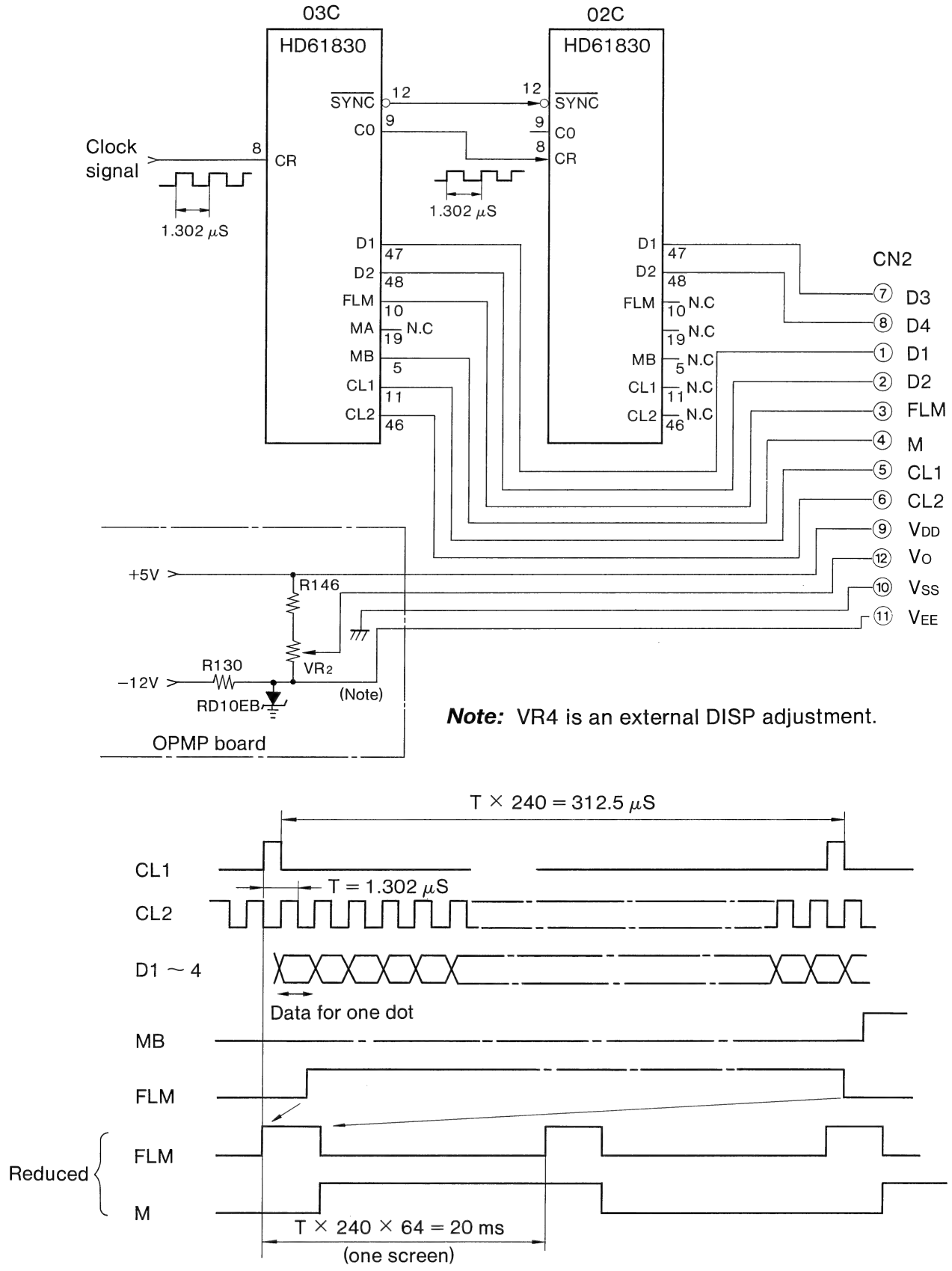


Figure 5-41. HD61830 LCD Interface Circuit Diagram and Timing Chart

(4) Abbreviated LCDC Control Program Flowchart

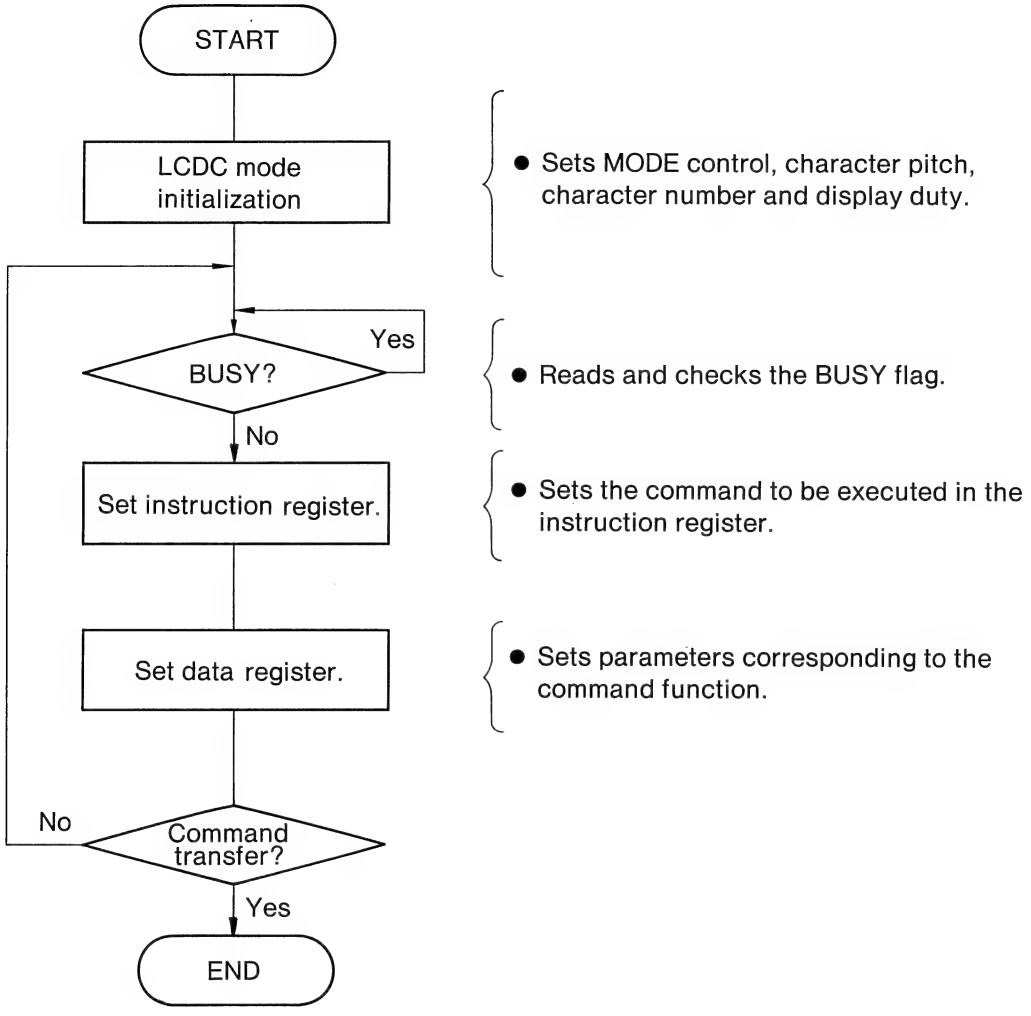
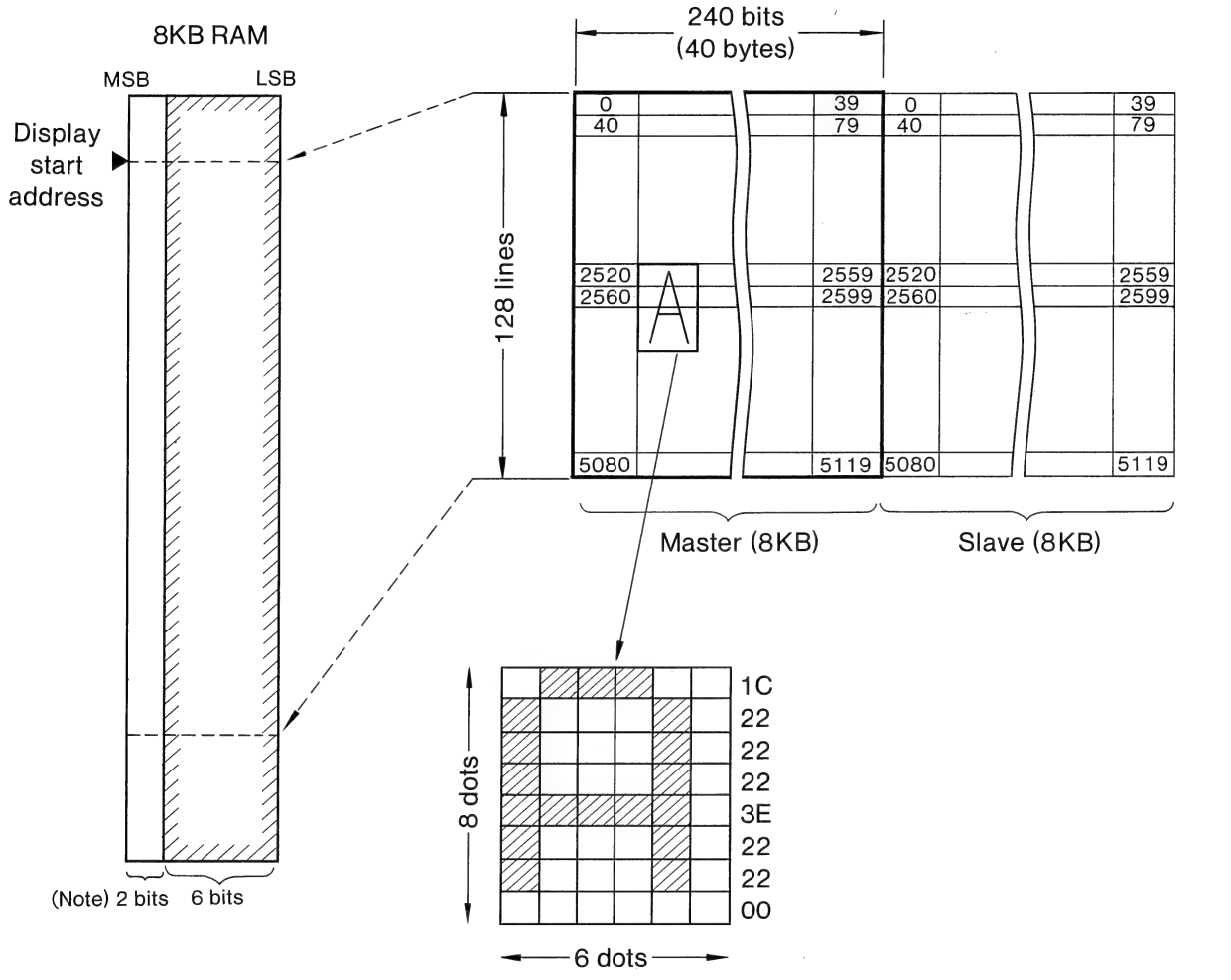


Figure 5-42. Abbreviated LCDC Control Program Flowchart

(5) Display Screen Memory Address

Since two HD61830s are used for the display screen memory address, this address is divided into left and right horizontal areas.

Both HD61830s are used in the graphics mode.



Note: The character face has a 6x8 dot configuration. Therefore, the two most significant bits are not used.

Figure 5-43. Display Screen Memory Configuration

5.9.3 LCD Unit

The operation of liquid crystal display module LM215P is explained in this section. The LCD and the driving circuit are discussed separately.

(1) LCD Panel

A liquid crystal is neither a liquid nor a solid. Its appearance, however, closely resembles that of a liquid. In terms of its electrical and optical characteristics, it is close to a crystal. Elements that use liquid crystals are referred to as liquid crystal display elements. LM215P uses TN (twisted nematic) type LCDs. The construction of the LCD panel is shown in Figure 5-44.

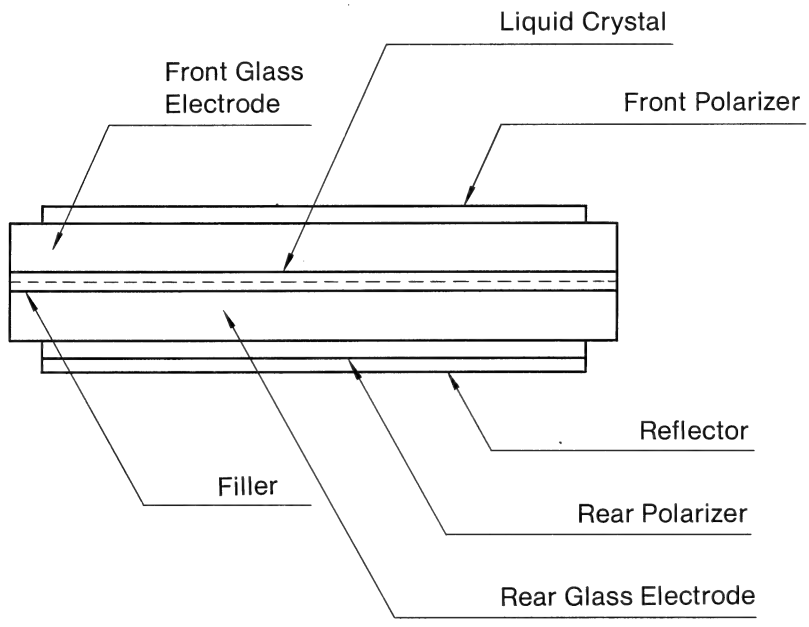


Figure 5-44. Construction of LCD Panel

An LCD acts as an electrical shutter that controls the passage of light. Light either passes or does not pass through the LCD, depending on the voltage that is applied to the LCD. The passage of light is controlled in order to display a character or a number. How the LCD operates is shown in Figure 5-45.

A liquid crystal display element is interposed between two polarizer plates. In order to optically twist light, the top and bottom plates are positioned so that their polarization axes are orthogonal to each other.

As shown in Figure 5-45(a), if no voltage is applied, light is dispersed and twisted by 90° by the liquid crystal molecules interposed between the top and bottom plates. This results in an optical movement of light by 90°, and light passes through.

As shown in Figure 5-45(b), if a voltage is applied, the liquid crystal appears as if it is frozen at the current position, and thus interrupts the passage of light.

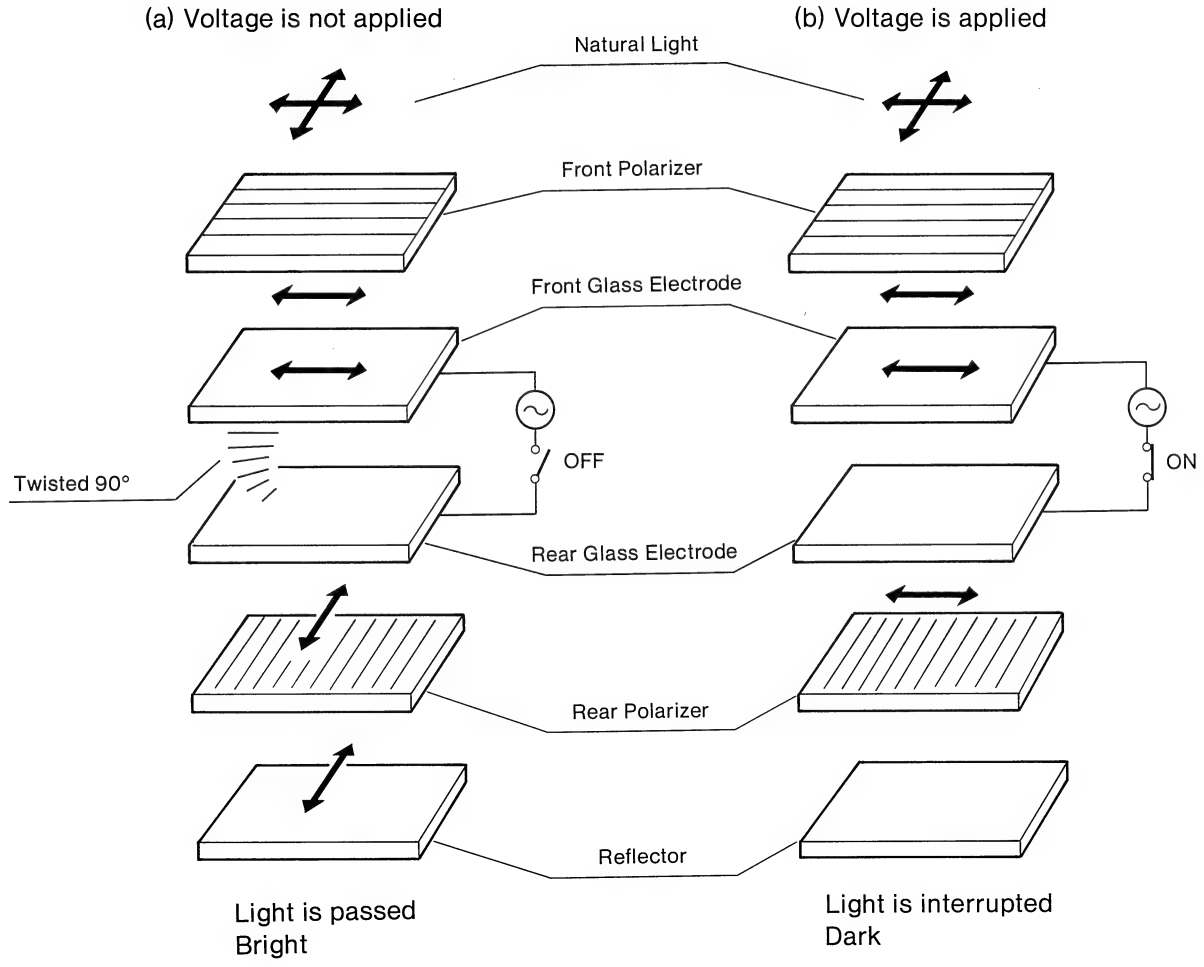


Figure 5-45. Operation Theory of LCD Board

The LCD used with the LM215 is comprised of electrodes arranged in a matrix configuration (128 commons, 960 segments).

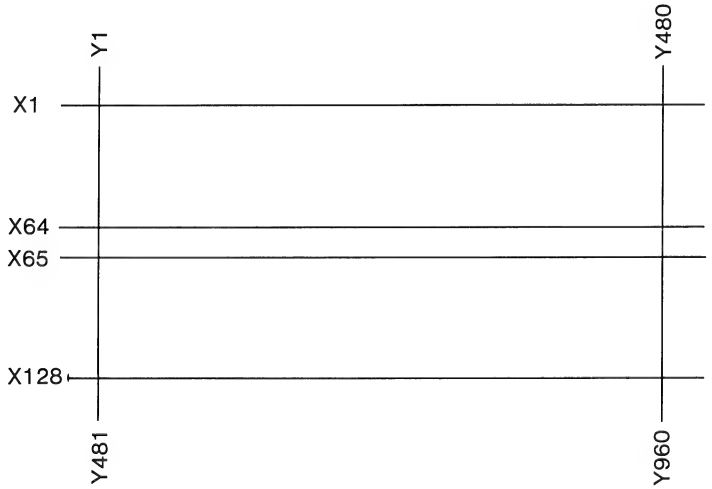


Figure 5-46. Matrix Configuration

Since the LCD is driven by a 1/64 time-sharing drive, the top and bottom 64 commons are driven by signals with the same timing.

The LCD view angle for a contrast (K) (luminosity of unlit segment/luminosity of lit segment) of at least 1.4 is approximately 20°.

The angle can be changed to horizontal or vertical orientation, or any position in between, by changing the LCD drive voltage (VDD-Vo).

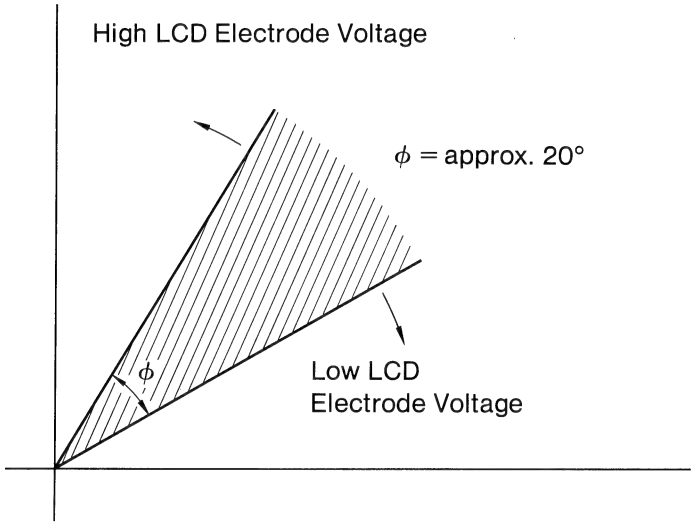


Figure 5-47. LCD View Angle

(2) Drive Circuit

(a) Circuit configuration

IC 3~14 (HD61100) are a segment driver IC, and ICs 1 and 2 (HD61103) are common driver ICs.

LM215P receives all signals necessary for LCD display operation, such as FLM, M and CL1, from an external source in accordance with the timing chart shown in Figure 5-41.

HD61103 has 64 driver outputs. One HD61103 each is used for the top (X1, X64) and the bottom (X65, X128) displays to enable parallel operation. The internal circuit configuration of HD61103 is shown in Figure 5-48.

HD611100 has 80 driver outputs, and drives 480 segment electrodes each for the top and bottom displays (total of 960 segment electrodes), using 12 ICs. The internal circuitry of the HD61100 is shown in Figure 5-49.

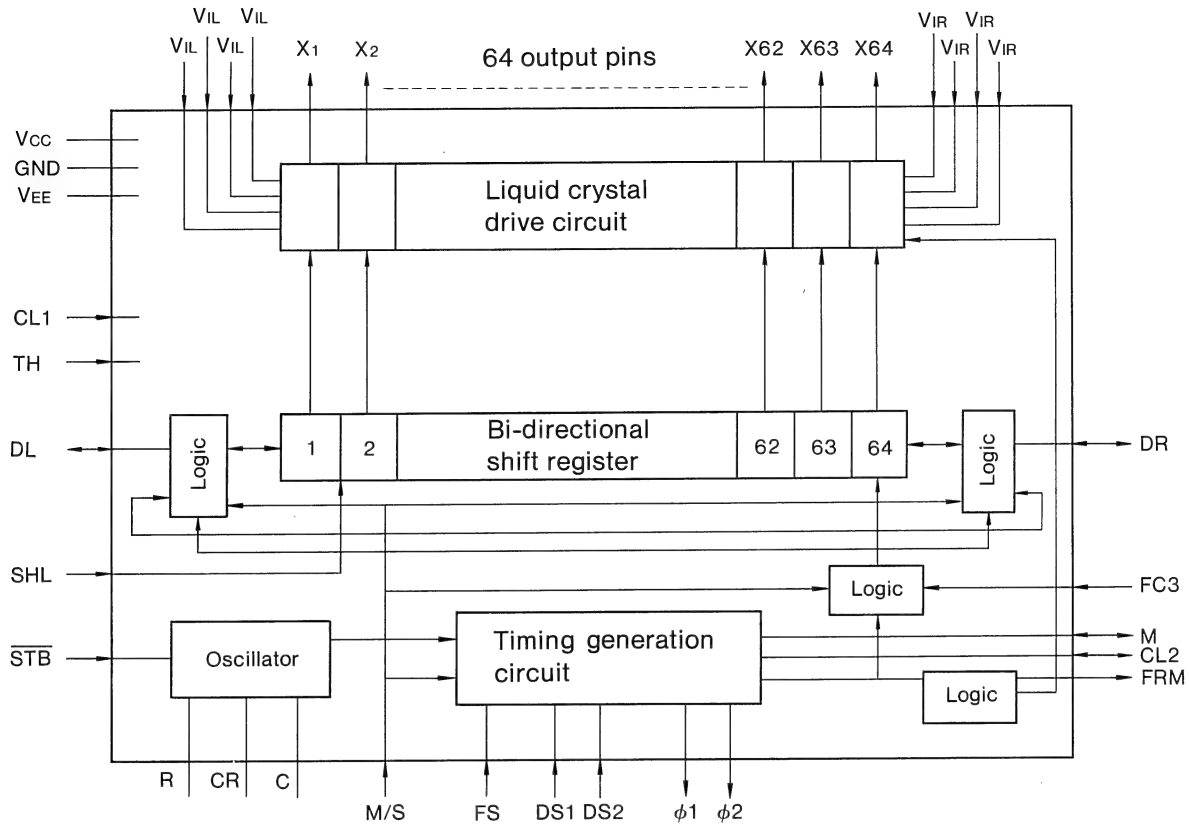


Figure 5-48. HD61103 Internal Circuitry

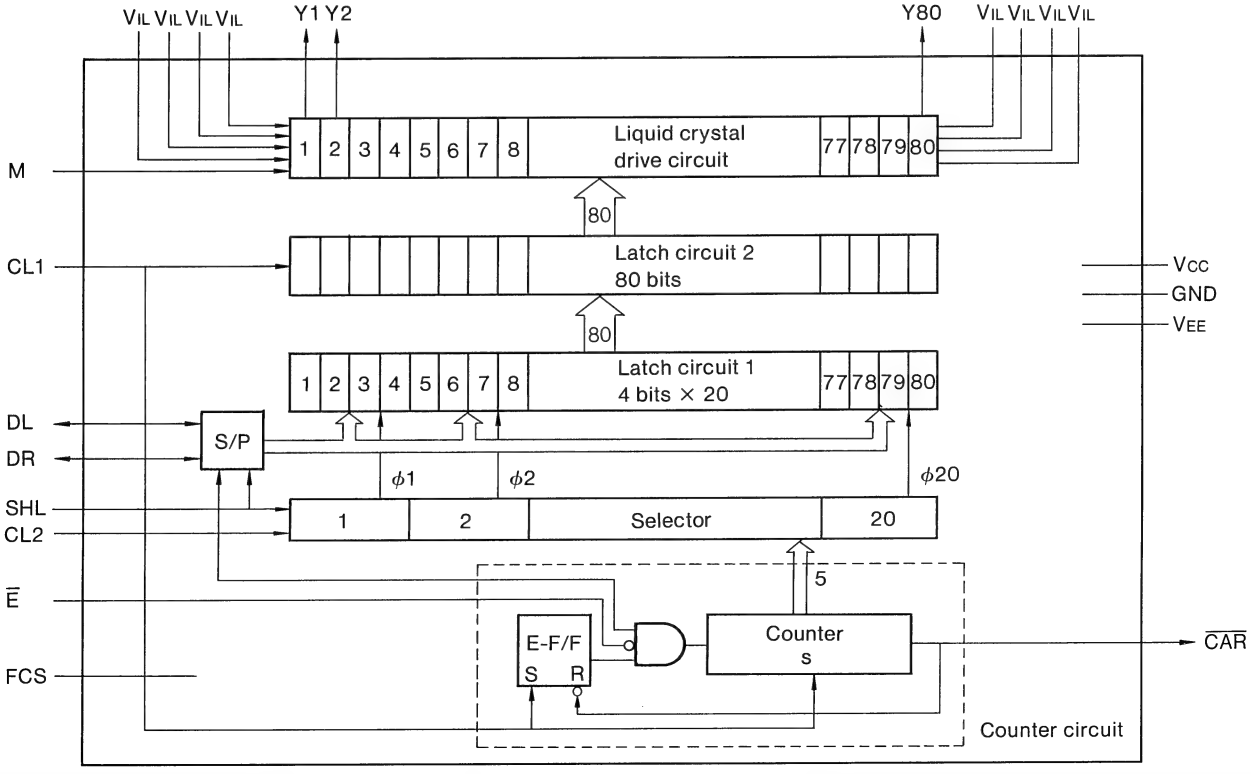


Figure 5-49. HD61100 Internal Circuitry

V_{DD}, V_{SS}, V_{EE}, V_O, etc., supply the power to the liquid crystals. V_{SS} is the ground (GRD) level.

R1 through R7 are split resistances used to create voltage V1 through V6 used for driving the liquid crystals. The output impedance of this power source is reduced by means of operational amplifier IC15 (HA17902).

(b) Timing signals
The external timing signals have the following functions:

FLM (First Line Marker): A signal used to determine the display scan frequency (normally set between 60 and 80 Hz). X1 and X65 are selected when FLM is input.

M (Multiplex): A control signal used to invert the liquid crystal drive waveform for each scan so as to effect an AC drive.

CL1 (Clock 1): A signal that is input every 240th clock and used for common data shifting and segment data latching.

CL2 (Clock 2): A clock signal used by HD61100 for fetching the segment data. The falling edge from HIGH to LOW is used as the timing for fetching the data.

D1-D4 (Data 1 through Data 4): Segment data signals.

(c) Operation
The commons successively select X1-X64 (X65-X128) by fetching the FLM signal into the internal shift register of HD61103 using the falling edge of HIGH to LOW. Therefore, FLM will be HIGH for a pulse width equivalent to 1/64 of the scan time, and will be LOW for the rest of the time. See Figure 5-51.

The 240 electrodes are divided into four segments for data transfer rate reasons. As shown in Figure 5-50, each LM215P is structured by combining four 64 ×240 dot-display blocks. The display data is synchronized with CL2, and data for 240 display dots is sent during one cycle of CL1. The data is read into register A, shown in Figure 5-49, using the falling edge from HIGH to LOW of CL2. The fetching sequence is as follows: The data first entered is read into the register corresponding to Y1, Y241, Y481, or Y721 (that is, to the leftmost segment of each of the four blocks), and the final data (240th data) is read into the register corresponding to Y240, Y480, Y720, or Y960. The data is latched from register A to register B using the falling edge from HIGH to LOW of CL1 as the timing. A liquid crystal being lit or not lit is determined by selecting or not selecting the common.

Segment Data	Common	
	Selected	Not Selected
1	Lit	Not lit
0	Not lit	Not lit

Table 5-10. Relationship between Segment Data and Common

(d) LCD Waveform

One example of a LCD waveform is shown in Figure 5-52. The bias coefficient that maximizes the voltage ratio between lit and unlit (that is, maximizes the contrast) is identified by a. With LM215P, a is set to 7.

	240	240
64	D1	D3
64	D2	D4

Figure 5-50. LCD Unit Screen Constitution

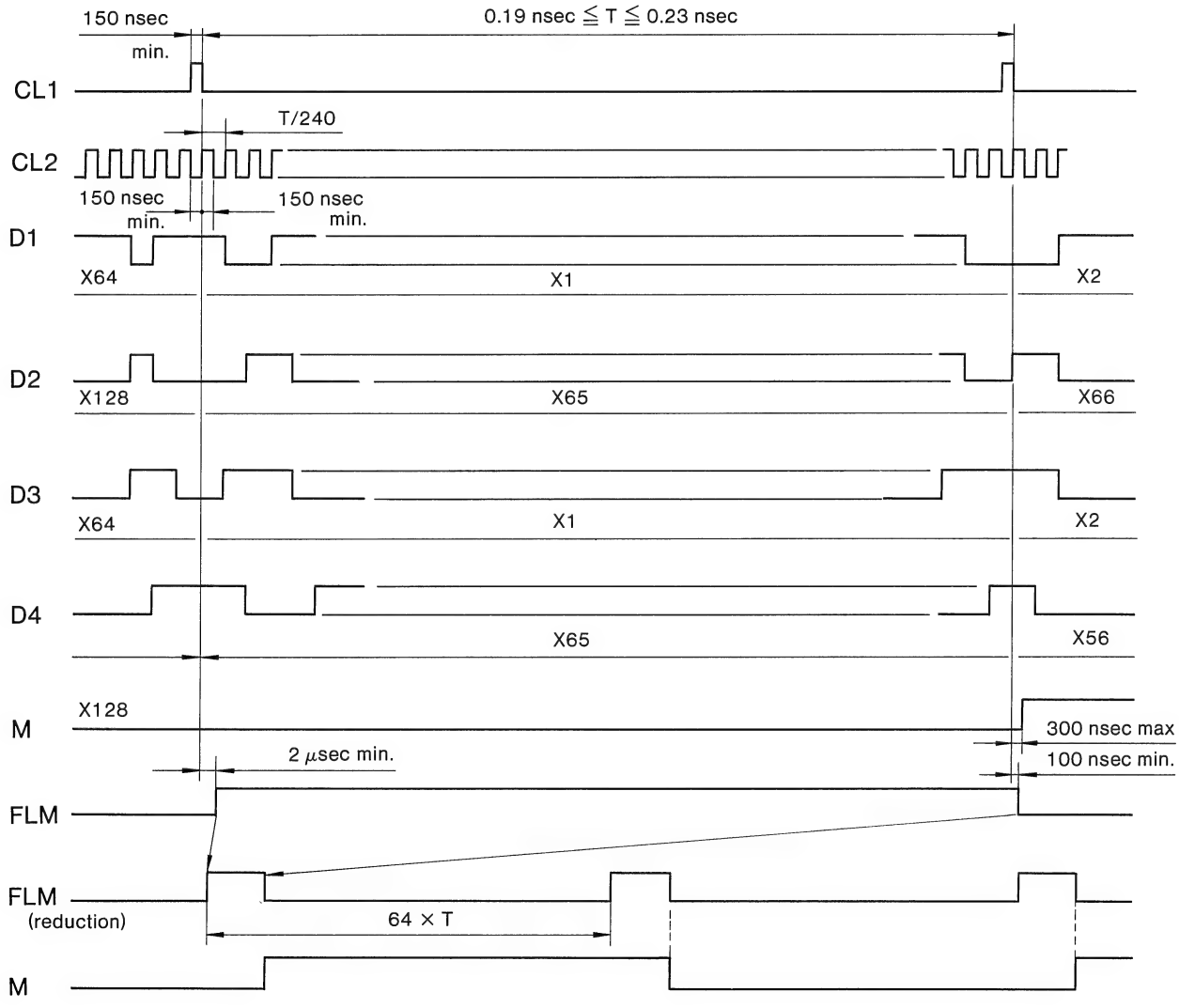


Figure 5-51. LCD Unit Interface Timing Chart

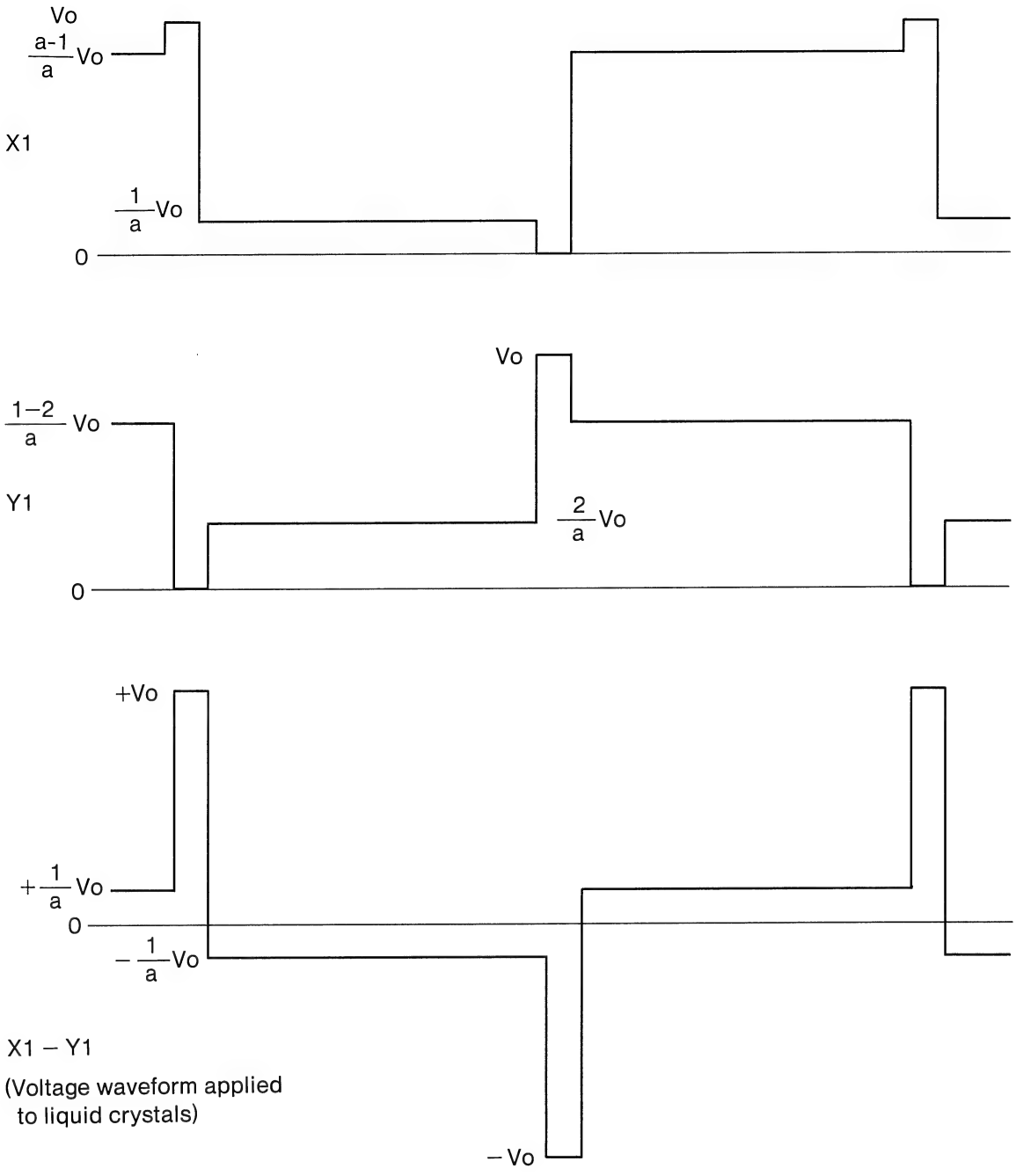


Figure 5-52. LCD Waveform

5.10 Serial Interface

5.10.1 Overview

The TANDY 600 is equipped with three serial interfaces: direct modem interface, acoustic coupler and RS232C interface. A block diagram of these interfaces is shown below:

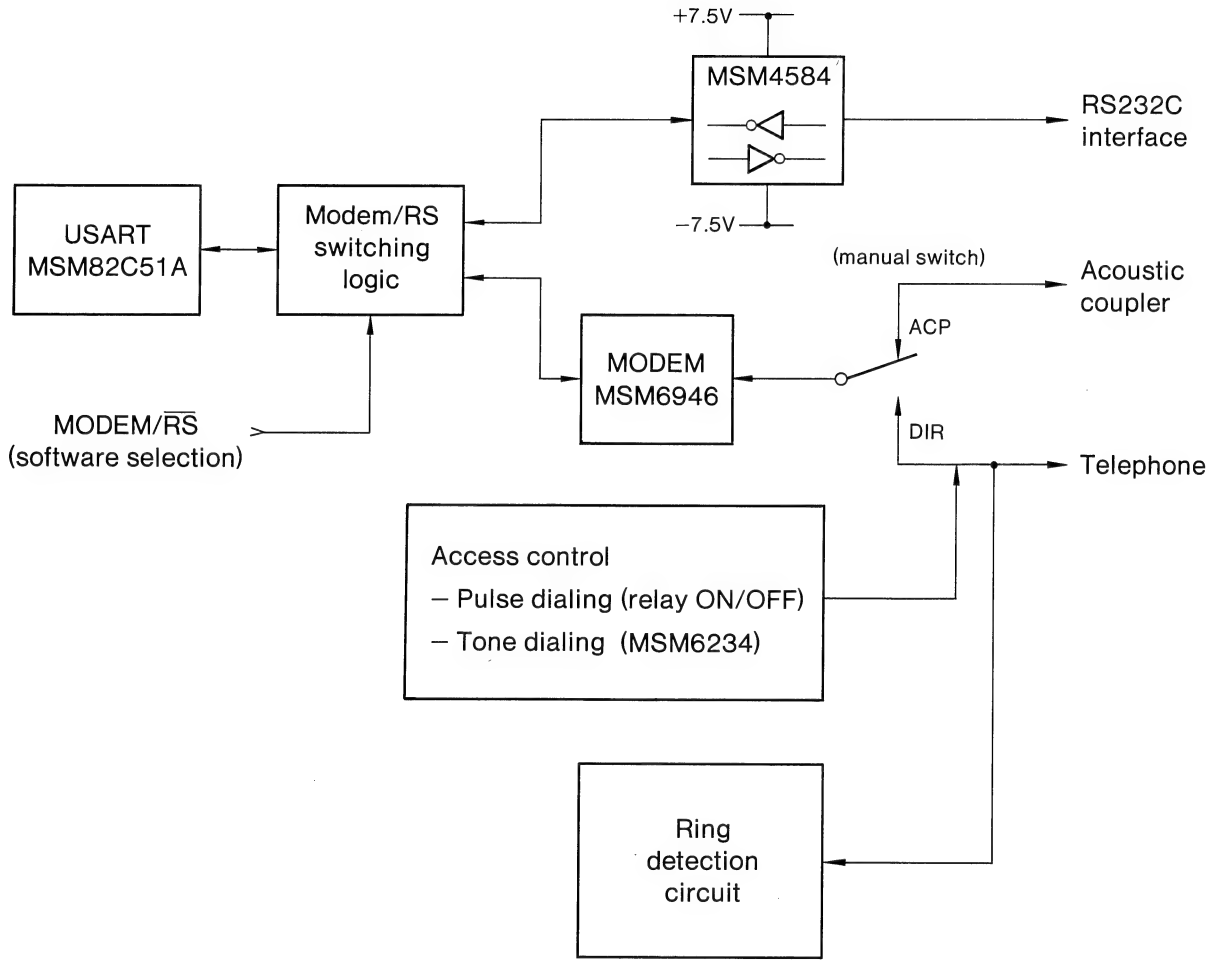


Figure 5-53. Serial Interface Block Diagram

5.10.2 USART (MSM82C51A)

(1) USART (MSM82C51A)

Serial data for the TANDY 600 is controlled by USART (MSM82C51A). The pin layout definitions are shown in Figure 5-54. Pins D0 through D7, C/$\overline{D}$, $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ are connections for the CPU interface signal lines that are used for sending commands to the 82C51A or for reading status.

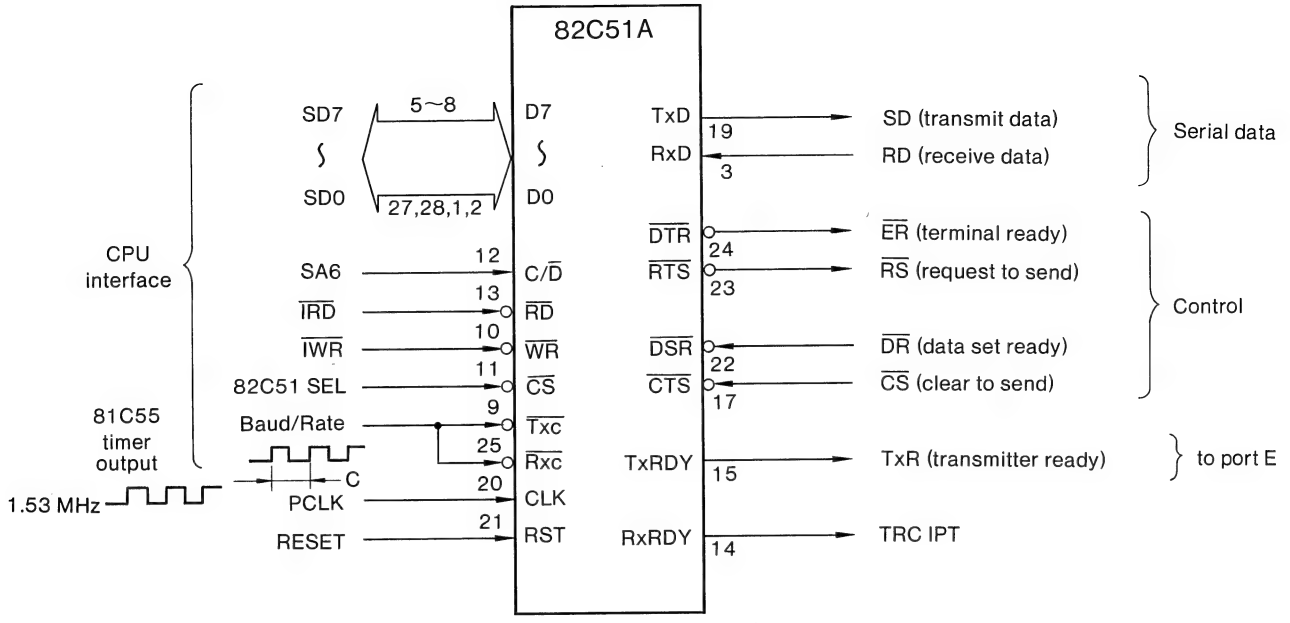
C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Function
0	0	1	0	Transmit data → D-Bus
0	1	0	0	Transmit data ← D-Bus
1	0	1	0	Status → D-Bus
1	1	0	0	Control ← D-Bus
X	1	1	0	D-Bus = High Z
X	X	X	1	D-Bus = High Z

Pressing the RESET switch sets the RESET terminal level to HIGH and resets 82C51.

A peripheral clock (PCLK) with a frequency of 1.53 MHz is input to the CLK terminal. $\overline{TxC}$ and $\overline{RxC}$ are clocks that determine the transmission rate of the 82C51A. The relationship between the baud rate and clock period is shown in the table in Figure 5-54. TxD and RxD are serial data transmission and reception lines, respectively.

$\overline{DTR}$, $\overline{RTS}$, $\overline{DSR}$ and $\overline{CTS}$ are control signal lines for RS232C or modem use. Since these lines are simply I/O ports for the 82C51A, they are all software-controlled. The TxR level is set to HIGH if the status register TxRDY is set to 1, if the $\overline{RTS}$ terminal level is LOW and if the $\overline{CTS}$ terminal level is LOW. Thus, TxR is a signal that notifies the CPU that the 82C51A is ready for transmission.

The RxRDY terminal level is set to HIGH when data reception by the 82C51 is completed.



Transmission rate (BPS)	Timer count value	t(μs)
110	873	568
300	320	208
600	160	104
1200	80	52
2400	40	26
4800	20	13
9600	10	6.5
19200	5	3.2

Note: For asynchronous mode with a baud rate factor of TANDY 600.

Figure 5-54. USART (82C51A) Pin Layout Definitions

5.10.3 MODEM/RS232C Switching Circuit

Since the serial port for the 82C51A has only one channel, the circuit shown in Figure 5-55 is multiplexed for modem and RS232C.

The MODEM/$\overline{RS}$ signal specifies whether the serial port is used as a modem or as the RS232C interface.

The MODEM/$\overline{RS}$ signal is controlled by the sixth bit of port D. The modem interface is selected when the MODEM/$\overline{RS}$ signal level is HIGH and the RS232C interface is selected when the MODEM/$\overline{RS}$ signal level is LOW.

The control signal for reception data and other inputs is processed by gate 05G (74HC157) and the control signal for transmission data and other outputs is processed by gate 03E, 03F or 02F.

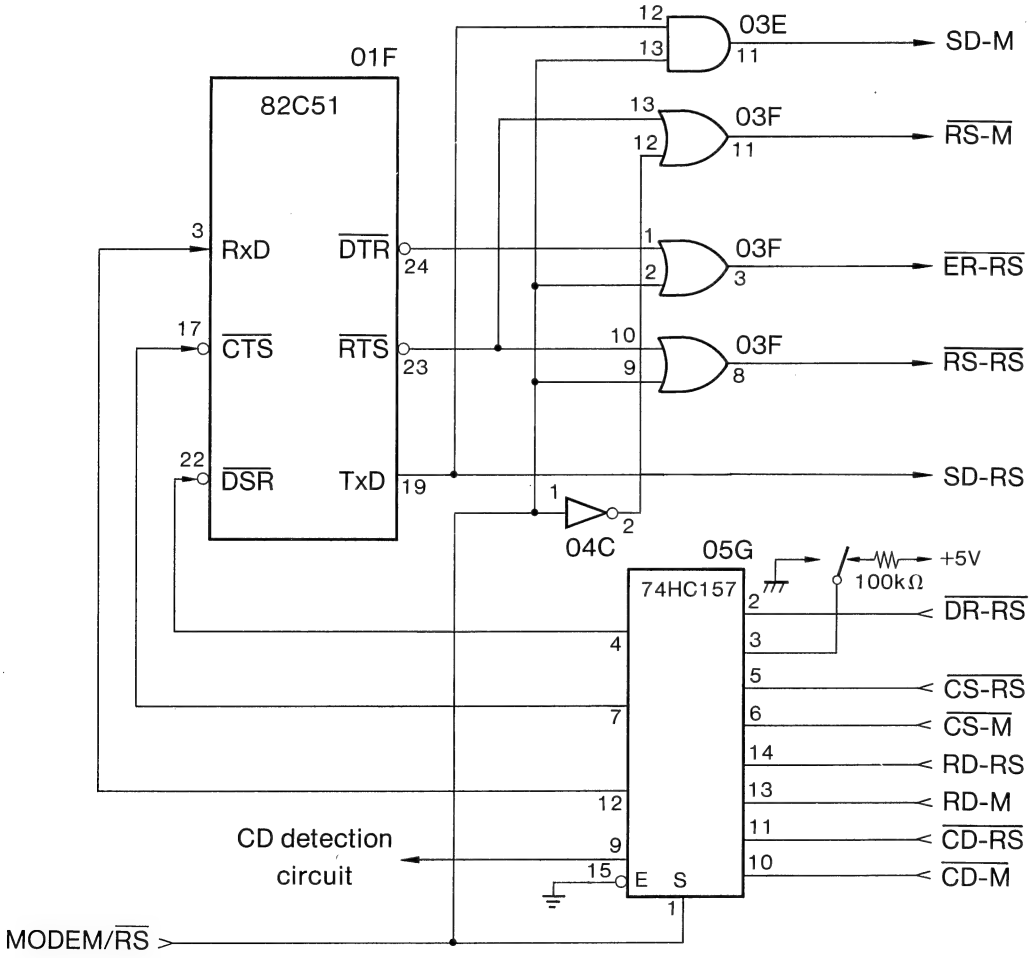
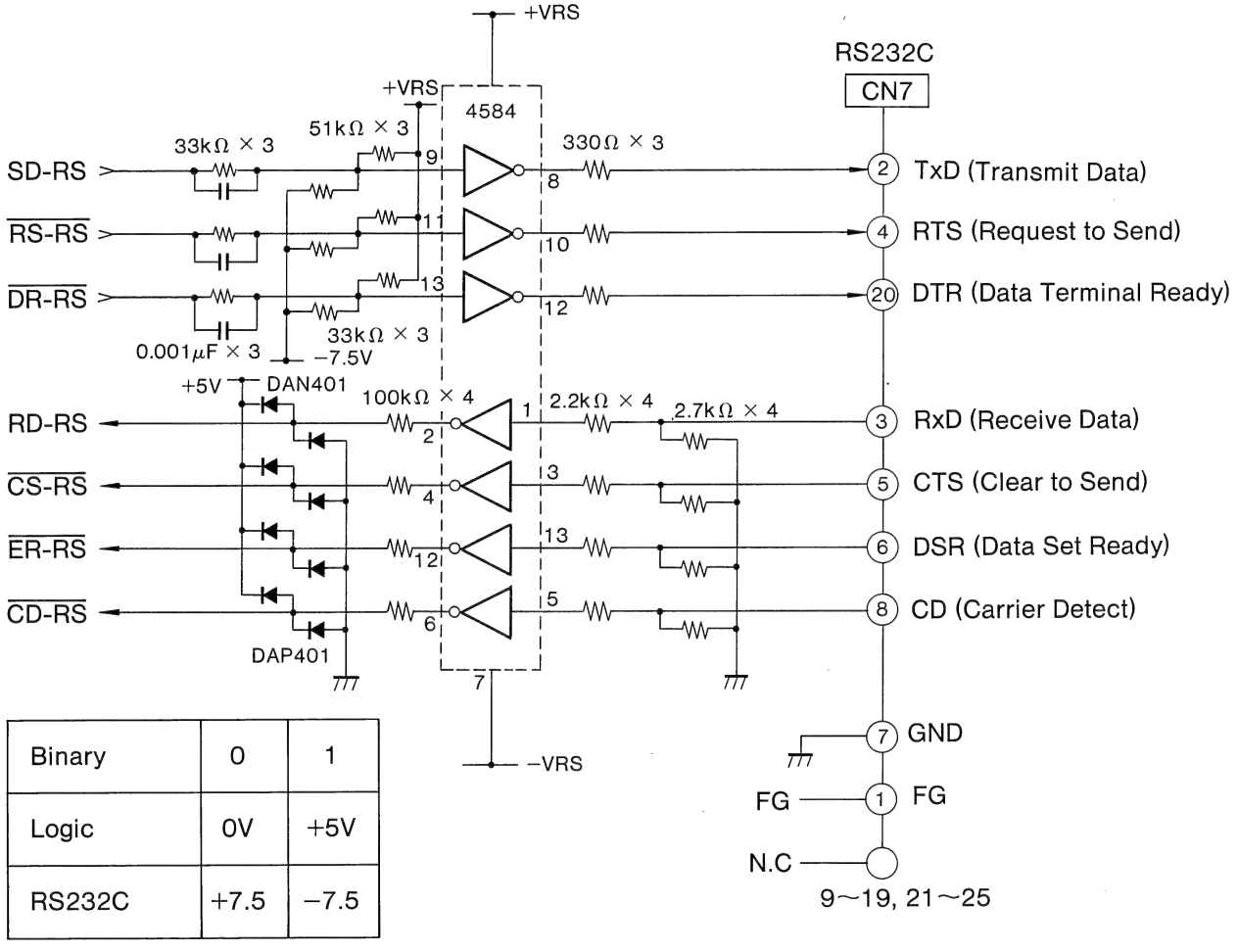


Figure 5-55. MODEM/RS232C Switching Circuit

5.10.4 RS232C Interface Circuit

Voltage level conversion for the TTL and RS232C levels is performed by this circuit.

TTL levels SD-RS, RS-RS and ER-RS are inverted and converted to a RS232C level by a Schmitt trigger-type inverter IC (MSM4584), and are then output to the RS232C connector (CN7). Signals from the RS232C connector (CN7) are converted to a TTL level by MSM4584 and diodes DAN401 and DAP401.



Binary	0	1
Logic	0V	+5V
RS232C	+7.5	−7.5

Figure 5-56. RS232C Interface Circuit

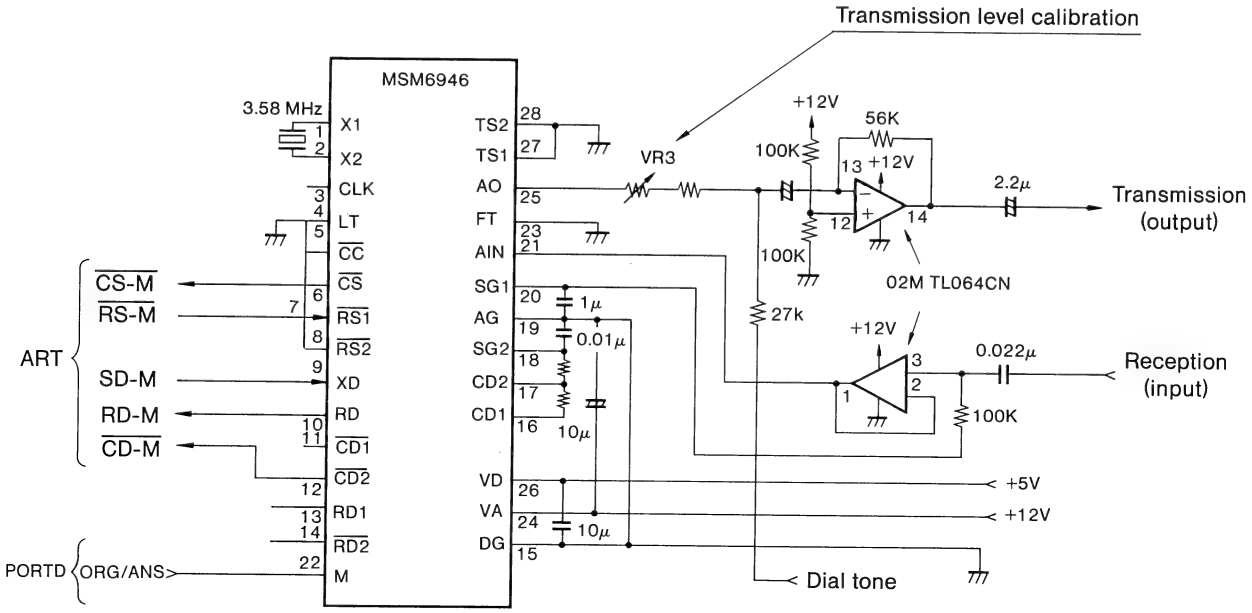
5.10.5 Modem

Modulation and demodulation are controlled by the MSM6946 (300bps FSK MODEM). The circuit diagram for the modem is shown in Figure 5-57. A carrier signal is output to terminal A0 when the $\overline{\text{RS-M}}$ signal level from USART becomes LOW. The $\overline{\text{CS}}$ terminal level is set to LOW 200ms after the $\overline{\text{RS-M}}$ signal level changes to LOW.

If transmission data is input to terminal XD, the carrier signal at terminal A0 is modulated. The modulated signal from terminal A0 passes through a transmission amplifier comprised of 02M (TL064) and is then output to an acoustic coupler or a telephone line.

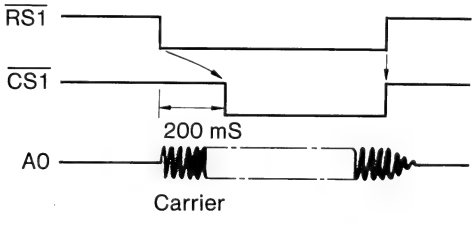
VR3 is a control for calibrating the transmission level; see section 4, Maintenance and Calibration, on how to perform the calibration. The reception carrier signal from an acoustic coupler or a telephone is input to terminal AIN of the MSM6946 after passing through the reception amplifier which is comprised of the 02M (TL064). While the carrier signal is being input to the AIN terminal, the $\overline{CD2}$ terminal level is set to LOW and demodulation is performed. The reception data is then output to terminal RD.

Terminal M, which is controlled by the seventh bit of port D, is used for selecting the originate mode or the answer mode (originate mode if the terminal M level is HIGH; answer mode if the level is LOW).



MODE	M	Bit	Frequency
Originate	High	Space Mark	1270 Hz ± 6 1070 Hz ± 6
Answer	Low	Space Mark	2225 Hz ± 6 2025 Hz ± 6

Relationship between RS1, CS1 and A0



Relationship between CD2 and AIN

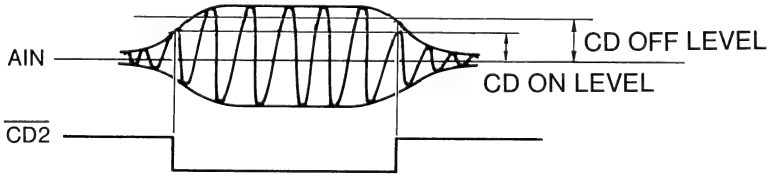


Figure 5-57. Modem Circuit Diagram and Timing Chart

5.10.6 Modem Connector Interface and Ring-Detection Circuit

The modem connector interface circuit is shown in Figure 5-58. Switch SW1 is used to switch between the acoustic coupler and the telephone line. The transmission signal and the reception signal are both connected to the line by means of the transformer. This is true for telephone lines as well. D36 and D37 are diodes used to absorb surge voltage in the telephone line.

With the acoustic coupler, the transmission output is input to the terminal SPEAKER after passing through an impedance matching resistance. The reception input signal is fed directly from terminal MIC to the reception amplifier. D3 and D4 are diodes that protect the reception amplifier. RL1, which is controlled by signal $\overline{\text{C-LP}}$, is used to disconnect the telephone and the line when a modem is being used.

RL2 is a relay used for dial pulse transmission. The relay turns signal $\overline{\text{C-DP}}$ on or off and controls the output of the dial pulse to the line. RL2 is in MAKE status when a modem is being used for communication.

The $\overline{\text{C-LP}}$ and $\overline{\text{C-DP}}$ signals are controlled by port D. 01H, an IC used for detecting calling signals (40-150V; 15.3-68 Hz) from the telephone office, uses an 02H (photocoupler) to create RP and $\overline{\text{RING DETECT}}$ signals.

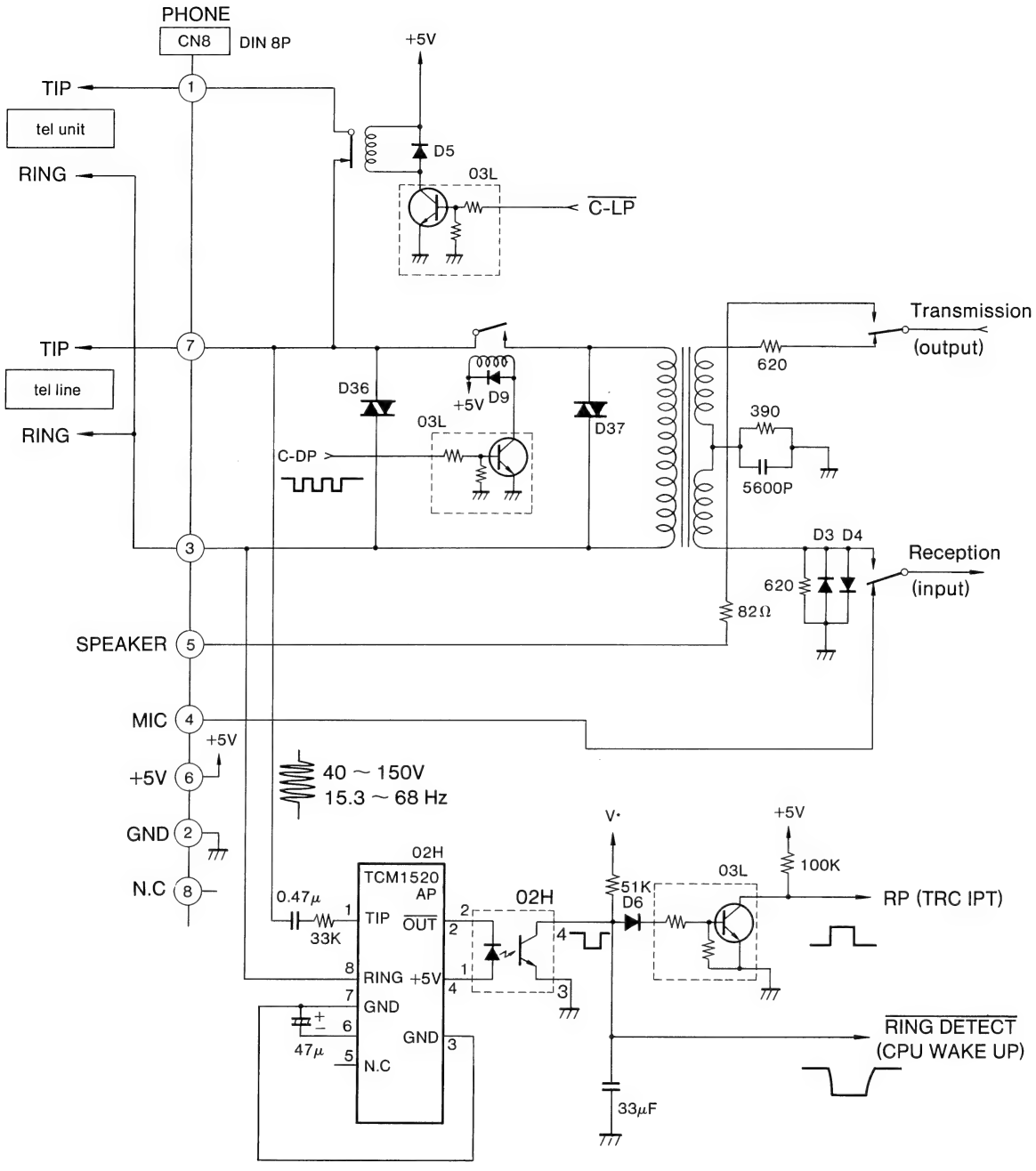


Figure 5-58. Modem Connector Interface and Ring-Detection Circuit

5.10.7 Serial Interface Interrupt

The circuit that controls interrupts from a serial interface is shown in Figure 5-59. There are three reasons for a serial interface to issue an interrupt:

- Change in CD signal level (rising edge or falling edge)
- Reception of a telephone access signal (ring pulse)
- Completion of data reception by 82C51 (RxRDY signal)

A logical OR is taken and the result is used as the level 2 interrupt.

An interrupt signal is input to clock terminal RxR F/F, RP F/F, CD ON F/F or CD off F/F (74HC74). D input is set to HIGH using the rising edge as the timing.

A logical OR is taken of the outputs from each F/F at gates 03C, 03F and 05C.
The final output is used as the $\overline{\text{TRC IPT}}$ signal.

$\overline{\text{TRC IPT CLEAR}}$ signal is used in decoding the address of the TRC IMP CLEAR command. When the TRC IPT CLEAR signal level becomes LOW, each F/F is reset and the interrupt is cleared.

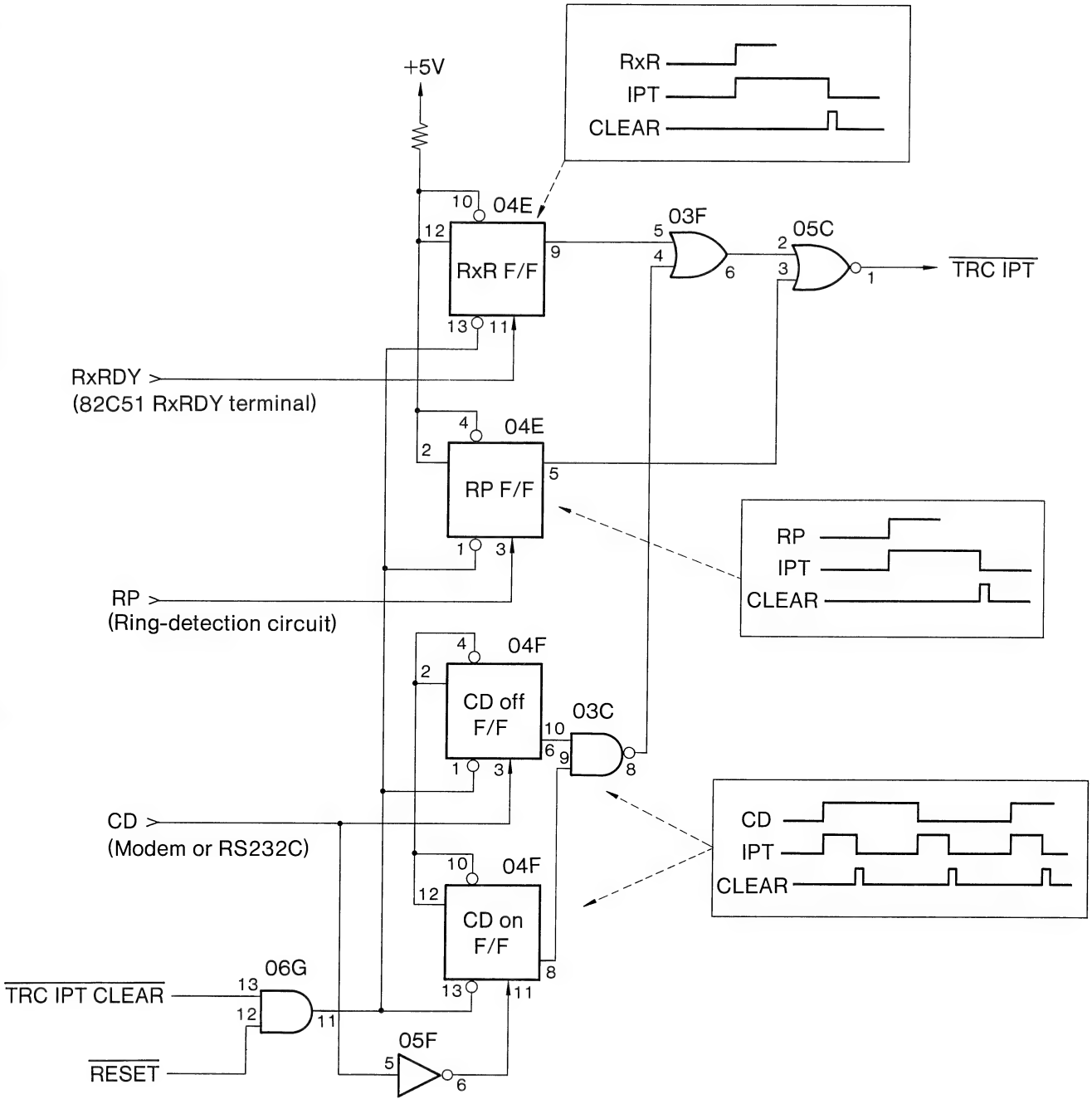


Figure 5-59. Serial Interface Interrupt Control

5.10.8 Auto-Dialing

Auto-dialing means that the TANDY 600 automatically performs the dialing operation with the telephone disconnected from the telephone line, as opposed to manual dialing where a telephone instrument is used.

There are two types of auto-dialing:

- Pulse dialing
- Tone dialing

The auto-dialing circuit diagram and the timing chart are shown in Figure 5-60.

(1) Pulse Dialing
In pulse dialing, the dialed number is specified by the number of pulses. Dial pulses are generated by switching RL2 (relay) on and off by controlling the $\overline{\text{C-DP}}$ signal. The timing chart for dial pulses is shown in Figure 5-60.

(2) Tone Dialing
In tone dialing, the dialed number is specified by combining two different frequencies. The TANDY 600 uses the MSM6234 to generate a dial tone. Terminals $\overline{\text{R1}}$ through $\overline{\text{R4}}$ are used to output the high frequency tone, while the low frequency tone is output from terminals $\overline{\text{C1}}$ through $\overline{\text{C4}}$. The specified dial tone is emitted from terminal TO when the TD terminal level becomes HIGH.

The relationship between a dialed number and the tone frequencies, and the tone dial timing chart, is shown in Figure 5-60.

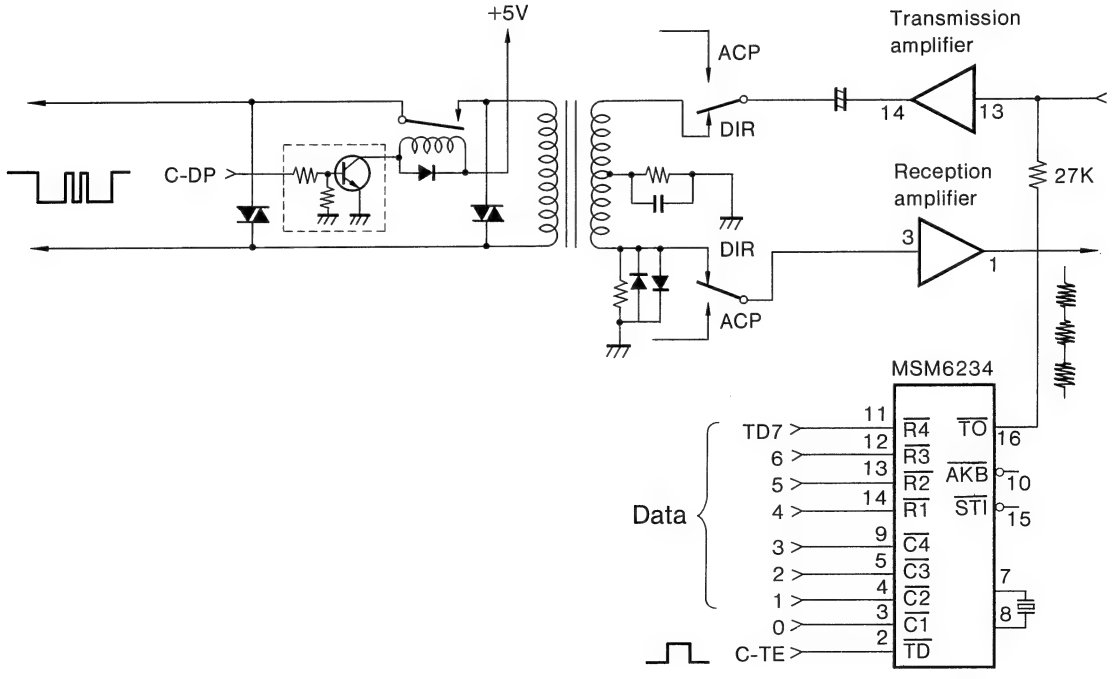


Figure 5-60. Auto-Dialing Circuit Diagram and Timing Chart

5.11 Buzzer Control

There are two ways to sound the buzzer: a specific frequency generated by PB7 and 81C55 timer out.

5.11.1 Output Signal from PB7 on 81C55

When PB6 is high, PB7 is synchronized with the sound frequency to alternate the high level and low level. As a result, the output from 11A-3 enters 07G-10 and then is output from 07G-8 to sound the buzzer. (See Figure. 5-61)

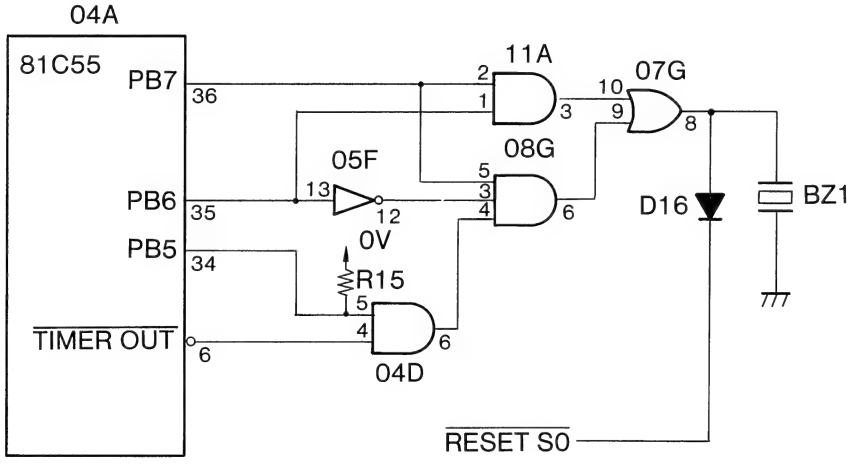
5.11.2 81C55 Timer Output

When PB5 and PB7 are high, and PB6 is low, the square wave output from the 81C55 timer flows from 04D-6 to 08G-4, from 08G-6 to 07G-9, and then is output from 07G-8 to sound the buzzer. Since the sound pitch coincides with frequency, a desired sounding frequency can be calculated as follows:

$$\text{Frequency (Hz)} = \frac{1.53 \times 10^6}{n}$$

Where n: Count value of 81C55 timer

(See Figure 5-61.)



(See Figure 5-66)

Figure 5-61. Buzzer Control Diagram

5.12 Real Time Clock (RTC)

The TANDY 600 includes real time clock built in the LSI (HD146818). The LSI, its peripheral circuitry and functions are discussed in this section.

5.12.1 Overview of TANDY 600 Real Time Clock (RTC) Functions

(1) The RTC's internal current time is used by the system.

(2) An interrupt request is issued when the current time matches the alarm time set for the RTC.

(3) If the current time matches the set alarm time while power to the TANDY 600 is off, power to the TANDY 600 can be automatically restored and the program restarts processing.

(4) A periodic interrupt or an update interrupt that is issued at regular intervals can be used as the timing for blinking the cursor, performing system KB scans, etc.

(5) Since the RTC is backed up by a battery located on the OPMP board, its data is not lost when power to the TANDY 600 is turned off. However, the battery backup is not activated if the RAM backup switch is set to OFF.

5.12.2 RTC Address Map

The RTC (HD146818) includes a built-in 64-byte CMOS RAM. DVA is assigned to address C000 through C03F. The HD146818 is controlled by reading from or writing into the first 14 bytes of the RAM area.

See Appendix C.4 for details on how the HD146818 is controlled.

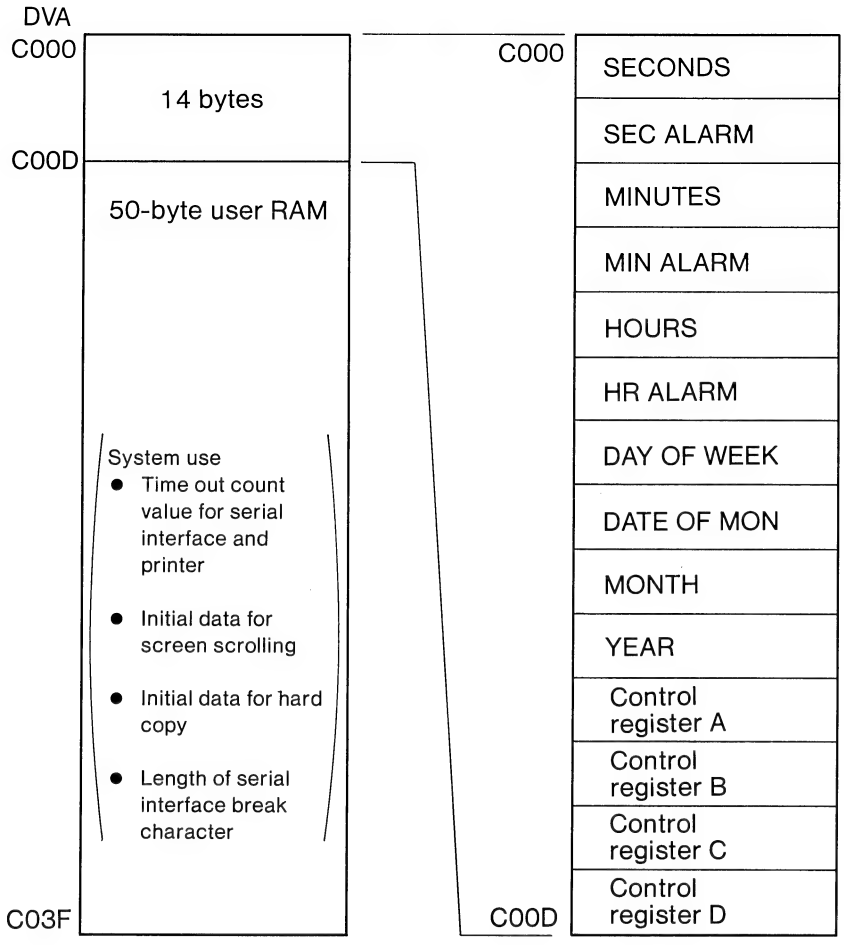


Figure 5-62. RTC Address Map

5.12.3 Clock Function (Update Interrupt)

The HD146818 is equipped with a clock that keeps the current time. The current time is determined by reading the RAM located in the RTC. This clock is updated every second. Each time an update is completed, the $\overline{IRQ}$ terminal level is set to LOW (update interrupt). The update interrupt can be mask-controlled by means of the UIE bit of control register B.

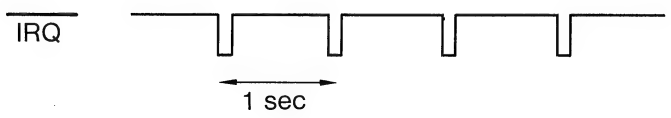


Figure 5-63. IRQ Signal Waveform

5.12.4 Alarm Function

When a comparison by the HD146818 of the current time with the set alarm time produces a match during an update cycle, the $\overline{IRQ}$ terminal level is set to LOW and an update interrupt is issued. The update interrupt can be mask-controlled by means of the AIE bit of control register B.

5.12.5 Periodic Interrupt

By setting a value in RS0 through RS3 of the HD146818 control register A, the $\overline{IRQ}$ terminal level can be set to LOW periodically so that periodic interrupts are issued. Such interrupts are used for system timing to control cursor blinking and KB scanning, as a general purpose software timer, etc. The periodic interrupt can be mask-controlled by means of the PIE bit of control register B.

RS 3 2 1 0	Period	RS 3 2 1 0	Period
0 0 0 0	————	1 0 0 0	3.90625 ms
0 0 0 1	3.90625 ms	1 0 0 1	7.8125 ms
0 0 1 0	7.8125 ms	1 0 1 0	15.625 ms
0 0 1 1	122.070 μs	1 0 1 1	31.25 ms
0 1 0 0	244.141 μs	1 1 0 0	62.5 ms
0 1 0 1	488.281 μs	1 1 0 1	125 ms
0 1 1 0	976.562 μs	1 1 1 0	250 ms
0 1 1 1	1.53125 ms	1 1 1 1	500 ms

5.12.6 HD146818 and Its Peripheral Circuitry

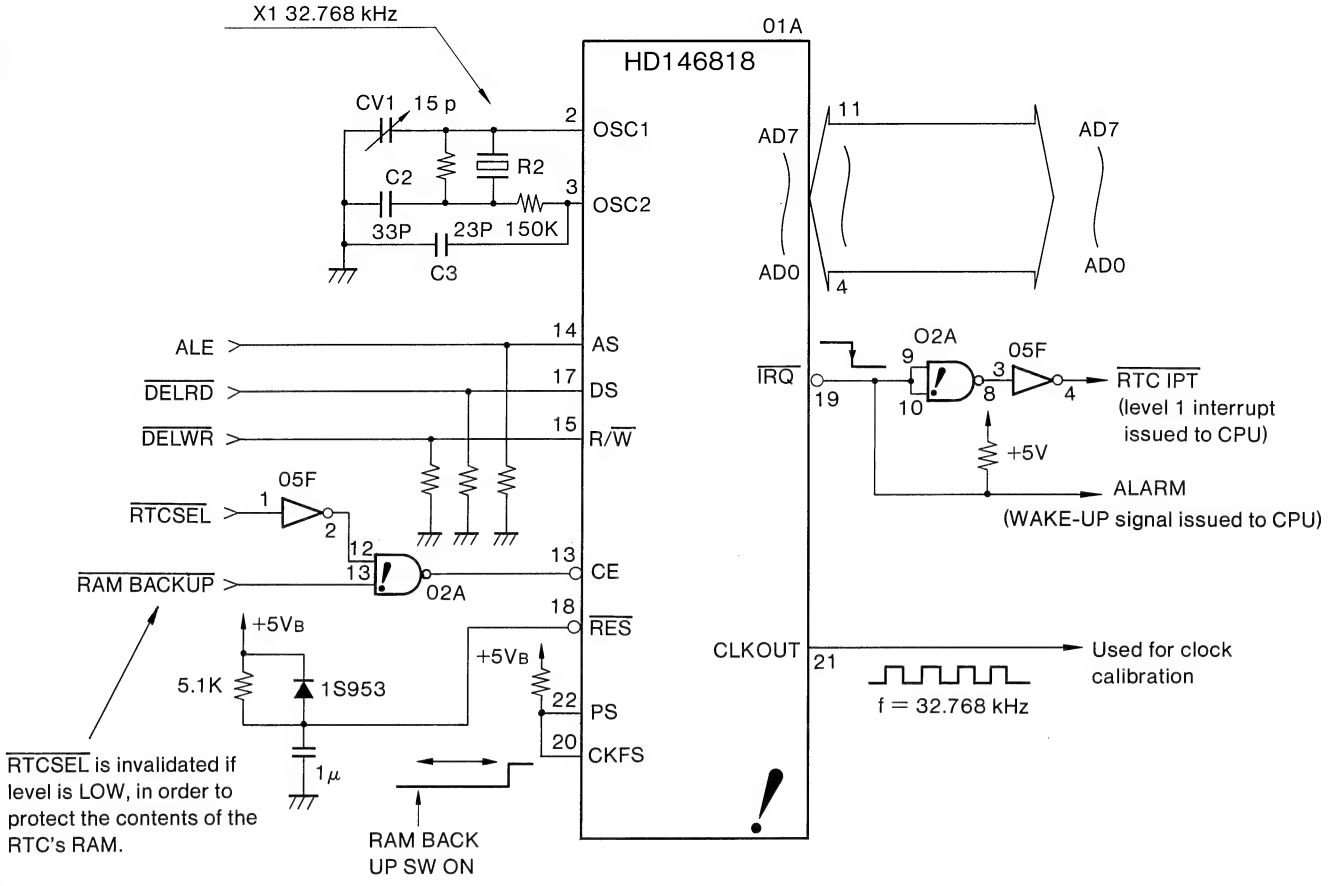
A battery on the OPMP board supplies power to the RTC block when the main power is off. The HD146818, its peripheral circuitry and a timing chart are shown in Figure 5-65. A quartz oscillator with a frequency of 32.768 kHz is connected to terminals OSC1 and OSC2 of the HD146818. The RTC operates using this frequency for reference.

A RESET signal is created by the POWER ON RESET circuit comprised of R3, C3 and D3. When the RAM BACK UP SW is switched from OFF to ON, this signal is input to terminal $\overline{RES}$ and HD146818 is reset.

The $\overline{IRQ}$ terminal level is set to LOW whenever one of the three HD146818 interrupts (periodic interrupt, update interrupt or alarm interrupt) is issued.

Terminal $\overline{IRQ}$ is also used as the level 1 (number two priority) CPU interrupt.

If the $\overline{IRQ}$ terminal level is LOW (alarm interrupt issued) while power to the TANDY 600 is off, power is restored and the CPU restarts the processing according to the program.



Note: The backup battery supplies +5VB to the ICs marked with the ! symbol.

Figure 5-64. HD146818 Peripheral Circuitry

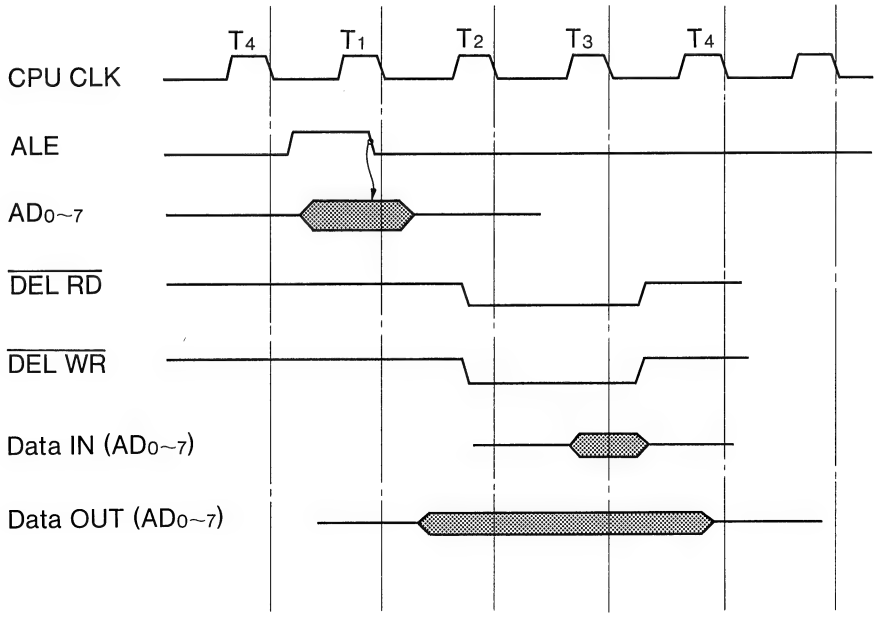


Figure 5-65. HD146818 Timing Chart

5.13 Power Supply Control and DC/DC Converter

5.13.1 Automatic Power Supply ON/OFF Function

Power to the unit can be turned on and off either automatically or manually.
The power ON/OFF modes are described below:

(1) ON/OFF using POWER switch
Power supply is controlled by the user by pressing the POWER switch on the keyboard.

(2) Power ON invoked over telephone line
Power to the unit is automatically turned on when a ring pulse is detected on the telephone line.

(3) Power ON invoked by RTC alarm
Power is automatically turned on when the alarm time set in advance in the RTC is reached.

(4) Auto power OFF
Power is automatically turned off to protect the battery when the unit is not used for 10 minutes.

5.13.2 Power Supply Control Circuit

The power supply control circuit is shown in Figure 5-66, while the power ON/OFF sequence timing chart is shown in Figure 5-67. Power is always supplied to the power supply control circuit regardless of the power ON/OFF setting.

F/F for 02T is a flip-flop switch that maintains the power ON/OFF status. If the F/F is set, RL4 is in make status and the power supply is on. If the F/F is reset, RL4 is in break status and the power is off.

When the POWER switch is pressed, the level of 02S-pin 4 changes from HIGH to LOW. The F/F setting for 02T is also reversed, thus reversing the power supply status.

When a telephone ring pulse is detected or when an RTC alarm interrupt is issued, the CPU WAKE-UP signal level becomes HIGH. F/F for 02T is set and power is turned ON.

F/F of 02T is reset and power is turned OFF when the $\overline{\text{AUTO POWER OFF}}$ signal level from port E becomes LOW. The TRAP signal level becomes HIGH when the power supply voltage drops to a prescribed level or when the user turns off the power by pressing the POWER switch. The TRAP signal is connected to pin NMI of the CPU.

When an NMI is issued, the CPU saves the current contents of registers and prepares for power disconnect.

The $\overline{\text{RAM BACKUP}}$ signal protects the contents of the RAM by closing all RAM gates while the power is off.

The $\overline{\text{LOWB}}$ signal lights the LED to notify the user of a drop in the power supply voltage.

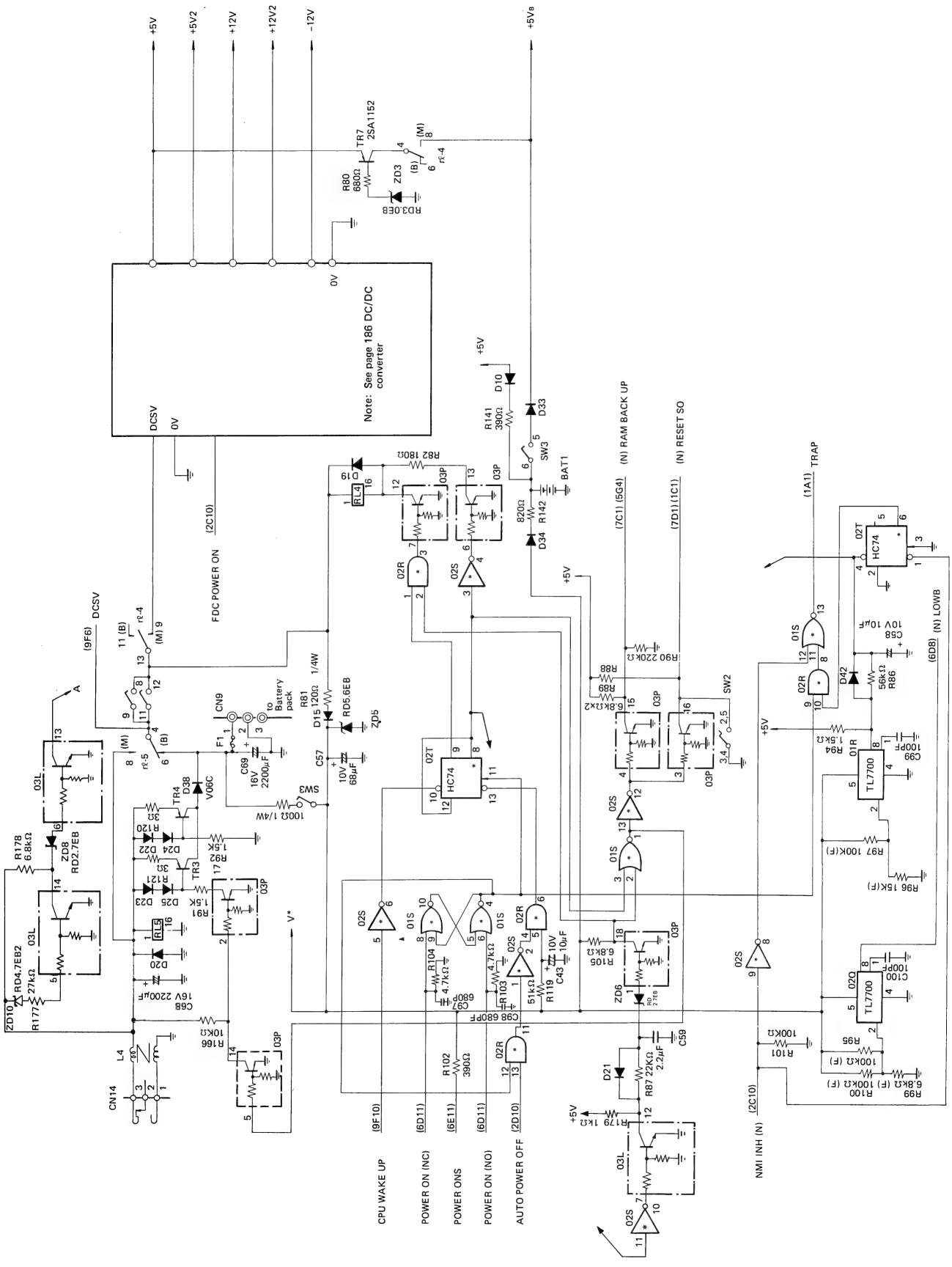


Figure 5-66. Power Supply Control Circuit Diagram

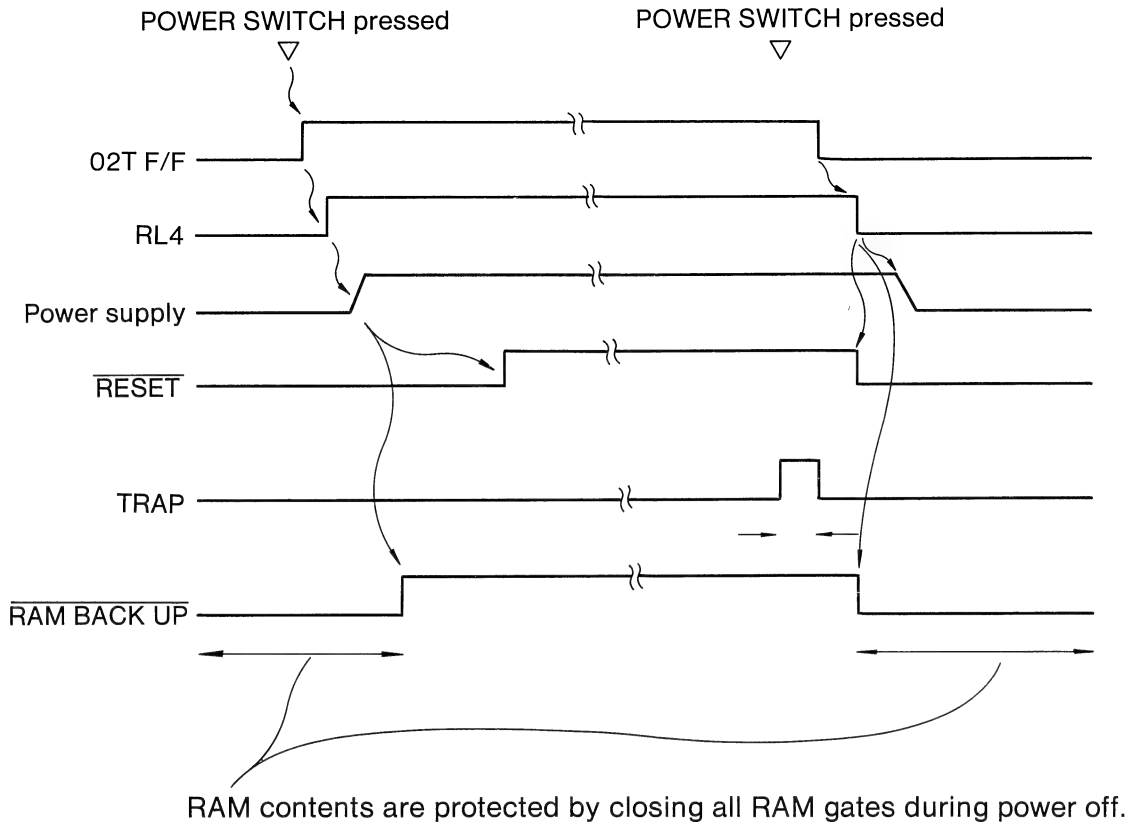


Figure 5-67. Power ON/OFF Sequence Timing Chart

5.13.3 DC/DC Converter

TR6 is a transistor with a controlled pulse width that feeds back a +5V1 output voltage. TLA-1 is a pulse transformer that is driven at a frequency of 30-40 kHz by TR6. Various required voltages are output from the secondary side of TLA-1.

IC1 consists of a reference voltage block, differential amplifier, generator and driver. Pin 2 on IC1 is connected to the +5V1 to detect its change by amplifying a difference between the voltage and a reference voltage. The detection signal (pin 4 on IC1) is transmitted to the generator by an unstabilized multivibrator to change the pulse width, thereby driving TR1 through the driver to control TR6.

The power supply to IC1 is stabilized by TR5, R122 and ZD4 and then supplied to pin 14 on IC1. +5V1 is stabilized by IC1, but +12V2 is stabilized separately by TR8, TR9 and ZD9.

RL3 is tripped when the FDC POWER ON signal level becomes HIGH, and power (+5V2, −5V2) for the FDD block is output.

Since the input voltage (DC 5V) is different between the AC adapter and the battery, the source power supply for the +12V2 power supply is selected by means of RL5.

A circuit diagram and waveforms are shown in Figures 5-68 and 5-69.

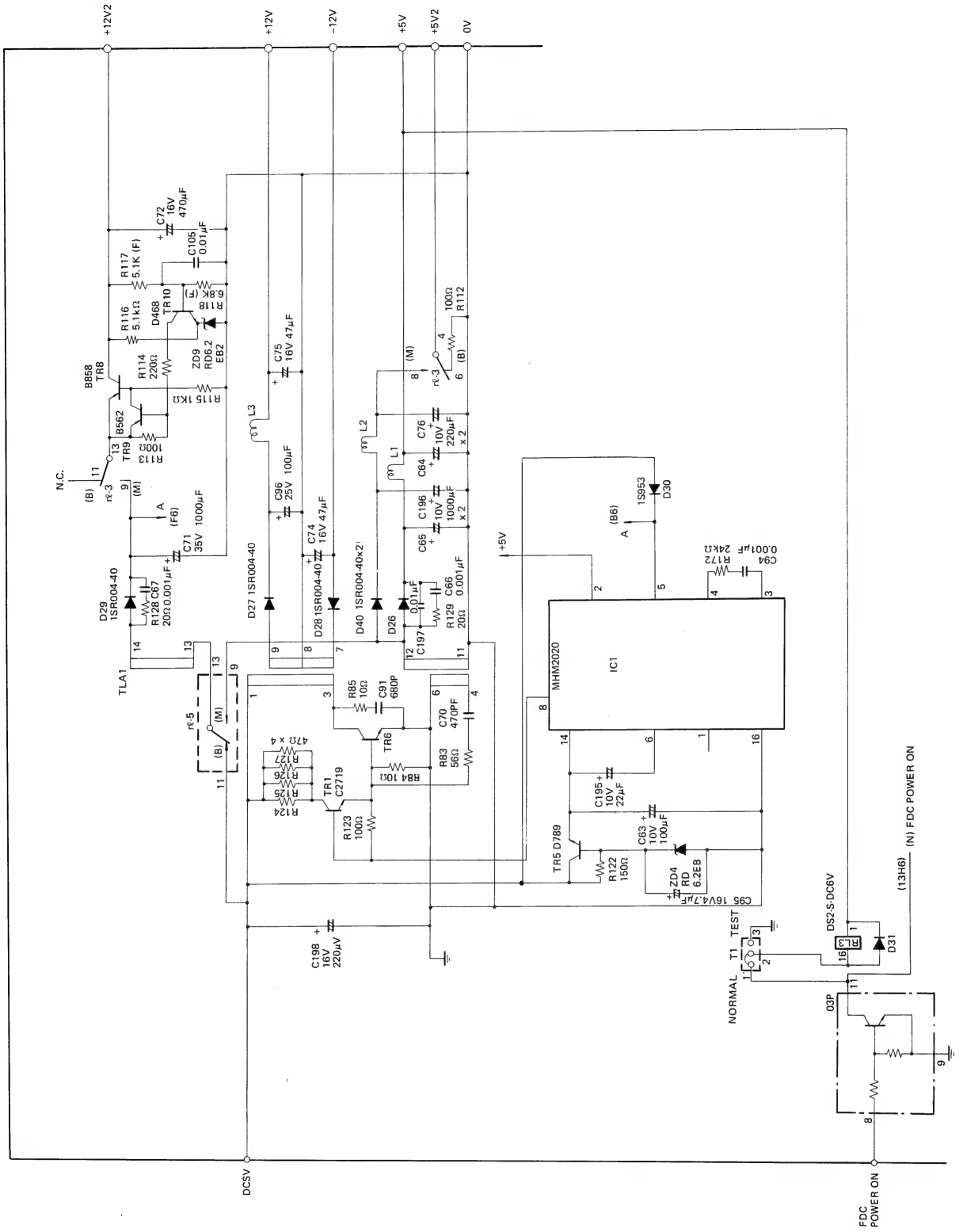


Figure 5-68. DC/DC Converter Circuit Diagram

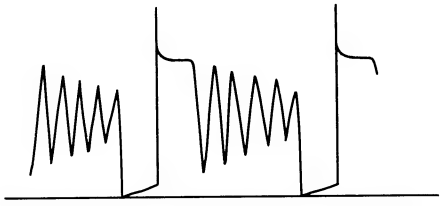


Figure 5-69. Vc Waveform of TR6

5.13.4 Power Supply Types

Six power supplies are used with the unit. They include V* which is always output, and +5V2, +12V2, etc., which are output when the FDD is being accessed.
The usage and the conditions under which the six power supplies are output are shown below:

Main power supply	ON	OFF	OFF	ON	Purpose
Backup SW	ON	ON	OFF	ON	
FDC POWER	OFF	–	–	ON	
+5V1	○	X	X	○	Normal +5V
+5V2	X	X	X	○	+5V for FDD block
+12V1	○	X	X	○	Normal +12V
+12V2	X	X	X	○	+12V for FDD block
-12V1	○	X	X	○	Normal −12V
V*	○	○	○	○	4.8V, continuously supplied
+5VB	○	○	X	○	RAM backup power supply

○: Output
X: Not output

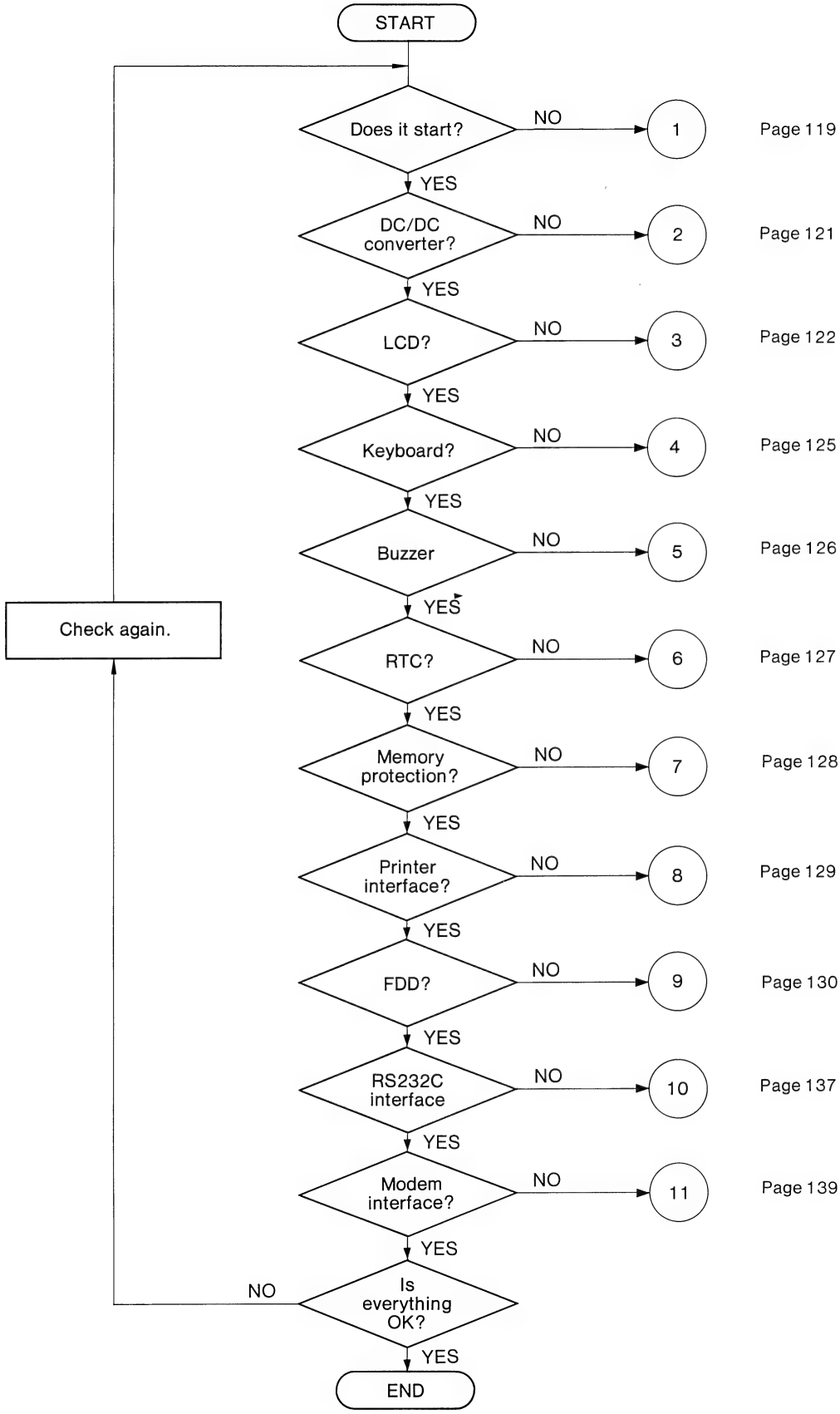
Table 5-11. Power Supply Usage

Section 6
TROUBLESHOOTING

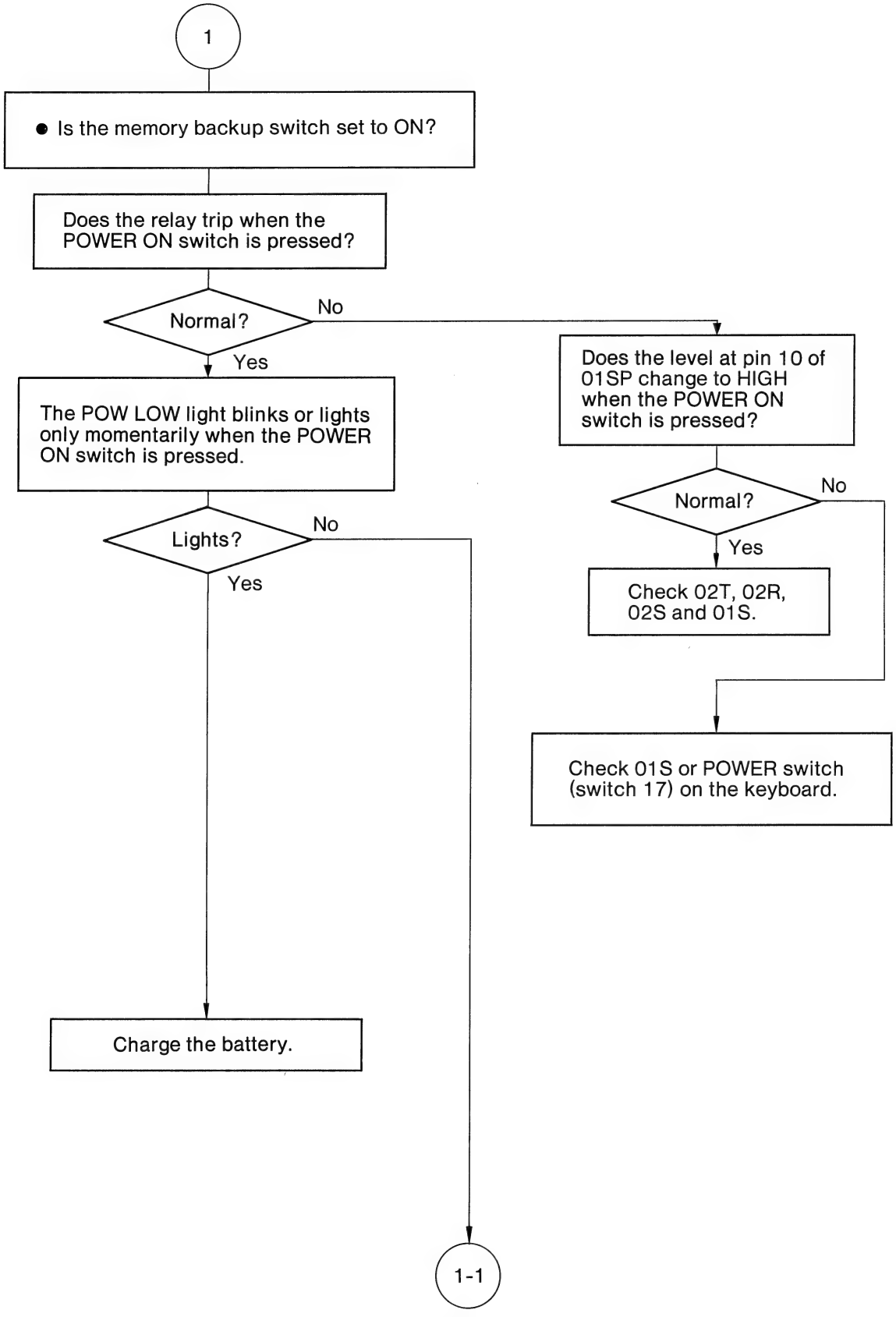
SECTION 6 – – TROUBLESHOOTING

This section contains a check list for testing the TANDY 600 and a troubleshooting flowchart for locating the cause of a failure. Use this section when repairing the unit and for post-repair device inspection.

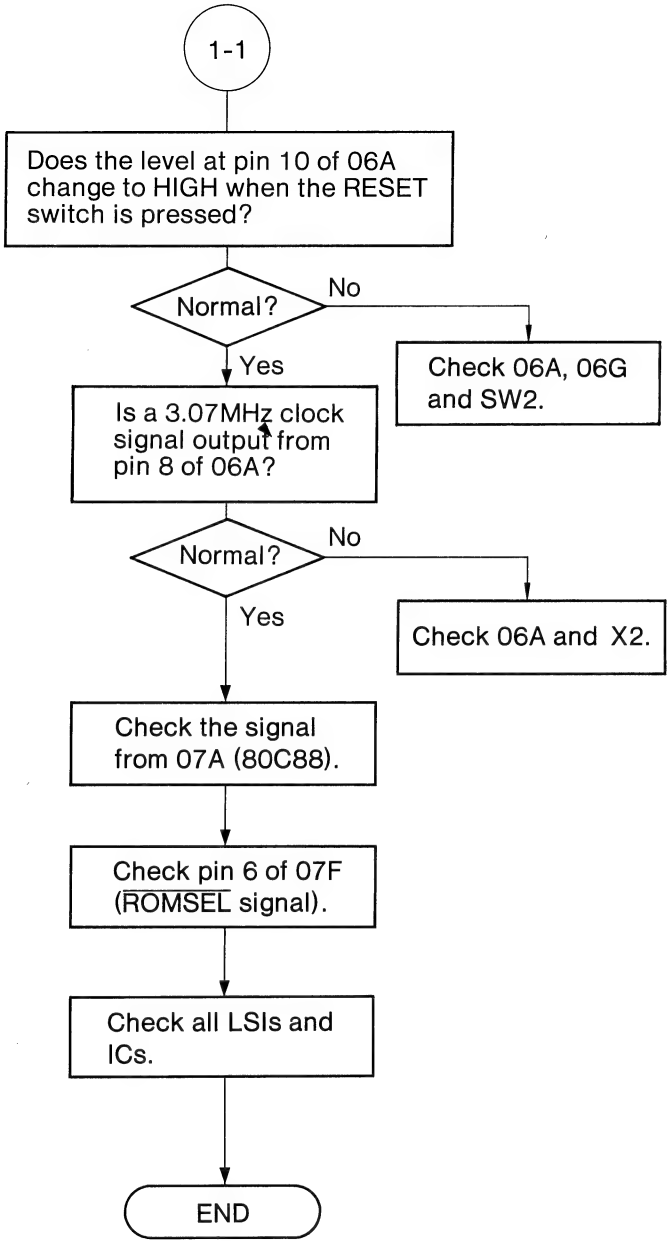
6.1 Troubleshooting Flowchart



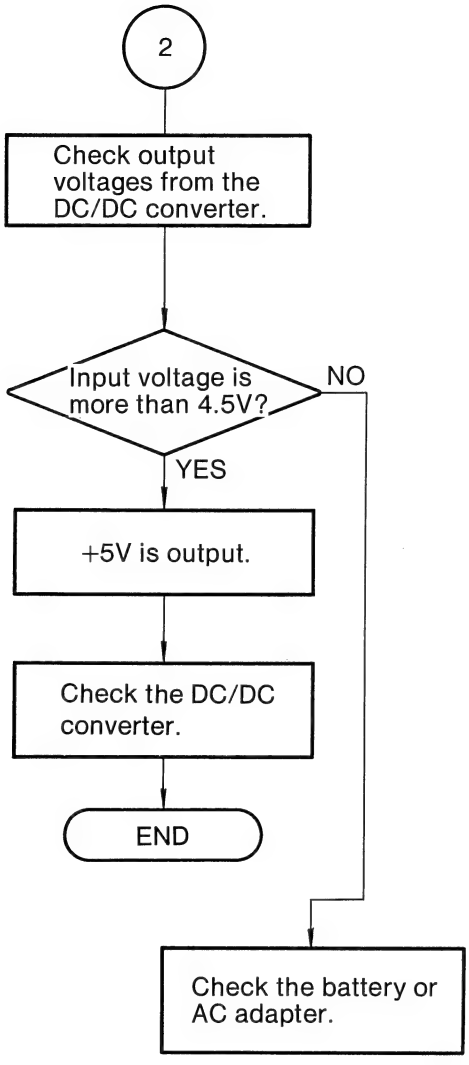
① Will Not Start.



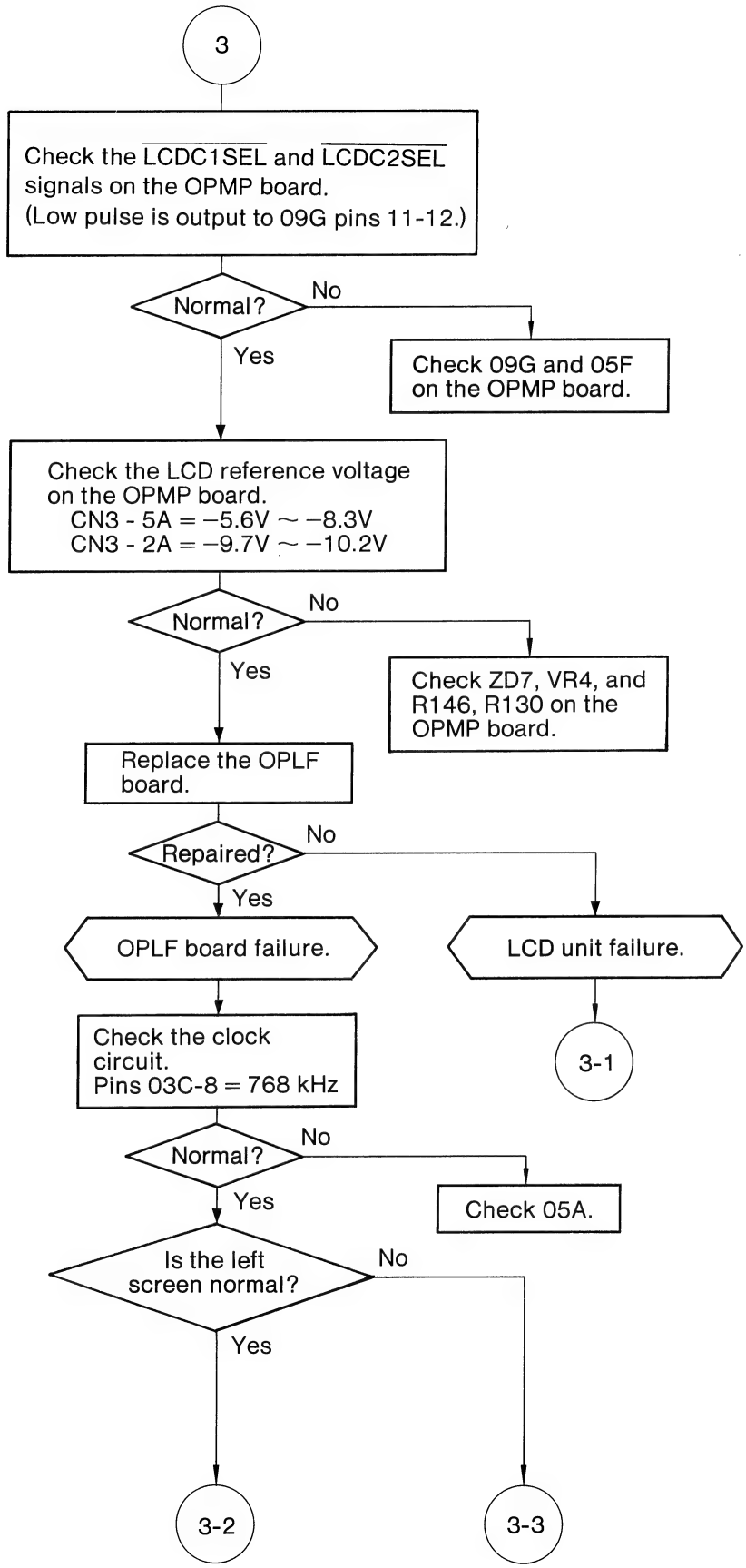
Note: The DC resistance of coils R_{LX} and R_{Ly} is 180 ohms.


1-1
Does the level at pin 10 of 06A change to HIGH when the RESET switch is pressed?
Normal?
No
Yes
Check 06A, 06G and SW2.
Is a 3.07MHz clock signal output from pin 8 of 06A?
Normal?
No
Yes
Check 06A and X2.
Check the signal from 07A (80C88).
Check pin 6 of 07F (ROMSEL signal).
Check all LSIs and ICs.
END

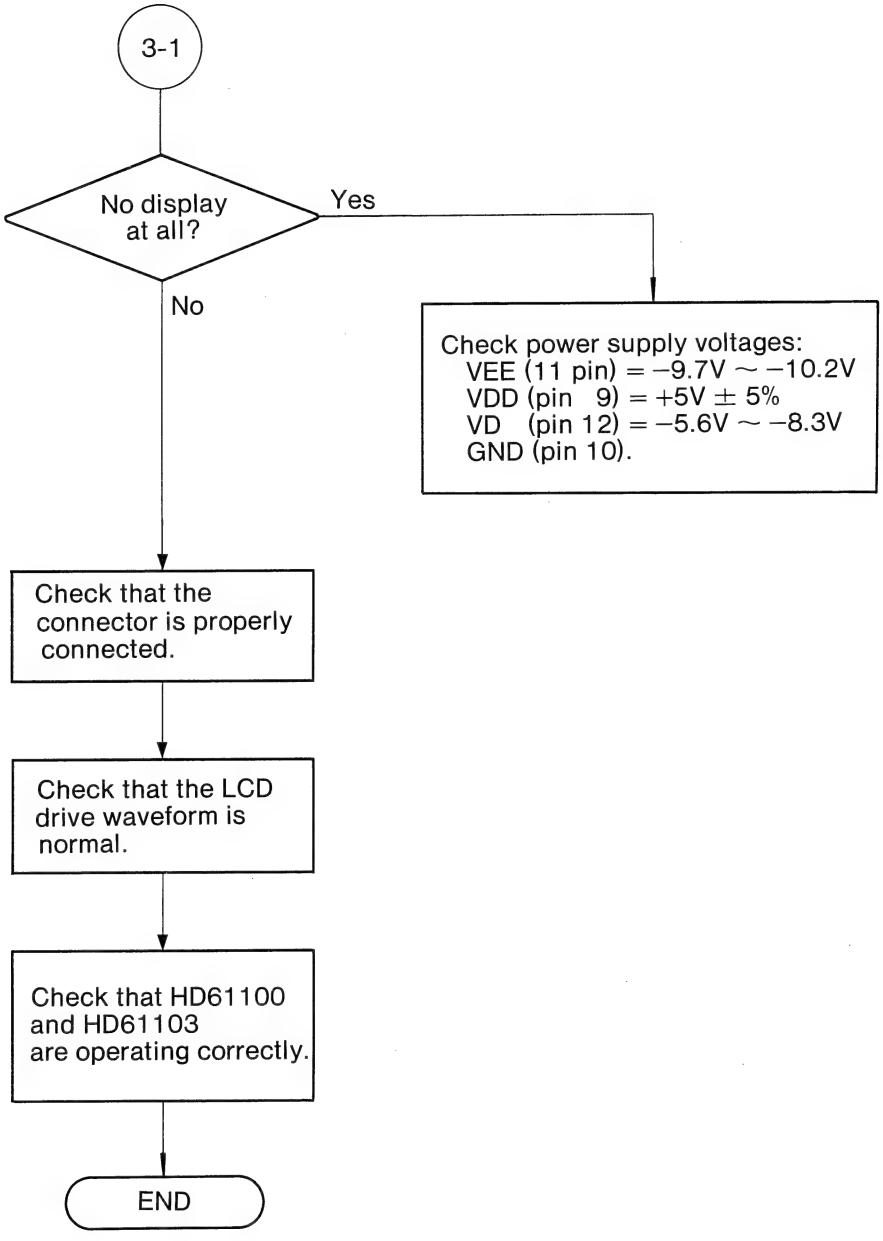
② DC/DC Converter Check.

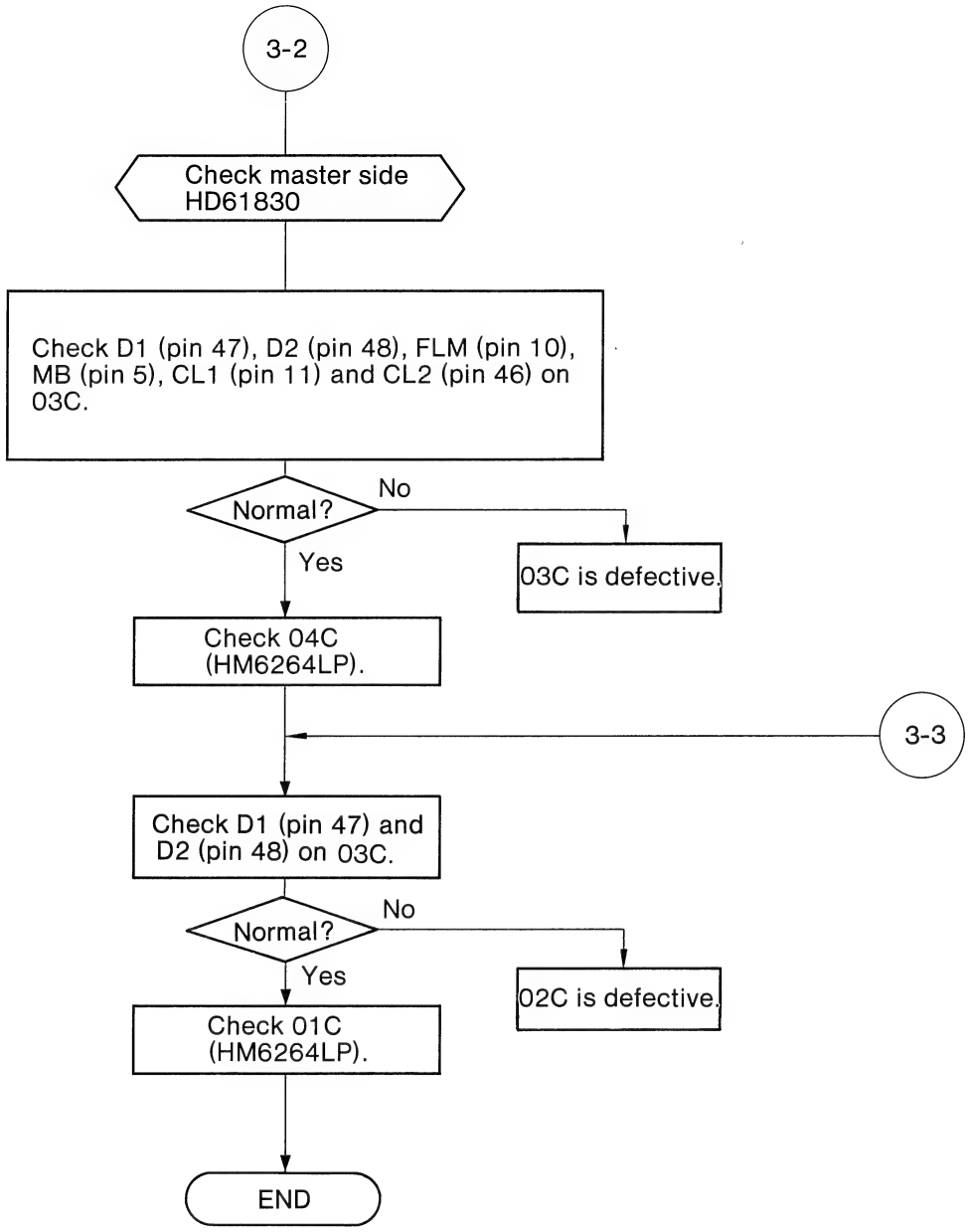


③ LCD Check.

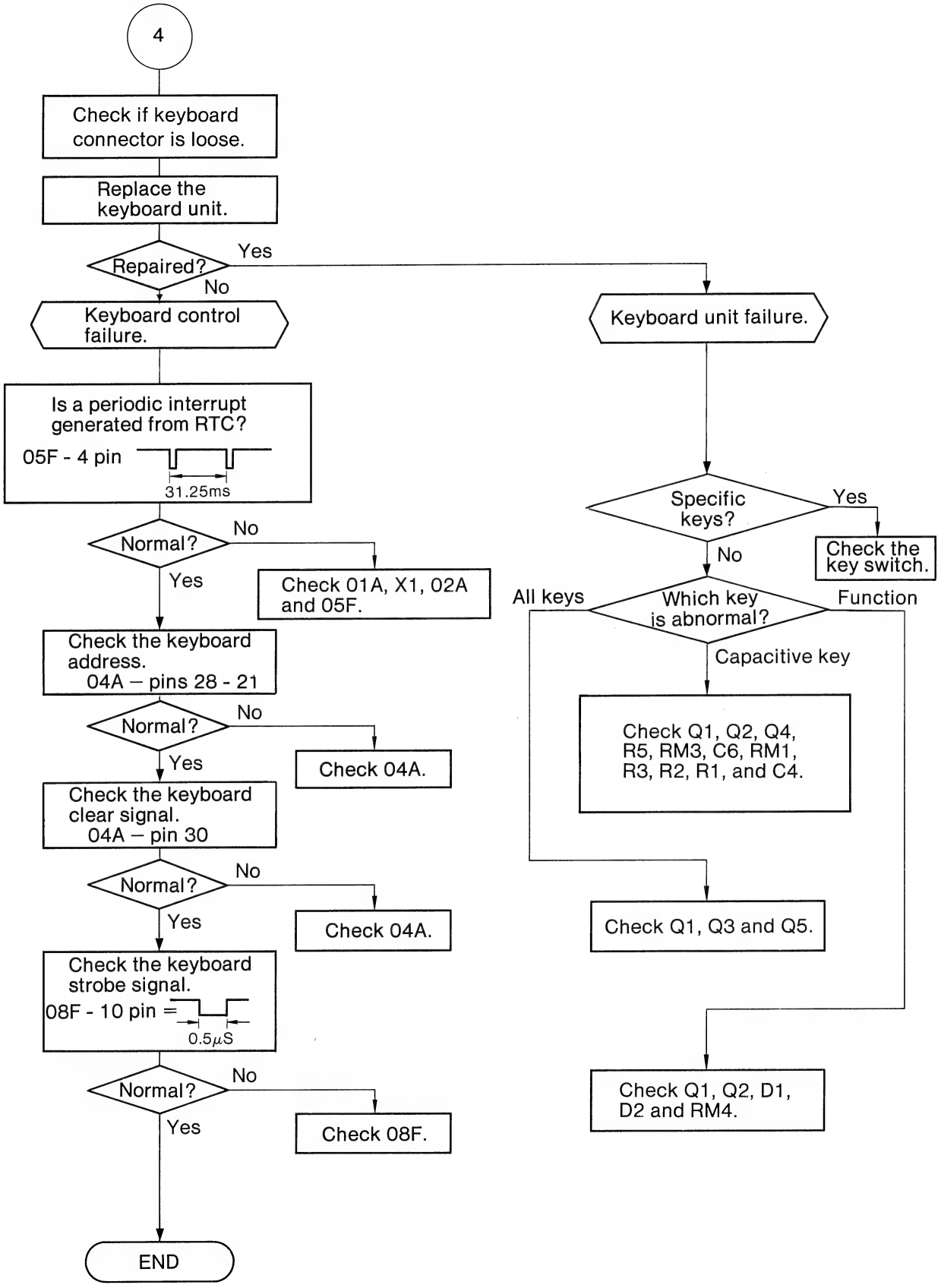

3
Check the $\overline{\text{LCDC1SEL}}$ and $\overline{\text{LCDC2SEL}}$ signals on the OPMP board.
(Low pulse is output to 09G pins 11-12.)
Normal?
No
Yes
Check 09G and 05F on the OPMP board.
Check the LCD reference voltage on the OPMP board.
CN3 - 5A = −5.6V ~ −8.3V
CN3 - 2A = −9.7V ~ −10.2V
Normal?
No
Yes
Check ZD7, VR4, and R146, R130 on the OPMP board.
Replace the OPLF board.
Repaired?
No
Yes
OPLF board failure.
LCD unit failure.
3-1
Check the clock circuit.
Pins 03C-8 = 768 kHz
Normal?
No
Yes
Check 05A.
Is the left screen normal?
No
Yes
3-2
3-3

LCD Unit

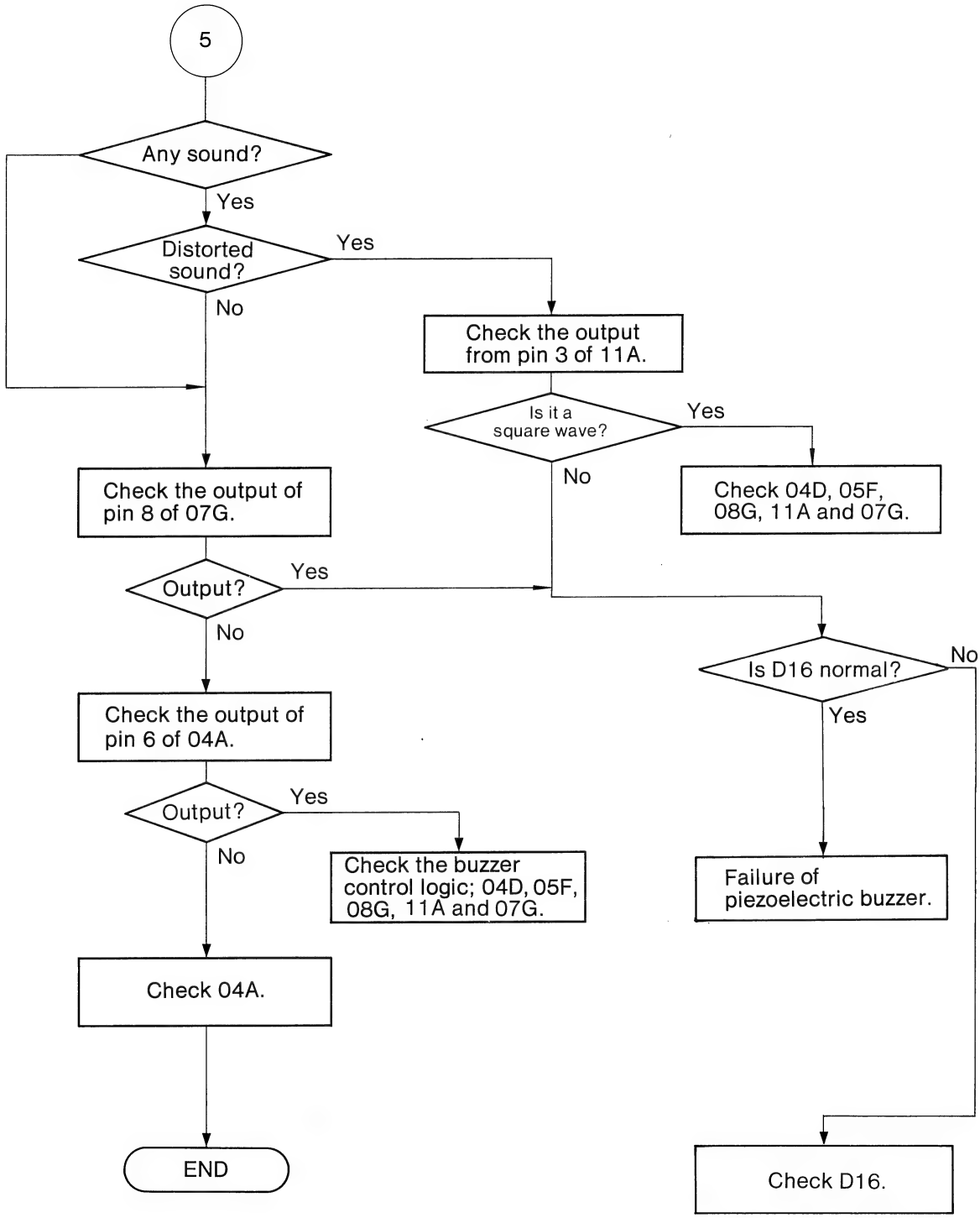

3-1
No display at all?
Yes
No
Check power supply voltages:
VEE (11 pin) = −9.7V ~ −10.2V
VDD (pin 9) = +5V ± 5%
VD (pin 12) = −5.6V ~ −8.3V
GND (pin 10).
Check that the connector is properly connected.
Check that the LCD drive waveform is normal.
Check that HD61100 and HD61103 are operating correctly.
END


3-2
Check master side HD61830
Check D1 (pin 47), D2 (pin 48), FLM (pin 10), MB (pin 5), CL1 (pin 11) and CL2 (pin 46) on 03C.
Normal?
No
Yes
03C is defective.
Check 04C (HM6264LP).
3-3
Check D1 (pin 47) and D2 (pin 48) on 03C.
Normal?
No
Yes
02C is defective.
Check 01C (HM6264LP).
END

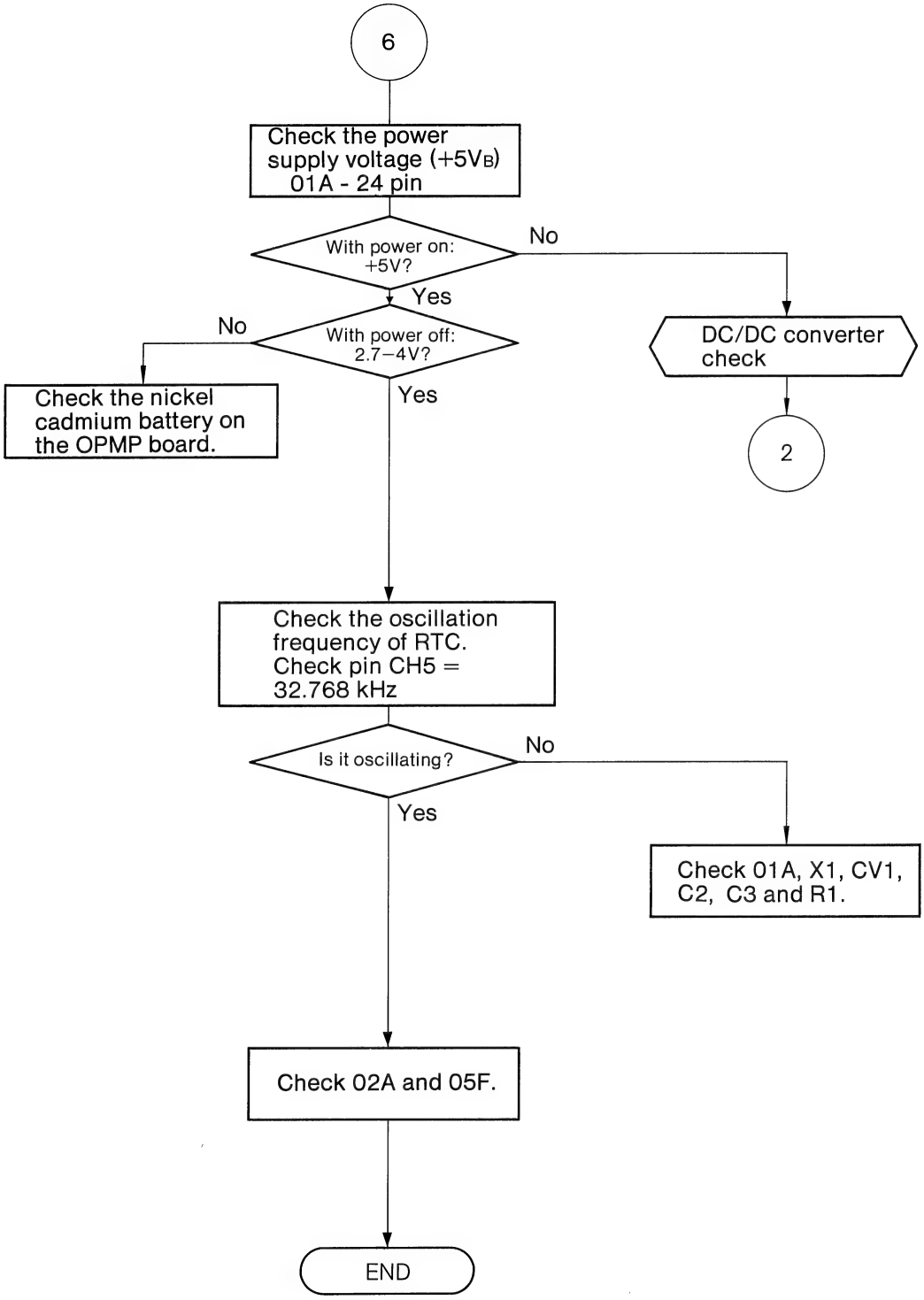
④ Keyboard Check.



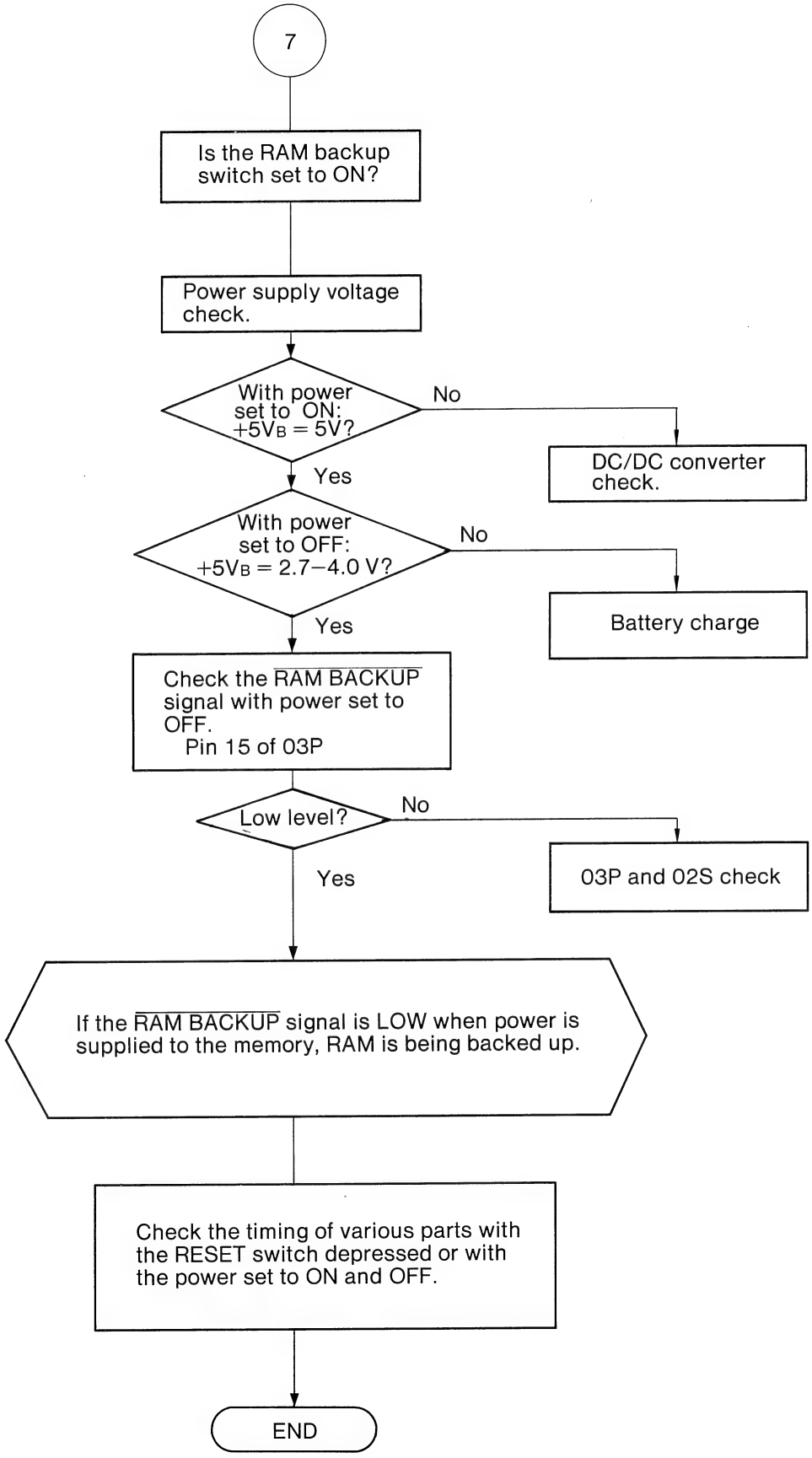
⑤ Buzzer check.



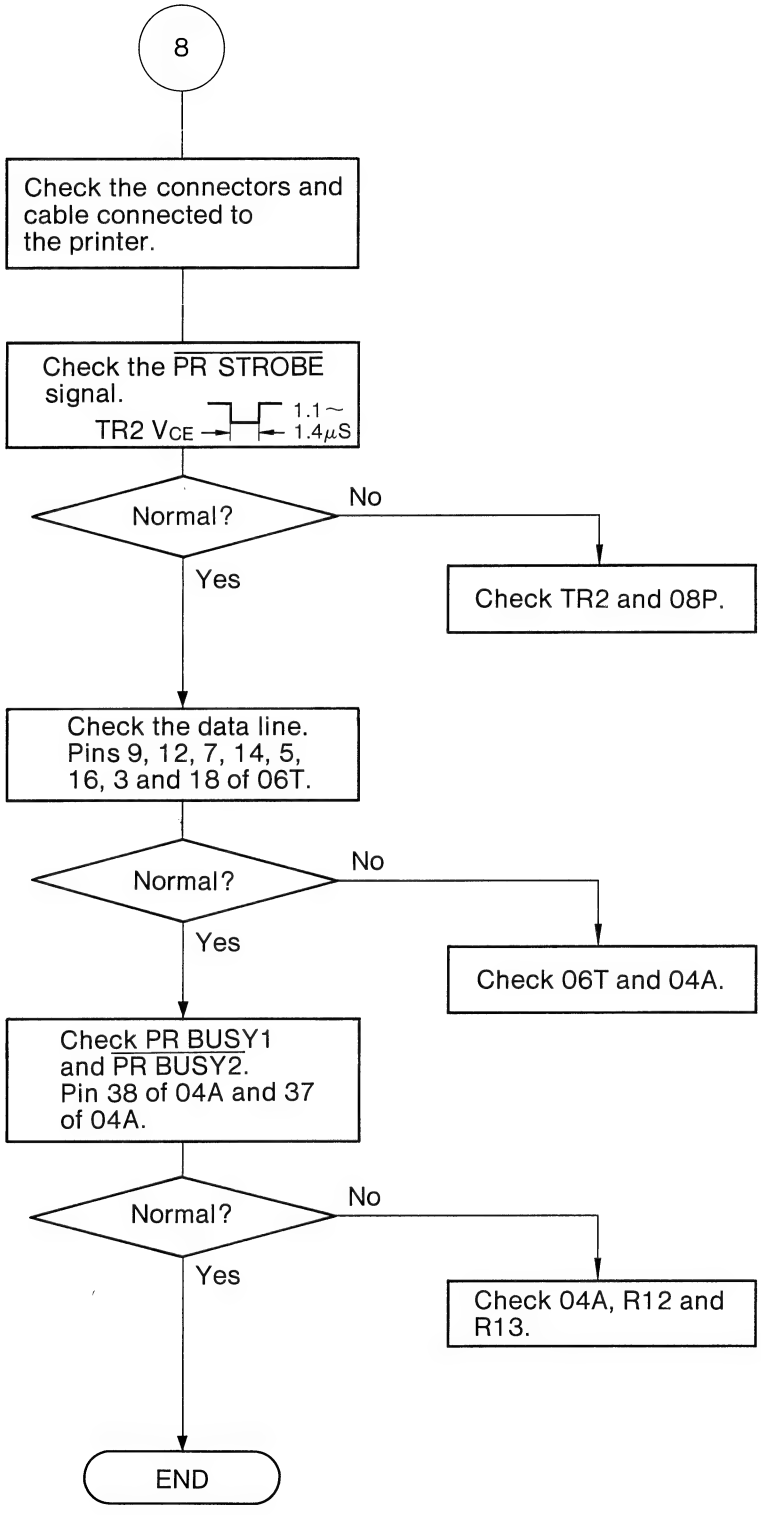
⑥ RTC (Real-Time Clock) Check.



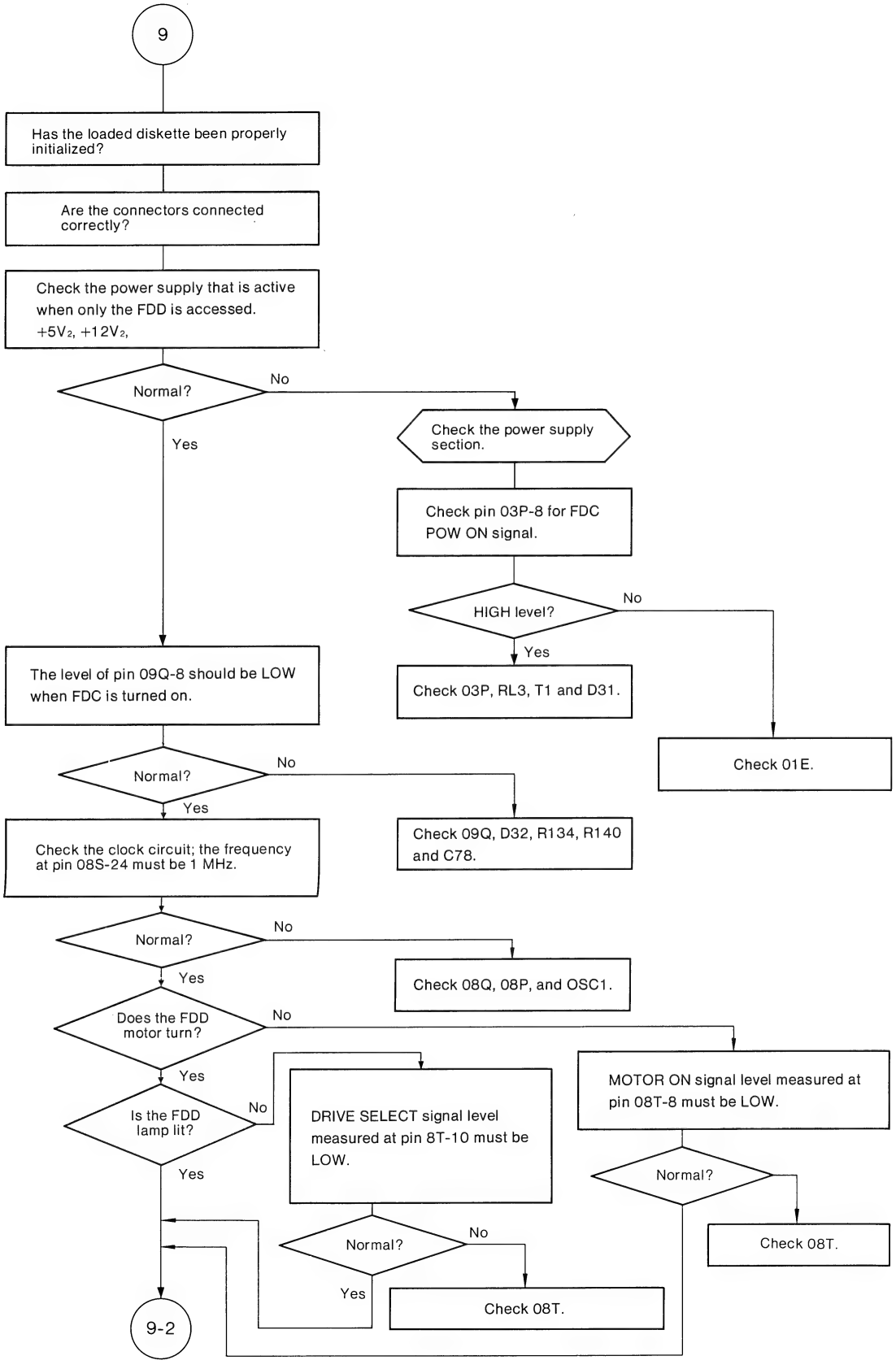
⑦ No Memory Protection.

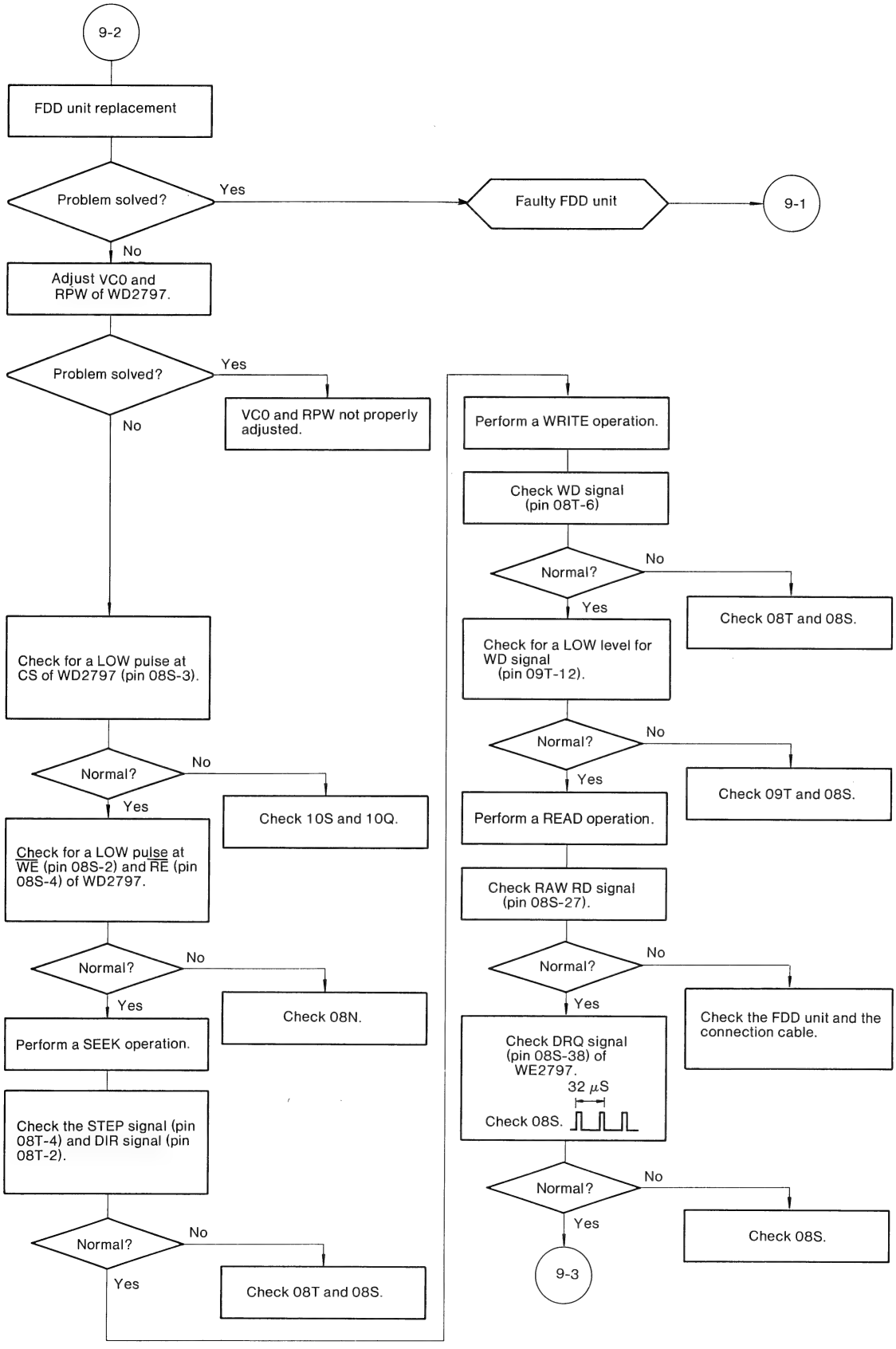


⑧ Printer Interface Check.

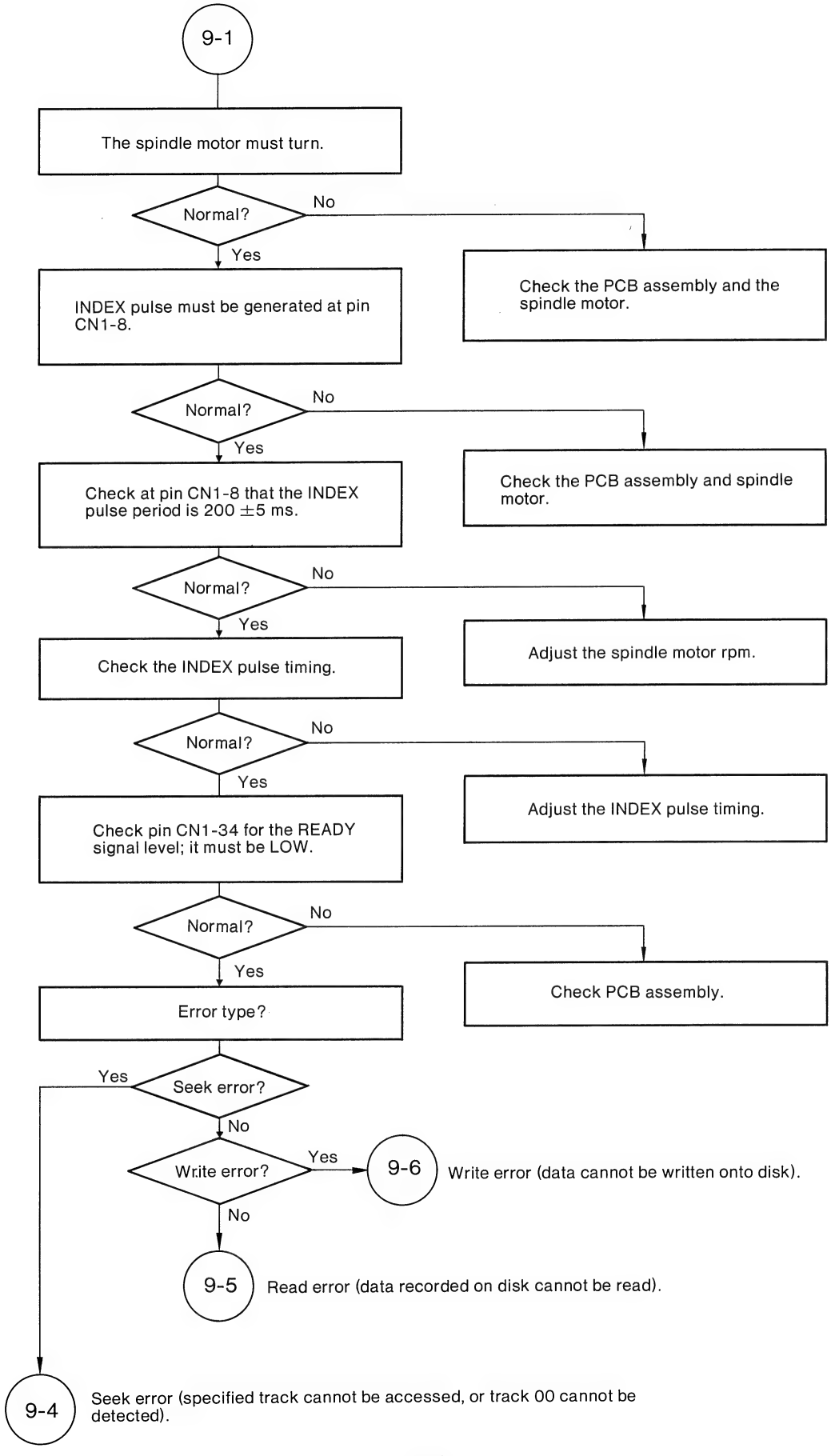


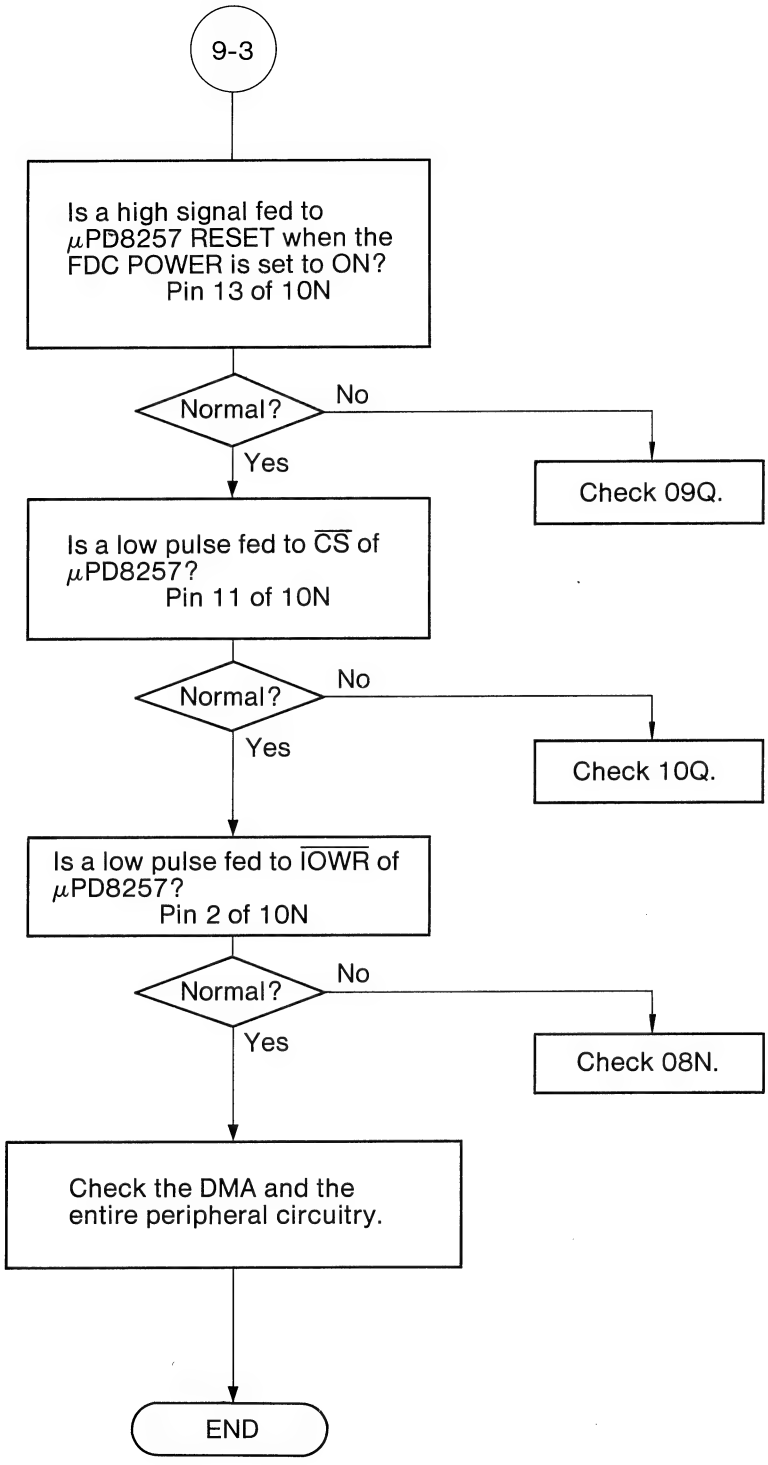
⑨ FDD Troubleshooting.



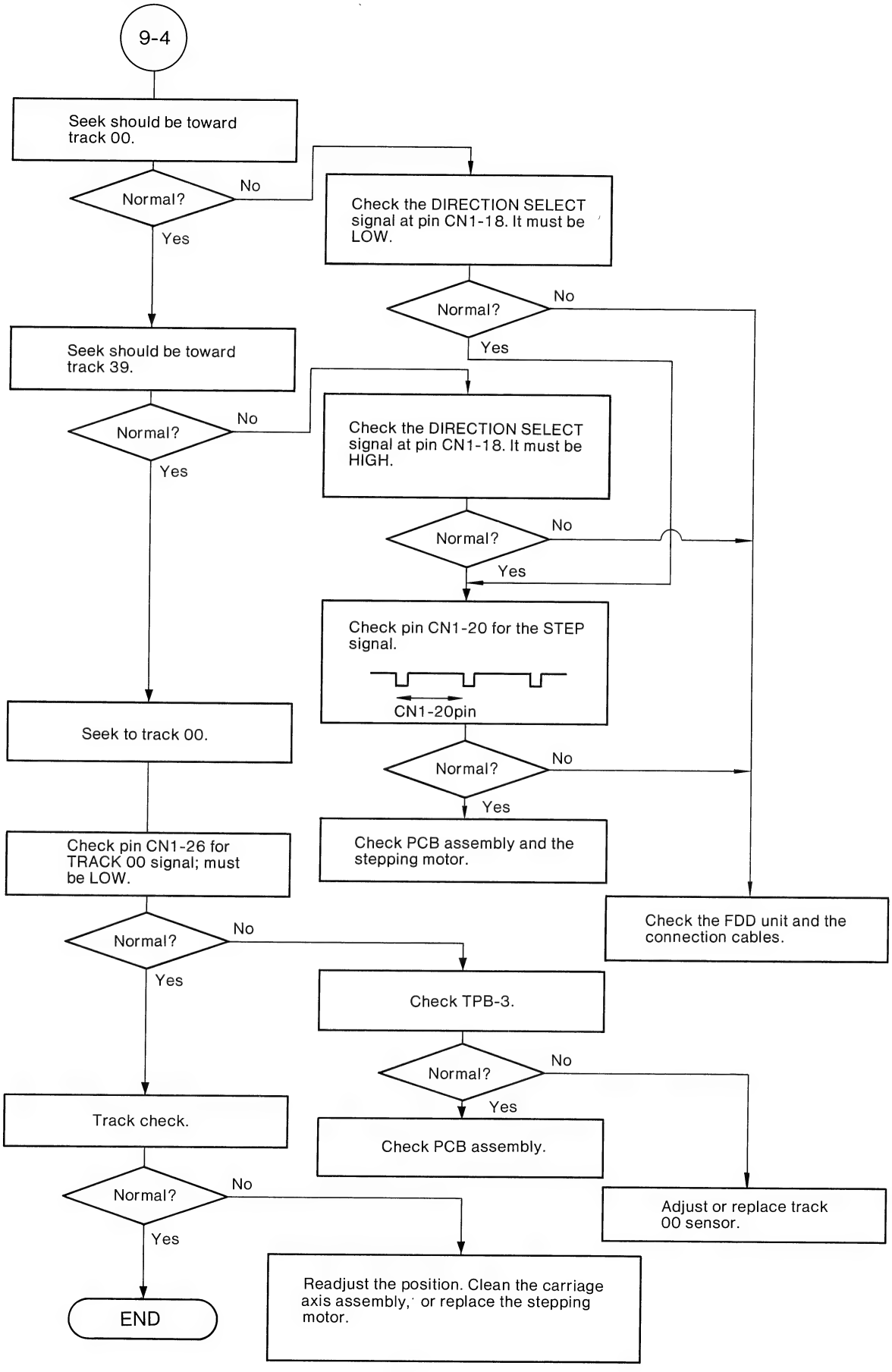

9-2
FDD unit replacement
Problem solved?
Yes
Faulty FDD unit
9-1
No
Adjust VCO and RPW of WD2797.
Problem solved?
Yes
VCO and RPW not properly adjusted.
No
Check for a LOW pulse at CS of WD2797 (pin 08S-3).
Normal?
No
Check 10S and 10Q.
Yes
Check for a LOW pulse at WE (pin 08S-2) and RE (pin 08S-4) of WD2797.
Normal?
No
Check 08N.
Yes
Perform a SEEK operation.
Check the STEP signal (pin 08T-4) and DIR signal (pin 08T-2).
Normal?
No
Check 08T and 08S.
Yes
Perform a WRITE operation.
Check WD signal (pin 08T-6)
Normal?
No
Check 08T and 08S.
Yes
Check for a LOW level for WD signal (pin 09T-12).
Normal?
No
Check 09T and 08S.
Yes
Perform a READ operation.
Check RAW RD signal (pin 08S-27).
Normal?
No
Check the FDD unit and the connection cable.
Yes
Check DRQ signal (pin 08S-38) of WE2797.
32 μS
Check 08S.
Normal?
No
Check 08S.
Yes
9-3

FDD Unit

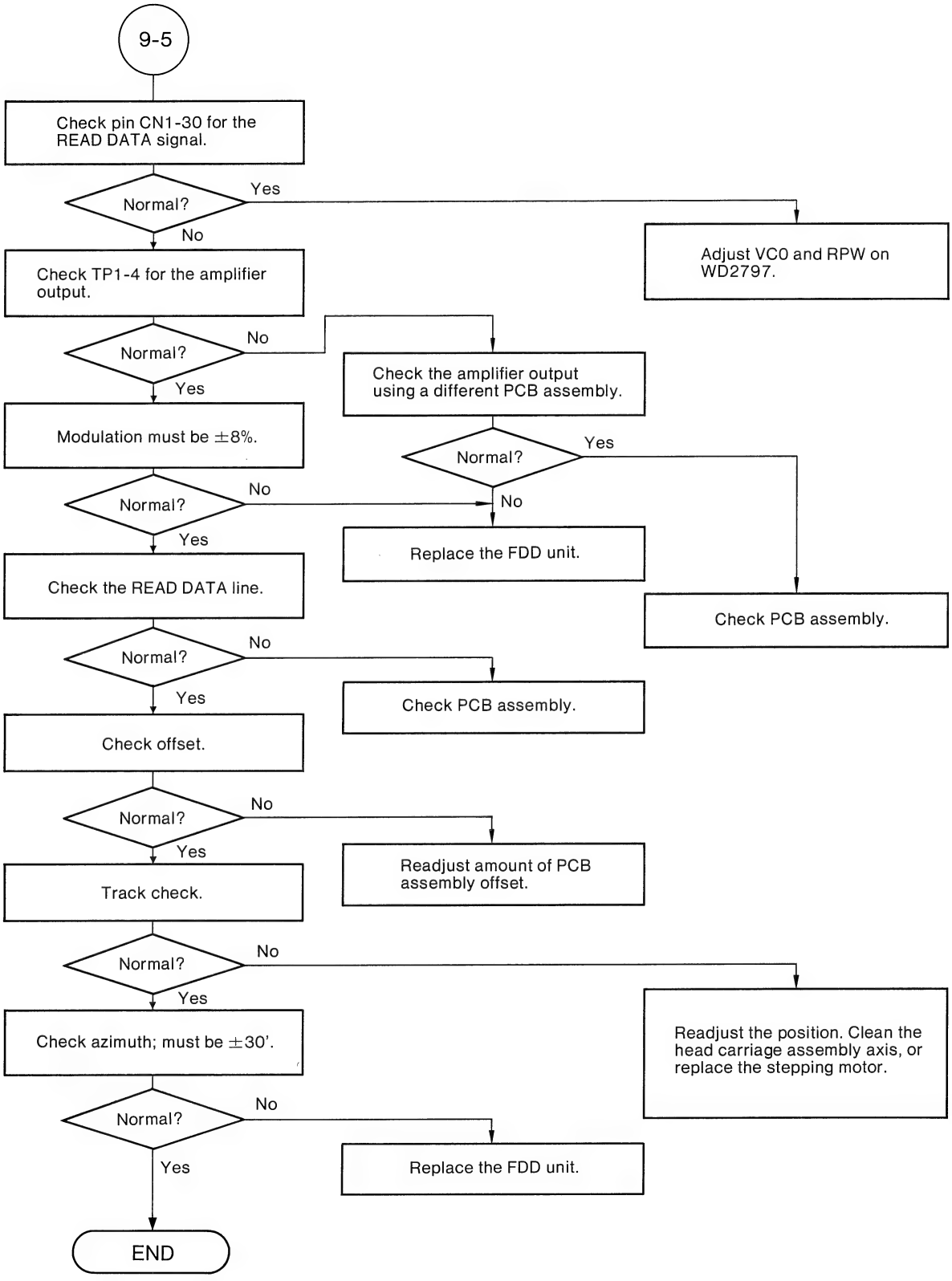

9-1
The spindle motor must turn.
Normal?
No
Yes
Check the PCB assembly and the spindle motor.
INDEX pulse must be generated at pin CN1-8.
Normal?
No
Yes
Check the PCB assembly and spindle motor.
Check at pin CN1-8 that the INDEX pulse period is 200 ±5 ms.
Normal?
No
Yes
Adjust the spindle motor rpm.
Check the INDEX pulse timing.
Normal?
No
Yes
Adjust the INDEX pulse timing.
Check pin CN1-34 for the READY signal level; it must be LOW.
Normal?
No
Yes
Check PCB assembly.
Error type?
Yes
Seek error?
No
Write error?
Yes
9-6
Write error (data cannot be written onto disk).
No
9-5
Read error (data recorded on disk cannot be read).
9-4
Seek error (specified track cannot be accessed, or track 00 cannot be detected).


9-3
Is a high signal fed to μPD8257 RESET when the FDC POWER is set to ON?
Pin 13 of 10N
Normal?
No
Yes
Check 09Q.
Is a low pulse fed to $\overline{CS}$ of μPD8257?
Pin 11 of 10N
Normal?
No
Yes
Check 10Q.
Is a low pulse fed to $\overline{IOWR}$ of μPD8257?
Pin 2 of 10N
Normal?
No
Yes
Check 08N.
Check the DMA and the entire peripheral circuitry.
END

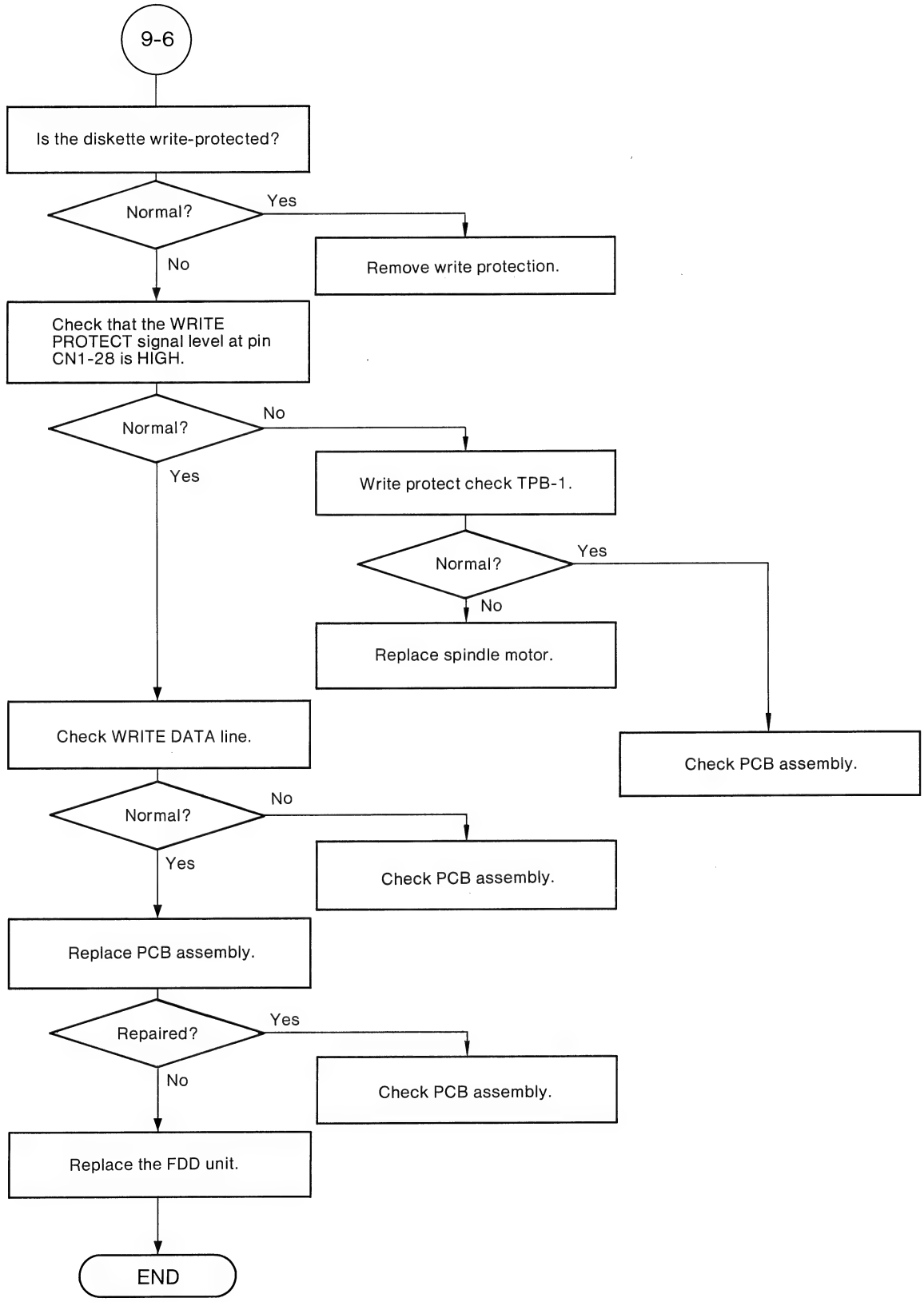
FDD Unit (Seek Error)



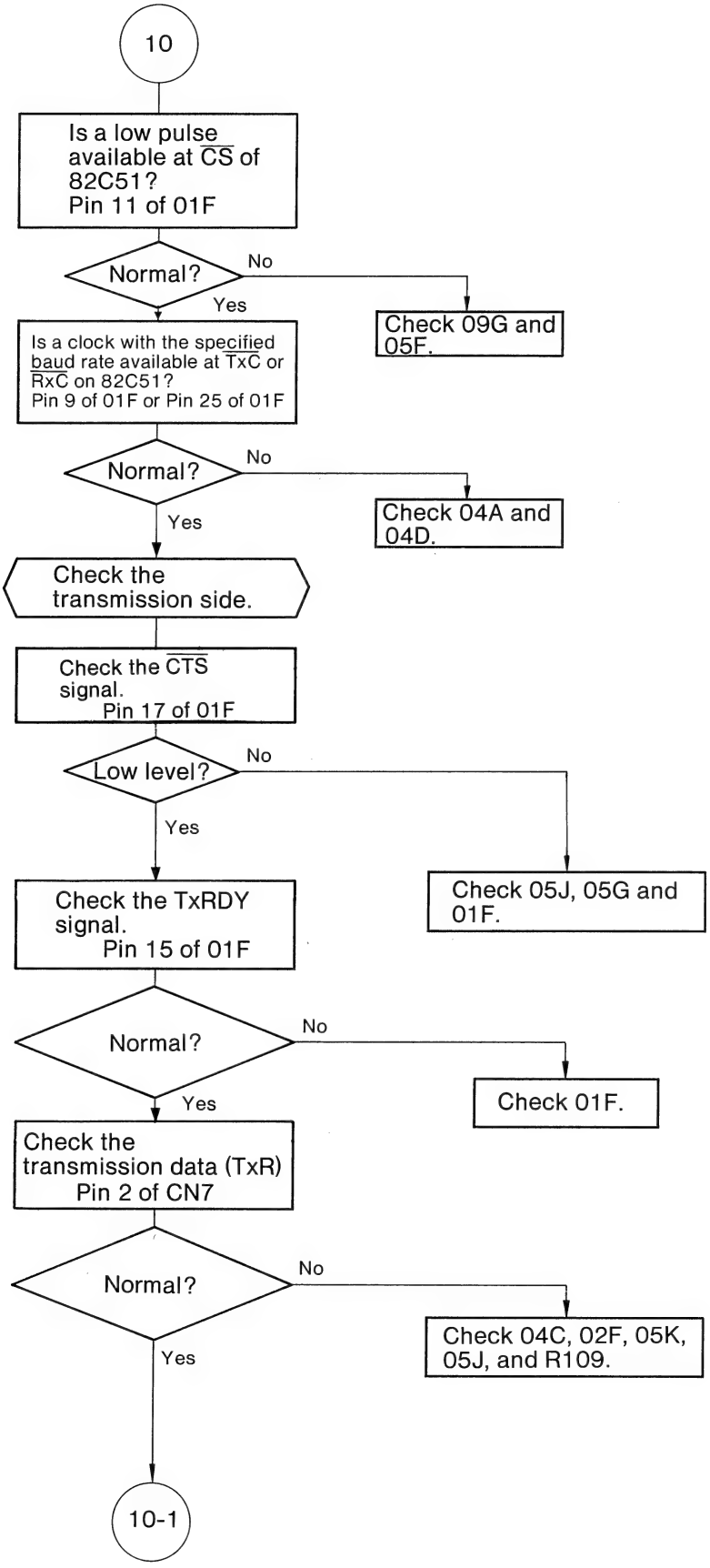
FDD Unit (Read Error)

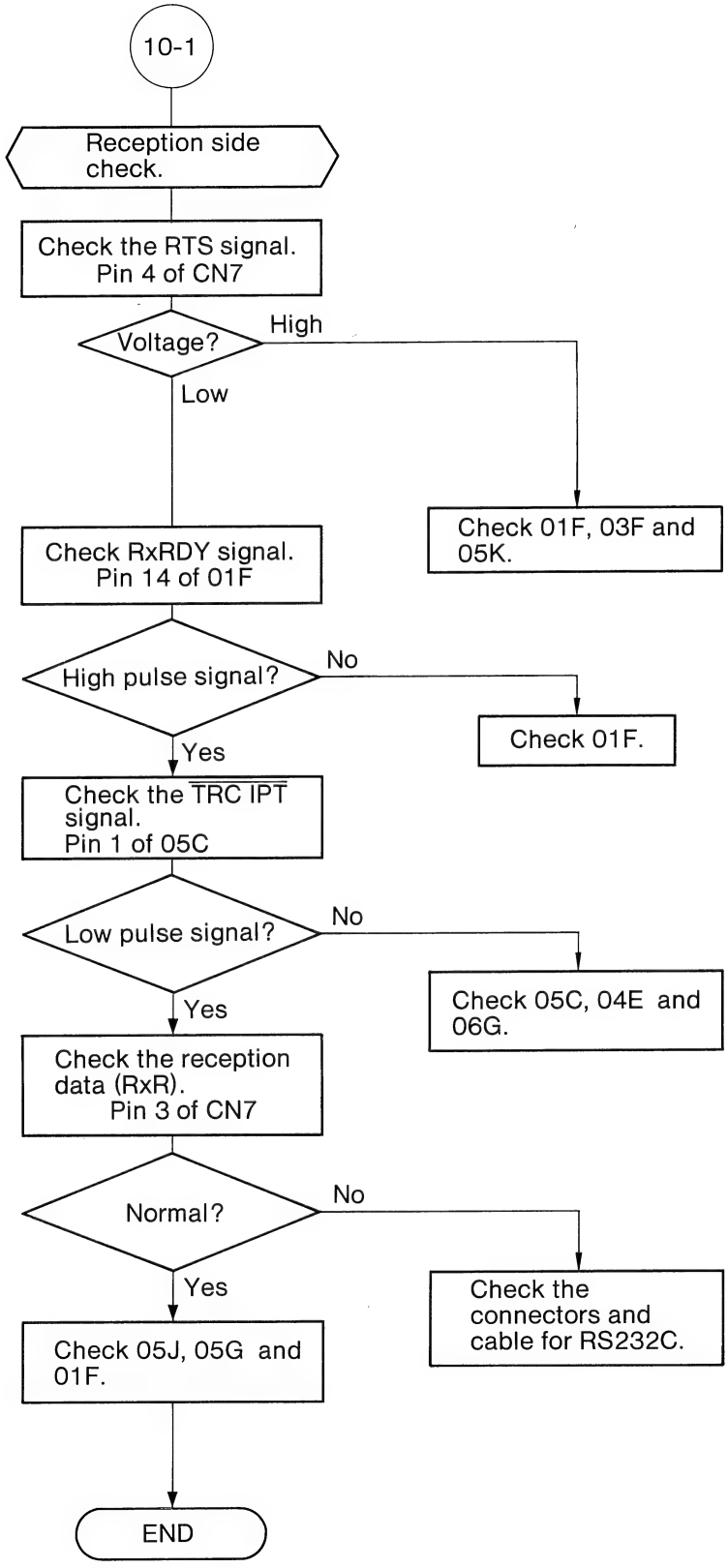


FDD Unit (Write Error)

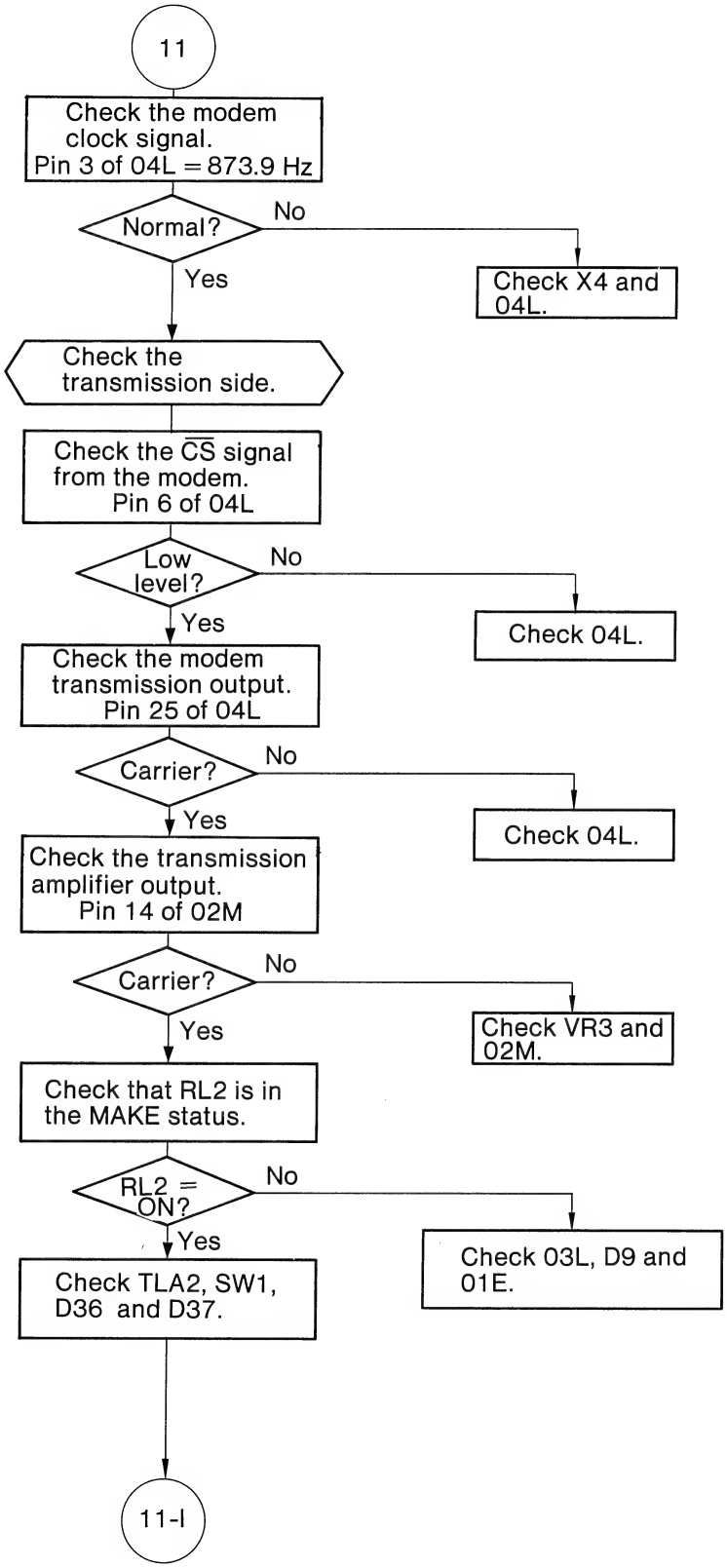


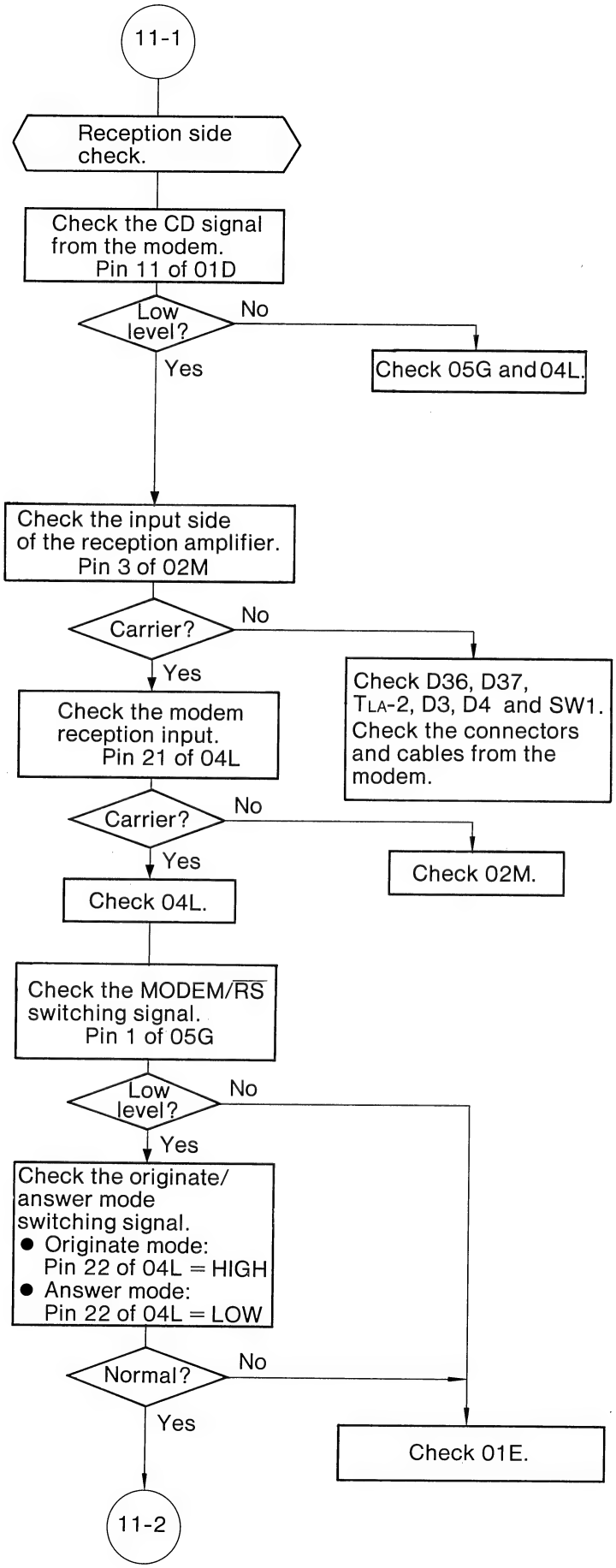
⑩ RS232C Interface Check.

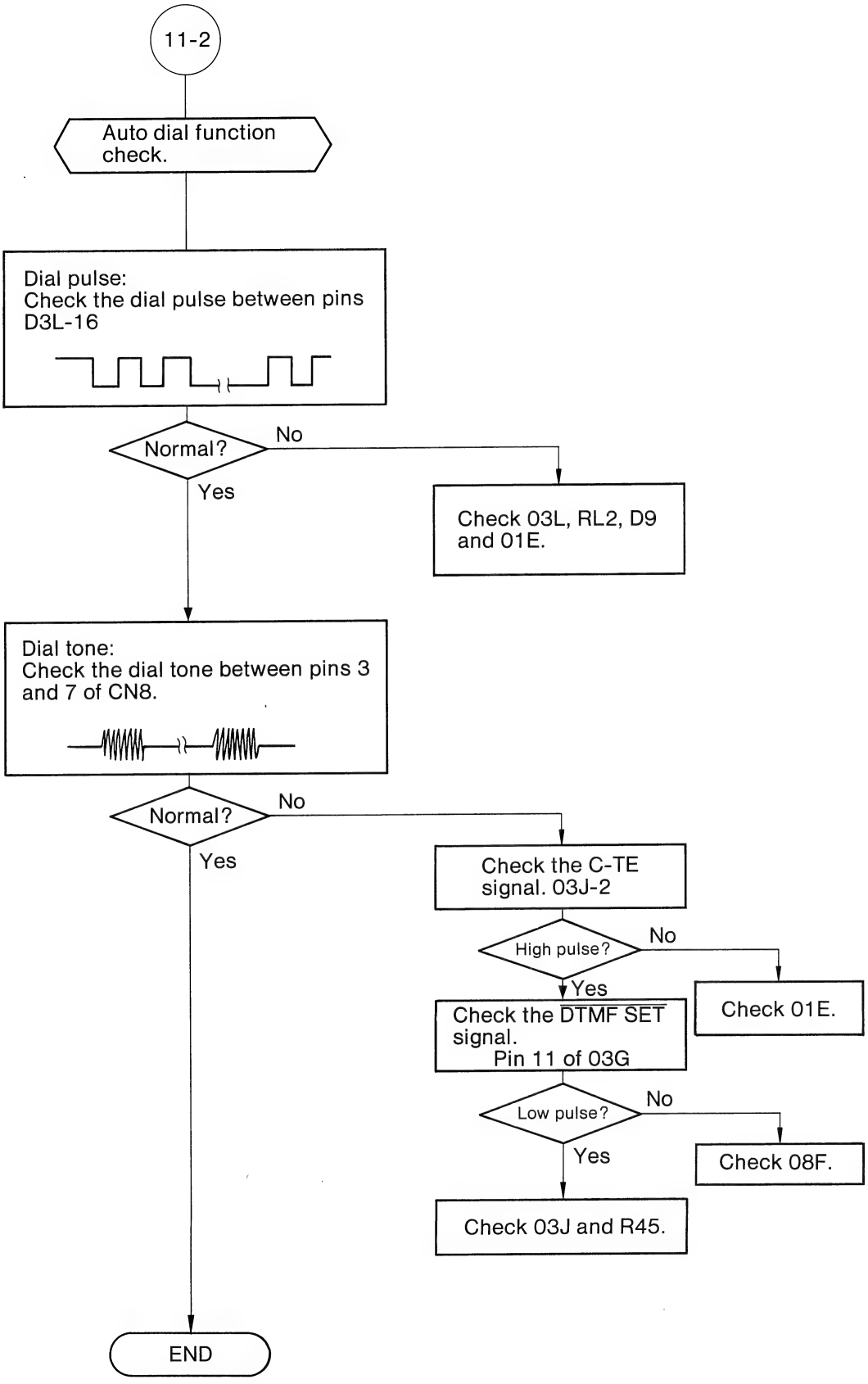



10-1
Reception side check.
Check the RTS signal. Pin 4 of CN7
Voltage?
High
Low
Check 01F, 03F and 05K.
Check RxRDY signal. Pin 14 of 01F
High pulse signal?
No
Check 01F.
Yes
Check the TRC IPT signal. Pin 1 of 05C
Low pulse signal?
No
Check 05C, 04E and 06G.
Yes
Check the reception data (RxR). Pin 3 of CN7
Normal?
No
Check the connectors and cable for RS232C.
Yes
Check 05J, 05G and 01F.
END

⑪ Modem Interface Check.




11-1
Reception side check.
Check the CD signal from the modem. Pin 11 of 01D
Low level?
No
Yes
Check 05G and 04L.
Check the input side of the reception amplifier. Pin 3 of 02M
Carrier?
No
Yes
Check D36, D37, TLA-2, D3, D4 and SW1. Check the connectors and cables from the modem.
Check the modem reception input. Pin 21 of 04L
Carrier?
No
Yes
Check 02M.
Check 04L.
Check the MODEM/RS switching signal. Pin 1 of 05G
Low level?
No
Yes
Check the originate/ answer mode switching signal.
● Originate mode: Pin 22 of 04L = HIGH
● Answer mode: Pin 22 of 04L = LOW
Normal?
No
Yes
Check 01E.
11-2


11-2
Auto dial function check.
Dial pulse:
Check the dial pulse between pins D3L-16
Normal?
No
Yes
Check 03L, RL2, D9 and 01E.
Dial tone:
Check the dial tone between pins 3 and 7 of CN8.
Normal?
No
Yes
Check the C-TE signal. 03J-2
High pulse?
No
Yes
Check 01E.
Check the DTMF SET signal.
Pin 11 of 03G
Low pulse?
No
Yes
Check 08F.
Check 03J and R45.
END

6.2 Check List

After all repairs and calibrations are completed, all functions are checked by running the "test program." However, before starting the checking procedure, perform a cold start (see procedure (4)).

(1) Buzzer and LCD Check (BASIC mode)

```
10  FOR I = 0 TO 255
20  PRINT CHR$ (I)
30  NEXT I
40  END
```

Operation

After the buzzer sounds once, the LCD display is cleared and all printable characters are displayed.

(2) Clock Test (BASIC mode)

a. Set the year, month, day, day of week, hour, minute, and second.
   Year, month and day setting: DATE = "MM/DD/YY"
   Day of week setting: DAY = "day-of-week" (e.g., SUN for Sunday)
   Hour, minute and second setting: TIME = "HH:MM:SS."
b. Check the data that is set.
   Return to the main menu using the MENU command. Confirm that the calendar values have been changed to the set values.

(3) Keyboard Test

Refer to the key functions shown in the owner's manual. Check that all functions operate as they should.

(4) Reset Function Test (Memory Protection Test)

a. Warm test
   Turn the computer off, then on again. Or, set the POWER switch to ON, and press the RESET (rear) switch. Check if all user files are displayed.
b. Cold test
   While pressing the CTRL key or the PAUSE key, press the RESET switch to check whether all previously created user files have been erased and whether the data has been initialized.

(5) Printer Interface Test (BASIC Mode)

Enter the characters to be printed on the LCD display. Then, press the hardcopy key, PRINT, to print out all the displayed characters.

(6) FDD Test (BASIC Mode)

Type out 3 to 4 lines of a program. The program is saved on a magnetic tape using the "SAVE filename" command. The program is then loaded using the "LOAD filename" command. A check can be made as to whether the program was set correctly.

(7) RS232C and Modem Test

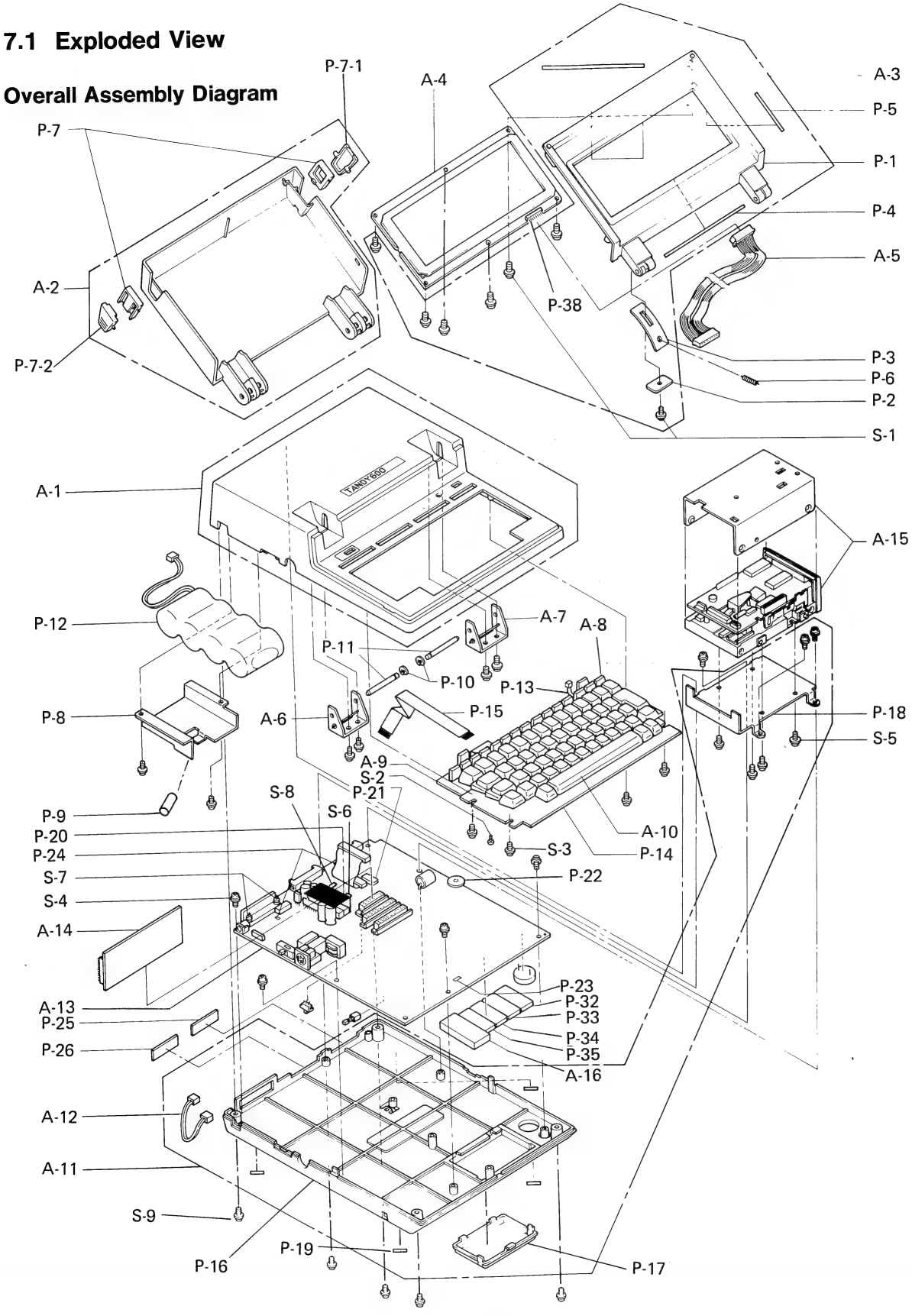
Data transmission and reception are performed first using the RS232C interface, then using the modem.

Section 7
EXPLODED VIEW AND PARTS LIST

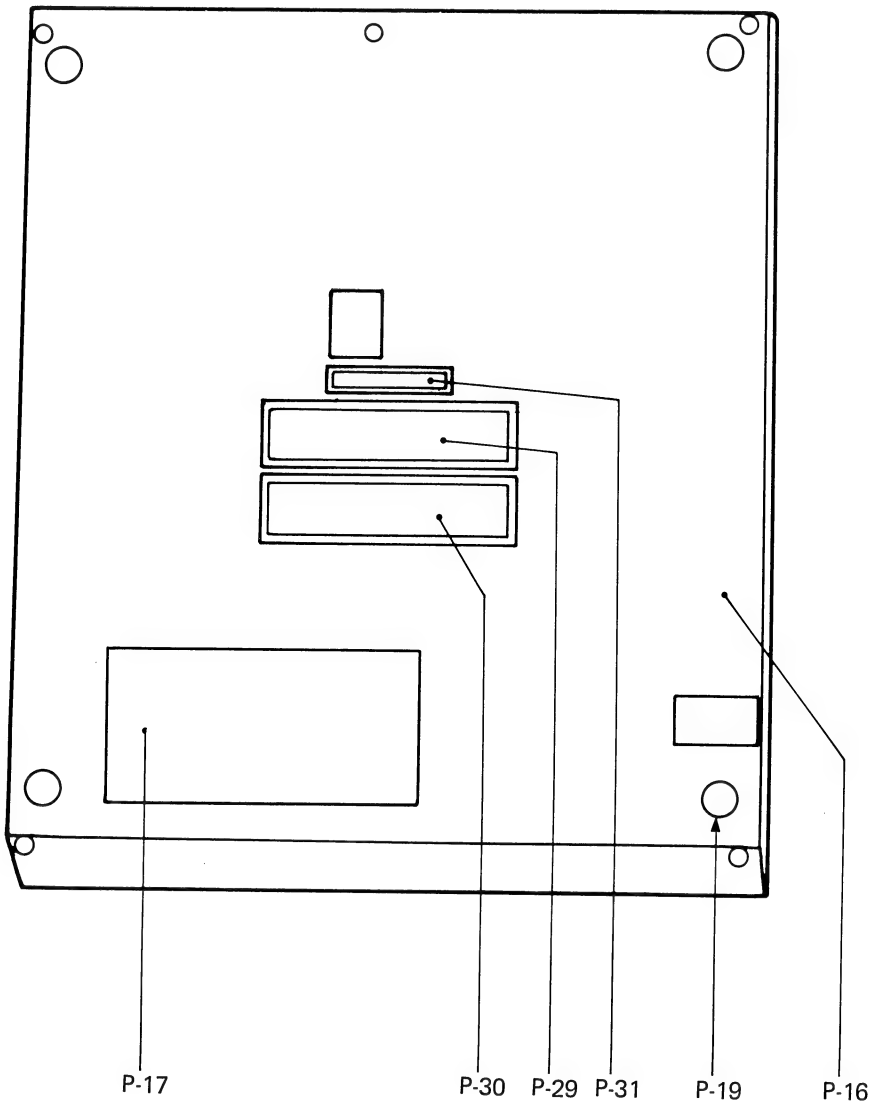
SECTION 7 – – EXPLODED VIEW AND PARTS LIST

7.1 Exploded View

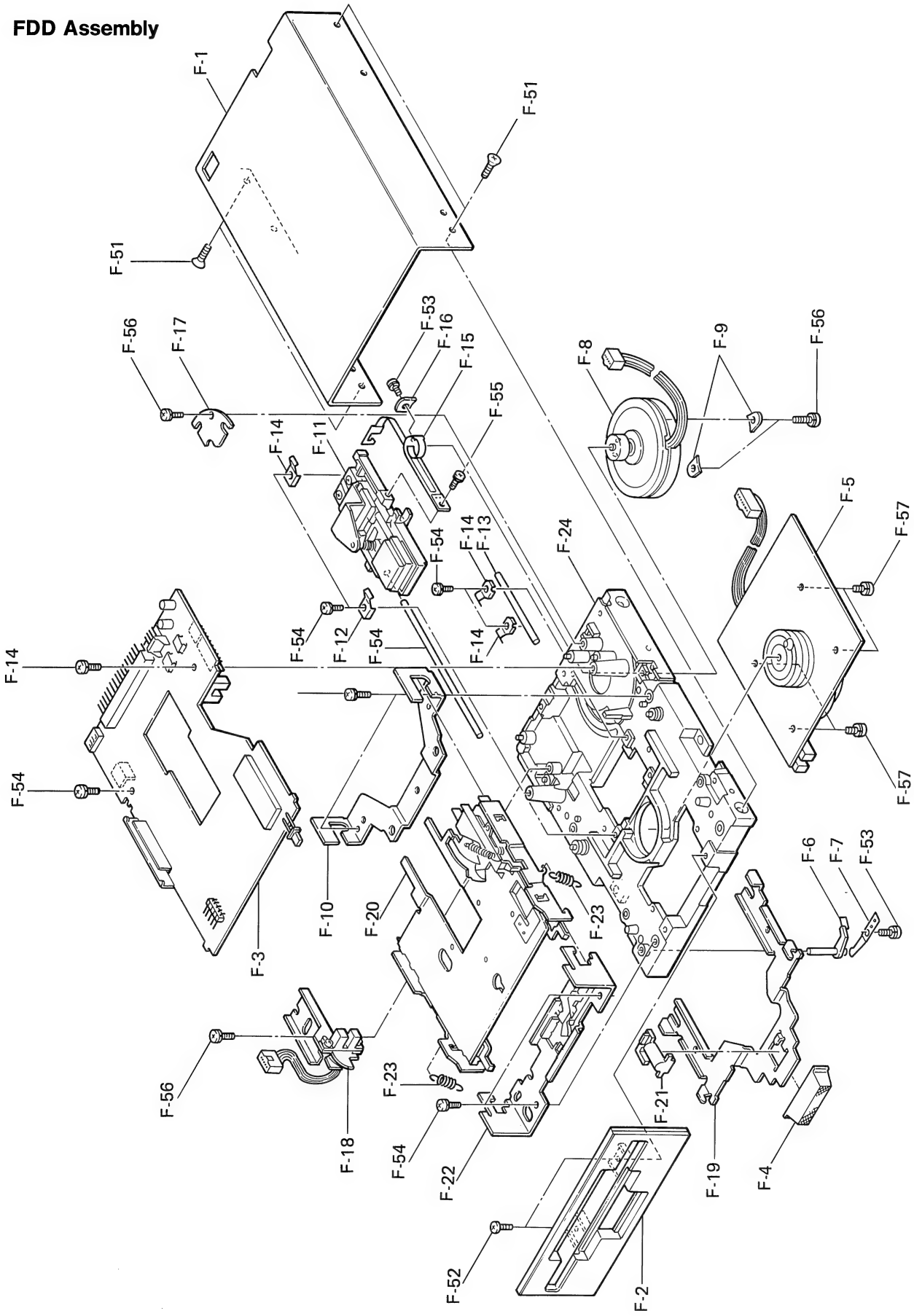
Overall Assembly Diagram



Bottom View



FDD Assembly



7.2 Parts List

MAIN PCB ASSEMBLY (OPMP Board)

Ref. No.	Description	RS Part No.	Mfr's Part No.
Battery			
BAT 1	Battery, 3-51FT-P	ACS0013	4LP-45472
Buzzer			
BZ 1	Buzzer, PKM24-4A0	AB7132	550A1047P0250
Capacitors			
C 2/C 3	Ceramic, TCC45SL1H330JYA, 33pF, 50V, ±10%	CC330KJCP	302A1024K0330
C 4	Ceramic, RPE123-127F105Z25, 1µF, 25V, +80/-20%	CC105ZFCP	303A4117Z2105
C 5-C35	Ceramic, FK20Y5V1H104Z, 0.1µF 50V, +80/-20% or RPE122-129F104Z50	CC104ZJCP	303A420Z3104
C36	Plastic Film, CF93MMA2E474M, 250V, 0.47µF, ±20%	CC474MRYP	306A2201M5474
C37	Electrolytic, 10MS5-10M, 10V, 10µF, ±20%	CC106MCAP	304A1046A1100
C38	Electrolytic, 10MS5-33M, 10V, 33µF, ±20%	CC336MCAP	304A1046A1330
C39	Mica, DM19E562K1, 100V, 5600pF, ±10%	CC562KLWP	301A1142K3562
C41	Ceramic, RPE122-127C223M50, 0.022µF, 50V, ±20%	CC223MJCP	303A4115M3223
C42	Electrolytic, 35MS5-2.2M, 35V, 2.2µF, ±20%	CC225MGAP	304A1046V1229
C43	Electrolytic, 10MS5-10M, 10V, 10µF, ±20%	CC106MCAP	304A1046A1100
C44	Ceramic, RPE122-127C223M50, 0.022µF, 50V, ±20%	CC223MJCP	303A4115M3223
C45	Electrolytic, 35MS5-2.2M, 35V, 2.2µF, ±20%	CC225MGAP	304A1046V1229
C46	Electrolytic, 10MS5-10M, 10V, 10µF, ±20%	CC106MCAP	304A1046A1100
C47	Ceramic, RPE122-127C103M50, 0.01µF, 50V, ±20%	CC103MJCP	303A4115M3103
C48	Ceramic, RPE123-127F105Z25, 1µF, 25V, +80/-20%	CC105ZFCP	303A4117Z2105
C49-C51	Ceramic, RPE122-127C102M50, 0.001µF, 50V, ±20%	CC102MJCP	303A4115M3102
C52/C53	Electrolytic, 25MS5-10M, 25V, 10µF, ±20%	CC106MFAP	304A1046E1100
C57	Electrolytic, 10MS5-68M, 10V, 68µF, ±20%	CC686MCAP	304A1046A1680
C58	Electrolytic, 10MS5-10M, 10V, 10µF, ±20%	CC106MCAP	304A1046A1100
C59	Ceramic, FD23Y5V1H225Z, 50V, 22µF, +80/-20%	CC226JCP	303A4117Z3225

Ref. No.	Description	RS Part No.	Mfr's Part No.
C63	Electrolytic, CE4W1A101, 100μF, 10V, ±20%	CC107MCAP	304A0101A1101
C64	Electrolytic, SRC10VB-220(M), 10V, 220μF, ±20%	CC227MCAP	304A1035A1221
C65	Electrolytic, CESHM1A102, 1000μF, 10V, ±20% or CEUSM1A102	CC108MCAP	304A1040A1102
C66/C67	Polyester Film, CQP-92MB2A102K, 100V, 0.001μF, ±10%	CC102KLGP	306A2007K2102
C68/C69	Electrolytic, CESHM1C222, 16V, 2200μF, ±20% or CEUSM1C222	CC228MDAP	304A1040C1222
C70	Ceramic, TCC45SL1H471JYA, 50V, 470pF, ±5%	CC471JJCP	302A1024K0471
C71	Electrolytic, CESHM1V02, 35V, 1000μF, ±20% or CEUSM1V02	CC108MGAP	304A1040V1102
C72	Electrolytic, CESHM1C471, 16V, 470μF, ±20% or CEUSM1C471	CC477MDAP	304A1040C1471
C74/C75	Electrolytic, 16MS5-47M, 16V, 47μF, ±20%	CC476MDAP	304A1046C1470
C76	Electrolytic, SRC10VB-220(M), 10V, 220μF, ±20%	CC227MCAP	304A1035A1221
C77	Ceramic, FK20Y5V1H104Z, 0.1μF 50V, +80/-20% or RPE122-129F104Z50	CC104ZJCP	303A420Z3104
C78	Electrolytic, 10MS5-10M, 10V, 10μF, ±20%	CC106MCAP	304A1046A1100
C79-C84	Ceramic, FK20Y5V1H104Z, 0.1μF 50V, +80/-20% or RPE122-129F104Z50	CC104ZJCP	303A420Z3104
C87	Polyester Film, CQP-92MB2A224K, 100V, 0.22μF, ±10%	CC224KLGP	306A2007K2224
C88/C89	Ceramic, FK20Y5V1H104Z, 0.1μF 50V, +80/-20% or RPE122-129F104Z50	CC104ZJCP	303A420Z3104
C91	Ceramic, TCC45SL1H471YA, 50V, 680pF, ±5%	CC681JJCP	302A1024K0681
C93	Electrolytic, CESHM1H470, 50V, 47μF, ±20% or SMC50VB-47(M)	CC476MJAP	304A0101H1470
C94	Polyester Film, CQP-92MB2A102K, 100V, 0.001μF, ±10%	CC120KLGP	306A2007K2102
C95	Electrolytic, 25MS547M, 25V, 4.7μF, ±20%	CC475MFAP	304A1046C1479
C96	Electrolytic, CESHM1E101, 100μF, 25V, ±20% or CEUSM1E101	CC107MFAP	304A1040E1101
C97/C98	Ceramic, RPE122-127C681M50, 50V, 680P, ±20%	CC681MJCP	303A4115M3681
C99/C100	Ceramic, TCC45UJ1H101JYA, 50V, 100pF, ±5%	CC101JJCP	302A1024U0101
C105	Polyester Film, CQP-92MB2A103K, 100V, 0.01μF, ±10%	CC103KLGP	306A2007K2103
C195	Electrolytic, 10MS5-22M,10V, 22μF, ±20%	CC226MCAP	304A1046A1220
C196	Electrolytic, CESHM1A102, 1000μF, 10V, ±20% or CEUSM1A102	CC108MCAP	304A1040A1102
C197	Polyester Film, CQP-92MB2A103K, 100V, 0.01μF, ±10%	CC103KLGP	306A2007K2103

Ref. No.	Description	RS Part No.	Mfr's Part No.
C198	Electrolytic, SRC10VB-220(M), 10V, 220μF, ±20%	CC227MCAP	304A1035A1221
C199/ C200	Ceramic, TCC45SL1H330JYA, 33pF, 50V, ±10%	CC330KJCP	302A1024K0330
Check Pins			
CH 1- CH 7	Pin, Check	AJ1486	230A7090P0001
Connectors			
CN 1/ CN 2	Female, 008272244949162, 44 pins	AJ4626	224A3367P0440
CN 3	Female, 008272230949162, 30 pins	AJ4627	224A3367P0300
CN 4	For Flex Cord, ZC-016, 16 pins	AJ4630	224A3590P0160
CN 6	Male, FRC2-C26L13-ON, 26 pins	AJ4622	225A3134P0260
CN 7	Female, RDBD-25S, 25 pins	AJ4628	220A1290P0250
CN 8	Female, TCS4490-01-1011, 8 pins	AJ4629	221A1523P0081
CN 9	Male, 008263031200000, 3 pins	AJ4624	224A3357P0030
CN10	Male, FRC2-C34L13-ON, 34 pins	AJ4623	225A3134P0340
CN11	Flat Cable Connector Code, 34 pins, Female	AJ4631	3YS4011-2318P1
CN12	Male, 008263041100000, Right Angle, 4 pins	AJ4625	224A3358P0040
CN14	Jack, DCP-20	AJ1484	223A3270P0001
Variable Capacitors			
CV 1	TZ03R200ER, 100V, 4.2-20pF, +50/-0%	AC4735	315A2011E1200
CV 2	ECR-BA070M12, 250V, 7-70pF	AC4736	315A2018M3700
Diodes			
D 1-C25	Silicon, 1S953 or 1S2075, 1S2473	DX0259	611A0003L0001
D26-D29	Shot Key, Barrier, ERA81-004 or EK04	DX2638	610A0303M0004
D30/D35	Silicon, DSA1A2 or EM1Z, SM-IA-02	DX0259	610A0003M0001
D36	Varistor, ERZ-C10DK361, 360V	DX2646	632A0229M0047U
D37	Varistor, ERZ-C10DK220, 22V	DX2647	632A0229M0041
D38	Silicon, V06C	DX0506	610A0021L0071C
D40	Shot Key, Barrier, ERA81-004 or EK04	DX2638	610A0303M0004
D42/D43	Silicon, 1S953 or 1S2075, 1S2473	DX0259	611A0003L0001
Diode Arrays			
DA 1/ DA 2	DAP401, Anode, Common	DX2644	761A2027M0401
Fuse			
F 1	Glass Tube, GHS315A	AHF0001	4LP-7094-4

Ref. No.	Description	RS Part No.	Mfr's Part No.
IC			
IC 1	LSI, MHM2020, DC/DC Converter, Hybrid IC	MX6644	772A1039M0001
IC Sockets and IC Socket Housing			
ICN 1-ICN 4	IC Socket, DL2-28A-05	AJ7682	245A1155P0280
ICN 5	IC Socket Housing, 5500-28A	AJ7683	4LP-5461-1
ICs AND LSIs			
01A	LSI, HD146818P, Real Time Clock, C-MOS	MX6639	804A0021F2201
01C	IC, 74HC174, Hex D-Type Flip-Flop with Common Clock and Reset, C-MOS	MX6620	702A1756M0174
01D	IC, 74HC244, Octal 3-State Noninverting Buffer, C-MOS	MX6622	702A1756M0244
01E	IC, 74HC273, Octal D-Type Flip-Flop with Common Clock and Reset, C-MOS	MX6624	702A1756M0273
01F	LSI, MSM82C51ARS, Programmable Communication Interface, C-MOS or M82C51A	MX6637	855A0424F0032A
01R	IC, TL7700 Analog Bipolar Linear	MX2177	720A4050M0005
01S	IC, 74HC02, Quad 2-Input NAND Gates, C-MOS	MX6611	702A1756M0002
02A	IC, 74HC00, Quad 2-Input NAND Gates, C-MOS	MX6678	702A1756M0000
02H	IC, TCM1520AP, Ring Detector, BIP	MX6631	720A4050M0003
02M	IC, TL064CN, Quad OP Amp, BIP	MX6629	720A0050M0018
02Q	IC, TL7700 Analog Bipolar Linear	MX2177	720A4050M0005
02R	IC, 74HC08, Quad 2-Input AND Gate, C-MOS	MX6613	702A1756M0008
02S	IC, 74HC04, Hex Unbuffered Inverter or 74HCU04	MX6612	702A1756M0004
02T	IC, 74HC74, Dual D-Type Flip-Flop, C-MOS	MX6616	702A1756M0074
03C	IC, 74HC00, Quad 2-Input NAND Gates, C-MOS	MX6678	702A1756M0000
03D	IC, 74HC32, Quad 2-Input OR Gate, C-MOS	MX6615	702A1756M0032
03E	IC, 74HC08, Quad 2-Input AND Gate, C-MOS	MX6613	702A1756M0008
03F	IC, 74HC32, Quad 2-Input OR Gate, C-MOS	MX6615	702A1756M0032
03G	IC, 74HC374, Octal 3-State D-Type Flip-Flop, C-MOS	MX6626	702A1756M0374
03H	IC, TLP521-1-GR, Photo Coupler, BIP	MX6632	652A0125M0008

Ref. No.	Description	RS Part No.	Mfr's Part No.
03J	LSI, MSM6234RS, Dual Tone, Multi-Frequency, C-MOS or M6234	MX6641	730A2524F0001
03L/03P	IC, M54513P, Octal Transistor Array, NPN	MX6628	760A0022M0801
04A	LSI, MSM81C55RS, I/O Ports and Timer, C-MOS or M81C55	MX6636	855A0424F0028
04C	IC, 74HC04, Hex Unbuffered Inverter or 74HCU04	MX6612	702A1756M0004
04D	IC, 74HC08, Quad 2-Input AND Gate, C-MOS	MX6613	702A1756M0008
04E/04F	IC, 74HC74, Dual D-Type Flip-Flop, C-MOS	MX6616	702A1756M0074
04L	LSI, MSM6946RS, FSK-Modem, C-MOS or M6946	MX6642	730A4024F0008
05C	IC, 74HC02, Quad 2-Input NAND Gates, C-MOS	MX6611	702A1756M0002
05D	IC, 74HC32, Quad 2-Input OR Gate, C-MOS	MX6615	702A1756M0032
05E	IC, 74HC74, Dual D-Type Flip-Flop, C-MOS	MX6616	702A1756M0074
05F	IC, 74HC04, Hex Unbuffered Inverter or 74HCU04	MX6612	702A1756M0004
05G	IC, 74HC157, Quad 2-Input Data Selectors/Multiplexers, C-MOS	MX6619	702A1756M0157
05J/05K	IC, MSM4584RS, Hex Schmlet Trigger, C-MOS or M4584	MX6627	702A0124F1084E
06A	LSI, MSM82C84ARS, Clock Generator and Driver, C-MOS or M82C84A	MX6635	855A0824F0001A
06E	IC, 74HC244, Octal 3-State Noninverting Buffer, C-MOS	MX6622	702A1756M0244
06F	IC, 74HC74, Dual D-Type Flip-Flop, C-MOS	MX6616	702A1756M0074
06G/06H	IC, 74HC08, Quad 2-Input AND Gate, C-MOS	MX6613	702A1756M0008
06T	IC, 74HC244, Octal 3-State Noninverting Buffer, C-MOS	MX6622	702A1756M0244
07A	LSI, MSM80C88RS, CPU C-MOS or M80C88	MX6634	851A0124F0002
07D	IC, 74HC373, Octal D-Type Transparent Latches, with 3-State Outputs, C-MOS	MX6625	702A1756M0373
07E	IC, 74HC138, 1-of-8 Decoder/ Demultiplexer, C-MOS	MX6617	702A1756M0138
07F	IC, 74HC11, Triple 3-Input AND Gate, C-MOS	MX6614	702A1756M0011
07G	IC, 74HC32, Quad 2-Input OR Gate, C-MOS	MX6615	702A1756M0032
07H	IC, 74HC244, Octal 3-State Noninverting Buffer, C-MOS	MX6622	702A1756M0244
08D	IC, 74HC373, Octal D-Type Transparent Latches, with 3-State Outputs, C-MOS	MX6625	702A1756M0373

Ref. No.	Description	RS Part No.	Mfr's Part No.
08E	IC, 74HC139, Dual 1-of-4 Decoder, C-MOS	MX6618	702A1756M0139
08F	IC, 74HC138, 1-of-8 Decoder/ Demultiplexer, C-MOS	MX6617	702A1756M0138
08G	IC, 74HC11, Triple 3-Input AND Gate, C-MOS	MX6614	702A1756M0011
08H	IC, 74HC244, Octal 3-State Noninverting Buffer, C-MOS	MX6622	702A1756M0244
08L	IC, 74HC245, Octal 3-State Bi-directional Noninverting Buffer, C-MOC	MX6623	702A1756M0245
08N	IC, 74HC244, Octal 3-State Noninverting Buffer, C-MOS	MX6622	702A1756M0244
08P	IC, 74HC04, Hex Unbuffered Inverter or 74HCU04	MX6612	702A1756M0004
08Q	IC, 74HC74, Dual D-Type Flip-Flop, C-MOS	MX6616	702A1756M0074
08S	LSI, WD2797APL-02, FDD Controller, N-MOS	MX6643	702A6260M0001A
08T	IC, SN7404N, Hex Inverters, TTL or HD7404P, DM7404N	MX6557	700A003M0004
09A	IC, 74HC244, Octal 3-State Noninverting Buffer, C-MOS	MX6622	702A1756M0244
09B	IC, 74HC245, Octal 3-State Bi-directional Noninverting Buffer, C-MOS	MX6623	702A1756M0245
09D	IC, 74HC373, Octal D-Type Transparent Latches, with 3-State Outputs, C-MOS	MX6625	702A1756M0373
09E	IC, 74HC00, Quad 2-Input NAND Gates, C-MOS	MX6678	702A1756M0000
09F	IC, 74HC32, Quad 2-Input OR Gate, C-MOS	MX6615	702A1756M0032
09G	IC, 74HC139, Dual 1-of-4 Decoder, C-MOS	MX6618	702A1756M0139
09H	IC, 74HC138, 1-of-8 Decoder/ Demultiplexer, C-MOS	MX6617	702A1756M0138
09Q	IC, 74HC04, Hex Unbuffered Inverter or 74HCU04	MX6612	702A1756M0004
09R	IC, 74HC00, Quad 2-Input NAND Gates, C-MOS	MX6678	702A1756M0000
09T	IC, SN7404N, Hex Inverters, TTL or HD7404P, DM7404N	MX6557	700A003M0004
10E/10G 10J/10K	LSI, HM6264LP-15, Static RAM, C-MOS	MX6640	804A0021F6301
10M	IC, 74HC373, Octal D-Type Transparent Latches, with 3-State Outputs, C-MOS	MX6625	702A1756M0373
10N	LSI, μPD8257C-2, Programmable DMA Controller, N-MOS or μPD8257C-5	MX6638	855A0423F0007B
10Q	IC, 74HC138, 1-of-8 Decoder/ Demultiplexer, C-MOS	MX6617	702A1756M0138

Ref. No.	Description	RS Part No.	Mfr's Part No.
10R	IC, 74HC08, Quad 2-Input AND Gate, C-MOS	MX6613	702A1756M0008
10S	IC, 74HC157, Quad 2-Input Data Selectors/Multiplexers, C-MOS	MX6619	702A1756M0157
11A	IC, 74HC08, Quad 2-Input AND Gate, C-MOS	MX6613	702A1756M0008
11C	IC, 74HC245, Octal 3-State Bi-directional Noninverting Buffer, C-MOS	MX6623	702A1756M0245
11M	IC, 74HC374, Octal 3-State D-Type Flip-Flop, C-MOS	MX6626	702A1756M0374
11Q	IC, 74HC175, Quad D-Type Flip-Flop, C-MOS	MX6621	702A1756M0175
11S	IC, 74HC32, Quad 2-Input OR Gate, C-MOS	MX6615	702A1756M0032
Coils			
L 1	Coil, SF-5T-1501	ACA3003	4LP-45437
L 2	Coil, TSL0807-470K1R0 or TSL-0707	ACA2014	350A3004K0470
L 3	Coil, PL0406-101K	ACA3004	4LP-45494
L 4	Coil, SC-02-02G	ACA2018	350A3016P2202
OSC			
OSC 1	OSC, CX0-046C, 2 MHz	ACA3985	4LP-12184-1-C
Resistors			
R 1	HMGL1/4C4, Metal, 5.6MΩJ, 1/4W, 5%	NO541EED	326A1110J0565
R 2	NAS1/4B, Carbon, 150kΩJ, 1/4W, 5% or RD1/4S, 150kΩJ	NO384EEC	321A1421J0154
R 3	NAS1/4B, Carbon, 5.1kΩJ, 1/4W, 5% or RD1/4S, 5.1kΩJ	NO252EEC	321A1421J0512
R 5/R 7	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371EEC	321A1421J0104
R 8	NAS1/4B, Carbon, 33kΩJ, 1/4W, 5% or RD1/4S, 33kΩJ	NO324EEC	321A1421J0333
R 9/R10	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371EEC	321A1421J0104
R11/R14	NAS1/4B, Carbon, 33kΩJ, 1/4W, 5% or RD1/4S, 33kΩJ	NO324EEC	321A1421J0333
R15-R20	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371EEC	321A1421J0104
R21/R22	NAS1/4B, Carbon, 33kΩJ, 1/4W, 5% or RD1/4S, 33kΩJ	NO324EEC	321A1421J0333
R23	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371EEC	321A1421J0104
R24	NAS1/4B, Carbon, 33kΩJ, 1/4W, 5% or RD1/4S, 33kΩJ	NO324EEC	321A1421J0333

Ref. No.	Description	RS Part No.	Mfr's Part No.
R25	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371EEC	321A1421J0104
R26-R37	NAS1/4B, Carbon, 33kΩJ, 1/4W, 5% or RD1/4S, 33kΩJ	NO324EEC	321A1421J0333
R38/R39	FRD16US, Carbon, 100kΩJ, 1/6W, 5% or ELR20, 100kΩJ, 1/5W	NO371ECC	321A3412J0104
R40	NAS1/4B, Carbon, 3.3kΩJ, 1/4W, 5% or RD1/4S, 3.3kΩJ	NO230ECC	321A1421J0332
R41	FRD16US, Carbon, 390ΩJ, 1/6W, 5% or ELR20, 390ΩJ, 1/5W	NO162ECC	321A3412J0391
R42	FRD16US, Carbon, 620ΩJ, 1/6W, 5% or ELR20, 620ΩJ, 1/5W	NO181ECC	321A3412J0621
R44	FRD16US, Carbon, 27kΩJ, 1/6W, 5% or ELR20, 27kΩJ, 1/5W	NO316ECC	321A3412J0273
R45	FRD16US, Carbon, 18kΩJ, 1/6W, 5% or ELR20, 18kΩJ, 1/5W	NO303ECC	321A3412J0183
R46/R49	FRD16US, Carbon, 100kΩJ, 1/6W, 5% or ELR20, 100kΩJ, 1/5W	NO371ECC	321A3412J0104
R50-R55	FRD16US, Carbon, 33kΩJ, 1/6W, 5% or ELR20, 33kΩJ, 1/5W	NO324ECC	321A3412J0333
R56-R58	FRD16US, Carbon, 51kΩJ, 1/6W, 5% or ELR20, 51kΩJ, 1/5W	NO344ECC	321A3412J0513
R59	NAS1/4B, Carbon, 2.7kΩJ, 1/4W, 5% or RD1/4S, 2.7kΩJ	NO224EEC	321A1421J0272
R60	NAS1/4B, Carbon, 2.2kΩJ, 1/4W, 5% or RD1/4S, 2.2kΩJ	NO216EEC	321A1421J0222
R61	NAS1/4B, Carbon, 2.7kΩJ, 1/4W, 5% or RD1/4S, 2.7kΩJ	NO224EEC	321A1421J0272
R62	NAS1/4B, Carbon, 2.2kΩJ, 1/4W, 5% or RD1/4S, 2.2kΩJ	NO216EEC	321A1421J0222
R63	NAS1/4B, Carbon, 2.7kΩJ, 1/4W, 5% or RD1/4S, 2.7kΩJ	NO224EEC	321A1421J0272
R64	NAS1/4B, Carbon, 2.2kΩJ, 1/4W, 5% or RD1/4S, 2.2kΩJ	NO216EEC	321A1421J0222
R65	NAS1/4B, Carbon, 2.7kΩJ, 1/4W, 5% or RD1/4S, 2.7kΩJ	NO224EEC	321A1421J0272
R66	NAS1/4B, Carbon, 2.2kΩJ, 1/4W, 5% or RD1/4S, 2.2kΩJ	NO216EEC	321A1421J0222
R67	FRD16US, Carbon, 12kΩJ, 1/6W, 5% or ELR20, 12kΩJ, 1/5W	NO288ECC	321A3412J0123
R68	FRD16US, Carbon, 5.6kΩJ, 1/6W, 5% or ELR20, 5.6kΩJ	NO257ECC	321A3412J0562
R69	FRD16US, Carbon, 82Ω, 1/6W, 5% or ELR20, 82Ω, 1/5W	NO122ECC	321A3412J0820
R70	FRD16US, Carbon, 100kΩJ, 1/6W, 5% or ELR20, 100kΩJ, 1/5W	NO371ECC	321A3412J0104
R71	FRD16US, Carbon, 620ΩJ, 1/6W, 5% or ELR20, 620ΩJ, 1/5W	NO181ECC	321A3412J0621
R72	FRD16US, Carbon, 56kΩJ, 1/6W, 5% or ELR20, 56kΩJ, 1/5W	NO345ECC	321A3412J0563
R73/R74	FRD16US, Carbon, 100kΩJ, 1/6W, 5% or ELR20, 100kΩJ, 1/5W	NO371ECC	321A3412J0104

Ref. No.	Description	RS Part No.	Mfr's Part No.
R75	FRD16US, Carbon, 51kΩJ, 1/6W, 5% or ELR20, 51kΩJ, 1/5W	NO344ECC	321A3412J0513
R76	FRD16US, Carbon, 3.3kΩJ, 1/6W, 5% or ELR20, 3.3kΩJ, 1/5W	NO230ECC	321A3412J0332
R77	FRD16US, Carbon, 62kΩJ, 1/6W, 5% or ELR20, 62kΩJ, 1/5W	NO529ECC	321A3412J0623
R78	FRD16US, Carbon, 100kΩJ, 1/6W, 5% or ELR20, 100kΩJ, 1/5W	NO371ECC	321A3412J0104
R79	FRD16US, Carbon, 51kΩJ, 1/6W, 5% or ELR20, 51kΩJ, 1/5W	NO344ECC	321A3412J0513
R80	NAS1/4B, Carbon, 680ΩJ, 1/4W, 5% or RD1/4S, 680ΩJ	NO183EEC	321A1421J0681
R81	NAS1/4B, Carbon, 120ΩJ, 1/4W, 5% or RD1/4S, 120ΩJ	NO136EEC	321A1421J0121
R82	FRD16US, Carbon, 180ΩJ, 1/6W, 5% or ELR20, 180ΩJ, 1/5W	NO144ECC	321A3412J0181
R83	NAS1/4B, Carbon, 56ΩJ, 1/4W, 5% or RD1/4S, 56ΩJ	NO107EEC	321A1421J0560
R84/R85	NAS1/4B, Carbon, 10ΩJ, 1/4W, 5% or RD1/4S, 100ΩJ	NO063EEC	321A1421J0100
R86	FRD16US, Carbon, 56kΩJ, 1/6W, 5% or ELR20, 56kΩJ, 1/5W	NO345ECC	321A3412J0563/
R87	FRD16US, Carbon, 22kΩJ, 1/6W, 5% or ELR20, 22kΩJ, 1/5W	NO311ECC	321A3412J0223
R88/R89	FRD16US, Carbon, 6.8kΩJ, 1/6W, 5% or ELR20, 6.8kΩJ, 1/5W	NO262ECC	321A3412J0682
R90	FRD16US, Carbon, 220kΩJ, 1/6W, 5% or ELR20, 220kΩJ, 1/5W	NO396ECC	321A3412J0224
R91/ R92/R94	FRD16US, Carbon, 1.5kΩJ, 1/6W, 5% or ELR20, 1.5kΩJ, 1/5W	NO206ECC	321A3412J0152
R95	RNL1/4C3F, Metal, 100kΩF, 1/4W, 1%	NO371BED	323A1222F0104
R96	RNL1/4C3F, Metal, 15kΩF, 1/4W, 1%	NO297BED	323A1222F0153
R97	RNL1/4C3F, Metal, 100kΩF, 1/4W, 1%	NO371BED	323A1222F0104
R99	RNL1/4C3F, Metal, 6.8kΩF, 1/4W, 1%	NO262BED	323A1222F0682
R100/ R101	RNL1/4C3F, Metal, 100kΩF, 1/4W, 1%	NO371ECC	323A1222F0104
R102	FRD16US, Carbon, 390ΩJ, 1/6W, 5% or ELR20, 390ΩJ, 1/5W	NO162ECC	321A3412J0391
R103/ R104	FRD16US, Carbon, 4.7kΩJ, 1/6W, 5% or ELR20, 4.7kΩJ, 1/5W	NO247ECC	321A3412J0472
R105	FRD16US, Carbon, 6.8kΩJ, 1/6W, 5% or ELR20, 6.8kΩJ, 1/5W	NO262ECC	321A3412J0682
R107	FRD16US, Carbon, 7.5kΩJ, 1/6W, 5% or ELR20, 7.5kΩJ, 1/5W	NO266ECC	321A3412J0752
R108	FRD16US, Carbon, 12kΩJ, 1/6W, 5% or ELR20, 12kΩJ, 1/5W	NO288ECC	321A3412J0123
R109- R111	FRD16US, Carbon, 330ΩJ, 1/6W, 5% or ELR20, 330ΩJ, 1/5W	NO159ECC	321A3412J0331
R112/ R113	FRD16US, Carbon, 100ΩJ, 1/6W, 5% or ELR20, 100ΩJ, 1/5W	NO132ECC	321A3412J0101
R114	NAS1/4B, Carbon, 220ΩJ, 1/4W, 5% or RD1/4S, 1.5kΩJ	NO149EEC	321A1421J0221

Ref. No.	Description	RS Part No.	Mfr's Part No.
R115	NAS1/4B, Carbon, 1kΩJ, 1/4W, 5% or RD1/4S, 1kΩJ	NO196EEC	321A1421J0102
R116/ R117	NAS1/4B, Carbon, 5.1kΩJ, 1/4W, 5% or RD1/4S, 5.1kΩJ	NO252EEC	321A1421J0512
R118	RNL1/4C3F, Metal, 6.8kΩF, 1/4W, 1%	NO262BED	323A1222F0682
R119	FRD16US, Carbon, 51kΩJ, 1/6W, 5% or ELR20, 51kΩJ, 1/5W	NO344ECC	321A3412J0513
R120/ R121	RBD-A, Metal, 3.0ΩJ, 1/2W, 5%	NO036EFD	320A4010J0309
R122	NAS1/4B, Carbon, 150ΩJ, 1/4W, 5% or RD1/4S, 150ΩJ	NO142EEC	321A1421J0151
R123	NAS1/4B, Carbon, 100ΩJ, 1/4W, 5% or RD1/4S, 100ΩJ	NO132EEC	321A1421J0101
R124- R127	NAS1/4B, Carbon, 47ΩJ, 1/4W, 5% or RD1/4S, 470ΩJ	NO099EEC	321A1421J0470
R128/ R129	FRD16US, Carbon, 20ΩJ, 1/6W, 5% or ELR20, 200ΩJ, 1/5W	NO077ECC	321A3412J0200
R130	NAS1/4B, Carbon, 510ΩJ, 1/4W, 5% or RD1/4S, 510ΩJ	NO173EEC	321A1421J0511
R131	NAS1/4B, Carbon, 33kΩJ, 1/4W, 5% or RD1/4S, 33kΩJ	NO324EEC	321A1421J0333
R132	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371EEC	321A1421J0104
R133	NAS1/4B, Carbon, 33kΩJ, 1/4W, 5% or RD1/4S, 33kΩJ	NO324EEC	321A1421J0333
R134- R139	NAS1/4B, Carbon, 10kΩJ, 1/4W, 5% or RD1/4S, 10kΩJ	NO281EEC	321A1421J0103
R140	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371EEC	321A1421J0104
R141	FRD16US, Carbon, 390ΩJ, 1/6W, 5% or ELR20, 390ΩJ, 1/5W	NO162ECC	321A3412J0391
R142	NAS1/4B, Carbon, 820ΩJ, 1/4W, 5% or RD1/4S, 820ΩJ	NO187EEC	321A1421J0821
R143- R145	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371EEC	321A1421J0104
R147	NAS1/4B, Carbon, 33kΩJ, 1/4W, 5% or RD1/4S, 33kΩJ	NO324EEC	321A1421J0333
R148- R150	NAS1/4B, Carbon, 5.1kΩJ, 1/4W, 5% or RD1/4S, 5.1kΩJ	NO252EEC	321A1421J0512
R151	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371EEC	321A1421J0104
R152/ R153	NAS1/4B, Carbon, 10kΩJ, 1/4W, 5% or RD1/4S, 10kΩJ	NO281EEC	321A1421J0103
R154/ R155	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371EEC	321A1421J0104
R156	NAS1/4B, Carbon, 1kΩJ, 1/4W, 5% or RD1/4S, 1kΩJ	NO196EEC	321A1421J0102
R157	NAS1/4B, Carbon, 10kΩJ, 1/4W, 5% or RD1/4S, 10kΩJ	NO281EEC	321A1421J0103
R158- R160	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371EEC	321A1421J0104

Ref. No.	Description	RS Part No.	Mfr's Part No.
R161-R165	FRD16US, Carbon, 620ΩJ, 1/6W, 5% or ELR20, 620ΩJ, 1/5W	NO181ECC	321A3412J0621
R166	FRD16US, Carbon, 10kΩJ, 1/6W, 5% or ELR20, 10kΩJ, 1/5W	NO281ECC	321A3412J0103
R167/R168	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100kΩJ	NO371ECC	321A1421J0104
R169	FRD16US, Carbon, 33kΩJ, 1/6W, 5% or ELR20, 33kΩJ, 1/5W	NO324ECC	321A3412J0333
R170	FRD16US, Carbon, 56kΩJ, 1/6W, 5% or ELR20, 56kΩJ, 1/5W	NO345ECC	321A3412J0563
R171	FRD16US, Carbon, 51kΩJ, 1/6W, 5% or ELR20, 51kΩJ, 1/5W	NO344ECC	321A3412J0513
R172	FRD16US, Carbon, 24kΩJ, 1/6W, 5% or ELR20, 24kΩJ, 1/5W	NO526ECC	321A3412J0243
R174	NAS1/4B, Carbon, 100ΩJ, 1/4W, 5% or RD1/4S, 100ΩJ	NO132EEC	321A1421J0101
R175/R176	FRD16US, Carbon, 3.3kΩJ, 1/6W, 5% or ELR20, 3.3kΩJ, 1/5W	NO230ECC	321A3412J0332
R177	FRD16US, Carbon, 27kΩJ, 1/6W, 5%	NO316ECC	321A3412J0273
R178	FRD16US, Carbon, 6.8kΩJ, 1/6W, 5% or ELR20, 6.8kΩJ, 1/5W	NO262ECC	321A3412J0682
R179	FRD16US, Carbon, 1kΩJ, 1/6W, 5% or ELR20, 1kΩJ, 1/5W		321A3412J0102
Reed Relays AND Relays			
RL 1	FRL764D05/1BS-T	AR8170	4LP-7916
RL 2	FRL764D05/1AS-T	AR8169	4LP-7915
RL 3/RL 5	DS2-S, DC, 6V	AR8171	4LP-7934
Resistor Arrays			
RM 1-RM 4	RGLD8X, 333J, Metal, 33kΩ x 8, 1/8W, 5%	ARX0438	334A3224J0333
RM 5	RGLD8X, 103J, Metal, 10kΩ x 8, 1/8W, 5% or HMR8-103J-A	ARX0023	334A3224J0103
RM 6/RM 7	RGLD8X, 333J, Metal, 33kΩ x 8, 1/8W, 5%	ARX0438	334A3224J0333
RM 8	RGLD8X, 104J, Metal, 100kΩ x 8, 1/8W, 5% or RGSD8X104J	ARX0435	334A3224J0104
RM 9/RM10	RGLD8X, 333J, Metal, 33kΩ x 8, 1/8W, 5%	ARX0438	334A3224J0333
Switches			
SW 1	Slide, DIR/ACP, SSB342NS-9	AS3071	203A1023P0400
SW 2	Push, Reset, SUJ12NSNL-1	AS3070	205A1138P2000
SW 3	Slide, Memory Power, SSS342NS-4	AS3072	203A1044P0400
Pins			
T 1/T 2	Pin, Short, Z-149A-3P	AJ1485	224A3186P0030

Ref. No.	Description	RS Part No.	Mfr's Part No.
Transformers			
TLA 1	Switching Power Supply	ATA1072	4LP-45476
TLA 2	Driver Transformer	ATB0510	4LP-45438
Transistors			
TR 1	2SC2719-K/L NPN-HF-TR	2SC2719L	602A1123M0046
TR 2	2SC641K, NPN-HF-TR	2SC641K	602A1021M0022
TR 3/ TR 4	2SA768, PNP	2SA768	600A1226M0026
TR 5	2SD789, NPN-LF-TR	2SD789	603A1121M0006
TR 6	2SC3345 NPN-HF-TR or 2SC3345, 2SC3346	2SC3157L	602A1225F0037
TR 7	2SA1152-K/L PNP-HF-TR	2SA1152L	600A1123M0015
TR 8	2SB858-C PNP-LF-TR	2SB858C	601A1221M0013C
TR 9	2SB562-C PNP-LF-TR	2SB562C	601A1121M0002C
TR10	2SD468-C NPN-LF-TR	2SD468C	603A1121M0003C
TR11	2SA1152-K/L PNP-HF-TR	2SA1152L	600A1123M0015
Potentiometers			
VR 2	Metal ET-6P10kΩ, B Type 10kΩ	AP7437	331A2005B0103
VR 3	Metal ET-6P50kΩ, B Type, 50kΩ	AP7438	331A2005B0503
VR 4	Carbon, K111B0002-20KB, B Type, 20kΩ	AP7439	332A2021B0203
Crystals			
X 1	P-5, 32.768 kHz	MX0076	380A1202A0001
X 2	HC18/U 9.216 MHz	MX0077	380A1170B7001
X 3/X 4	PX-1 3579.545 kHz	MX0078	380A1203B0001
Diodes			
ZD 1/ ZD 2	Zener, RD4.3E-B, 4.3V	DX2593	613A1231L0092
ZD 3	Zener, RD3.0E-B, 3.0V	DX1541	613A1231L0052
ZD 4	Zener, RD6.2E-B, 6.2V	DX0501	613A1231L0132
ZD 5	Zener, RD5.6E-B, 5.6V	DX0735	613A1231L0122
ZD 6	Zener, RD2.7E-B, 2.7V	DX1680	613A1231L0042
ZD 7	Zener, RD10E-B3, 10V	DX0090	613A1231L0182C
ZD 8	Zener, RD2.7E-B, 2.7V	DX1680	613A1231L0042
ZD 9	Zener, RD6.2E-B2, 6.2V	DX0089	613A1231L0132B
ZD10	Zener, RD4.7E-B, 4.7V		613A1231L0102

Ref. No.	Description	RS Part No.	Mfr's Part No.
Miscellaneous			
P-20	Heat Sink		4PP3516-1034P001
P-21	Insulator for CXO-046C		4LR-194115-2
P-22	Knob, Variable Resistor	AK5732	4PB4020-5072P1
P-23	OSC Holder		5LK-50311
P-24	Plug, Short, Z-128A	AJ7684	224A3185P0020
S- 6	Screw, Machine, Braizer with Spring Washer, 3 x 8	AHD0013	⊕ P(SW)3-8-HHC
S- 7	Screw, Machine, Braizer with Spring Washer & Double Size Washer, 3 x 8	AHD0040	⊕ P(SW+2W)3-8-HH
S- 8	Screw, Machine, Braizer with Spring Washer & Washer 3 x 8	AHD0041	⊕ P(SW+W)3-8-HHC

KEYBOARD UNIT ASSEMBLY
[KEYBOARD PCB ASSEMBLY (OPKK Board)]

Ref. No.	Description	RS Part No.	Mfr's Part No.
Capacitors			
K-C 1- K-C 7	Ceramic, FK20Y5V1H104Z, 0.1µF, 50V, +80/-20% or RPE122-129F104Z50	CC104ZJCP	303A0420Z3104
Connector			
K-CN 1	CF116A for Flex Cord, 16 pins	AJ4621	224A3592P0160
Diodes			
K-D 1/ K-D 2	Silicon, 1S953 or IS2075, IS2473	DX0259	611A0003L0001
LED			
K-LED 1	LED, GL-3PR1, LED	AL1490	650A0128M0003
ICs			
K-Q 1	MC74HC42N BCD to 1-of-10 Decoder C-MOS	MX6608	702A1756M0042
K-Q 2/ K-Q 3	MSM4051RS, 8 ch Multiplexer/ Demultiplexer, C-MOS or M4051	MX6609	731A0524F1001E
K-Q 4	µPC271C Comparator, BIP	MX6610	720A0523F0003
K-Q 5	MC74HC00N Quad 2-Input NAND Gate, C-MOS	MX6678	702A1756M0000
Resistors			
K-R 1	NAS1/4B, Carbon, 510ΩJ, 1/4W, 5% or RD1/4S, 510Ω		321A1421J0511
K-R 2	RNL1/4C3F, Metal, 10kΩF, 1/4W, 1%	NO281BED	323A1222F0103
K-R 3	RNL1/4C3F, Metal, 13kΩF, 1/4W, 1%	NO289BED	323A1222F0133
K-R 4	NAS1/4B, Carbon, 100kΩJ, 1/4W, 5% or RD1/4S, 100k	NO371EEC	321A1421J0104
K-R 5	RNL1/4C3F, Metal, 1.5kΩF, 1/4W, 1%	NO206BED	323A1222F0152
K-R 6	RNL1/4C3F, Metal, 1.3kΩF, 1/4W, 1%	NO202BED	323A1222F0132
K-R 7	NAS1/4B, Carbon, 820ΩJ, 1/4W, 5% or RD1/4S, 820Ω	NO187EEC	321A1421J0821

Ref. No.	Description	RS Part No.	Mfr's Part No.
Resistor Arrays			
K-RM 1	RGLD8X512J 5.1kΩ x 8, 1/8W, 5% or RGSD8X512J	ARX0434	334A3224J0512
K-RM 2	RGLD8X104J 100kΩ x 8, 1/8W, 5% or RGSD8X104J	ARX0435	334A3224J0104
K-RM 3	RGLD8X332J 3.3kΩ x 8, 1/8W, 5% or RGSD8X332J	ARX0436	334A3224J0332
K-RM 4	RGLD8X104J 100kΩ x 8, 1/8W, 5% or RGSD8X104J	ARX0435	334A3224J0104
Switches			
K-SW 1-K-SW16	Function Key, SHM-13	AS7582	3LK-50711-1
K-SW17	Push, Power on/off, KHE 10901	AS7581	205A1134P2000
Miscellaneous			
P-13	Collar, LED, 6 mm	ART5631	5LM-13967-6

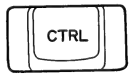
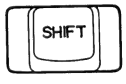
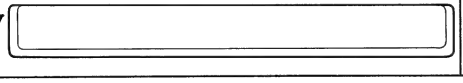
KEYBOARD UNIT ASSEMBLY
[KEYBOARD MAINTENANCE KIT]

Ref. No.	Description	RS Part No.	Mfr's Part No.
Miscellaneous			
A-101-A-156	Ass'y, Key Lever	ART5626	4PA4014-1045G1
A-160	Ass'y, Arm Bar, Enter Key	ART0094	4PA4014-1013G5
A-161	Ass'y, Arm Bar, Space Key	ART0093	4PA4014-1013G1
P-14	Key Switch Base	ART5625	2PB4014-1115P1
P-15	Cable, Keyboard connection	AW3296	4LP-5463-2
P-101-P-155	Reset Spring, Capacitive Key Switch	ARB7774	4LK-52027
P-160	Lever, Key Guide, Enter	ART5627	4LK-52012
P-161	Lever, Key Guide Space	ART5628	4LK-52013
P-162	Spring, Space Key	ARB7775	4LK-52028
P-163	Tape, Double-Sided		NITTO#501W5L270
S- 2	Screw, Tap Tight, Braizer, 2.35 x 5	AHD2975	4LP-7122
S- 3	Screw, Machine,Braizer with Spring Washer & Double Size Washer, 3 x 8	AHD1873	⊕ P(SW+2W)3-8-HHC
Key Tops			
K- 1	Key Top, POWER	AK5730	3PK4014-1148G1
K-2- 1	Key Top, BREAK / PAUSE	AK5731	3LK-52266-F
K-2- 2	Key Top, PRINT	AK5731	3LK-52266-F
K-2- 3	Key Top, F1	AK5731	3LK-52266-F
K-2- 4	Key Top, F2	AK5731	3LK-52266-F
K-2- 5	Key Top, F3	AK5731	3LK-52266-F
K-2- 6	Key Top, F4	AK5731	3LK-52266-F
K-2- 7	Key Top, F5	AK5731	3LK-52266-F
K-2- 8	Key Top, F6	AK5731	3LK-52266-F

Ref. No.	Description	RS Part No.	Mfr's Part No.
K-2- 9	Key Top, 	AK5731	3LK-52266-F
K-2-10	Key Top, 	AK5731	3LK-52266-F
K-2-11	Key Top, 	AK5731	3LK-52266-F
K-2-12	Key Top, 	AK5731	3LK-52266-F
K-2-13	Key Top, 	AK5731	3LK-52266-F
K-2-14	Key Top, 	AK5731	3LK-52266-F
K-2-15	Key Top, 	AK5731	3LK-52266-F
K-2-16	Key Top, 	AK5731	3LK-52266-F
K- 3	Key Top, 	AK5672	3LK-52049-133-D1
K- 4	Key Top, 	AK5673	3LK-52049-134-D1
K- 5	Key Top, 	AK5674	3LK-52049-135-D1
K- 6	Key Top, 	AK5675	3LK-52049-136-D1
K- 7	Key Top, 	AK5676	3LK-52049-137-D1
K- 8	Key Top, 	AK5677	3LK-52049-138-D1
K- 9	Key Top, 	AK5678	3LK-52049-139-D1
K-10	Key Top, 	AK5679	3LK-52049-140-D1
K-11	Key Top, 	AK5680	3LK-52049-141-D1

Ref. No.	Description	RS Part No.	Mfr's Part No.
K-12	Key Top, 	AK5681	3LK-52049-142-D1
K-13	Key Top, 	AK5682	3LK-52049-143-D1
K-14	Key Top, 	AK5683	3LK-52049-144-D1
K-15	Key Top, 	AK5684	3LK-52049-145-D1
K-16	Key Top, 	AK5685	3LK-52049-146-D1
K-17	Key Top, 	AK5686	3LK-52045-116-D1
K-18	Key Top, 	AK5687	3LK-52045-117-D1
K-19	Key Top, 	AK5688	3LK-52045-118-D1
K-20	Key Top, 	AK5689	3LK-52045-119-D1
K-21	Key Top, 	AK5690	3LK-52045-120-D1
K-22	Key Top, 	AK5691	3LK-52045-121-D1
K-23	Key Top, 	AK5692	3LK-52045-122-D1
K-24	Key Top, 	AK5693	3LK-52045-123-D1
K-25	Key Top, 	AK5694	3LK-52045-124-D1
K-26	Key Top, 	AK5695	3LK-52045-125-D1
K-27	Key Top, 	AK5696	3LK-52045-126-D1
K-28	Key Top, 	AK5697	3LK-52031-431-D1

Ref. No.	Description	RS Part No.	Mfr's Part No.
K-29	Key Top, 	AK5698	3LK-52031-432-D1
K-30	Key Top, 	AK5699	3LK-52031-433-D1
K-31	Key Top, 	AK5700	3LK-52031-434-D1
K-32	Key Top, 	AK5701	3LK-52031-435-D1
K-33	Key Top, 	AK5702	3LK-52031-436-D1
K-34	Key Top, 	AK5703	3LK-52031-437-D1
K-35	Key Top, 	AK5704	3LK-52031-438-D1
K-36	Key Top, 	AK5705	3LK-52031-439-D1
K-37	Key Top, 	Ak5706	3LK-52031-440-D1
K-38	Key Top, 	AK5707	3LK-52031-441-D1
K-39	Key Top, 	AK5708	3LK-52035-100-D1
K-40	Key Top, 	AK5709	3LK-52035-101-D1
K-41	Key Top, 	AK5710	3LK-52035-102-D1
K-42	Key Top, 	AK5711	3LK-52035-103-D1
K-43	Key Top, 	AK5712	3LK-52035-104-D1
K-44	Key Top, 	AK5713	3LK-52035-105-D1
K-45	Key Top, 	AK5714	3LK-52035-106-D1

Ref. No.	Description	RS Part No.	Mfr's Part No.
K-46	Key Top, 	AK5715	3LK-52035-107-D1
K-47	Key Top, 	AK5716	3LK-52035-108-D1
K-48	Key Top, 	AK5717	3LK-52035-109-D1
K-49	Key Top, 	AK5718	3LK-52035-110-D1
K-50	Key Top, 	AK5719	3LK-52031-442-D1
K-51	Key Top, 	AK5720	3LK-52031-443-D1
K-52	Key Top, 	AK5721	3LK-52031-444-D1
K-53	Key Top, 	AK5722	3LK-52077-26-D1
K-54	Key Top, 	AK5723	3LK-52120-9-D1
K-55	Key Top, 	AK5724	3LK-52277-6-D1
K-56	Key Top,  Left	AK5725	3LK-52061-6-D1
K-57	Key Top,  Right	AK5726	3LK-52085-11-D1
K-58	Space Key 	AK5727	2LK-52123-D
SWITCHES			
K-SW1-K-SW16	Switch, Function Key, SHM-13	AS7582	3LK-50711-1

LCD CONTROLLER PCB ASSEMBLY (OPLF Board)

Ref. No.	Description	RS Part No.	Mfr's Part No.
Capacitors			
L-C 1- L-C 5	Ceramic, FK20Y5V1H104Z, 0.1µF, 50V, +80/-20% or RPE122-129F104Z50 FK20Y5V1H104Z	CC104ZJCP	303A0420Z3104
Connectors			
L-CN 1	Male, 008272230001162, 30 pins	AJ4632	224A3368P0300
L-CN 2	Male, 008263121200000, 12 pins	AJ4633	224A3357P120
ICs AND LSIs			
L-01C	LSI, HM6264LP-15, Static, RAM, C-MOS	MX6640	804A0021F6301
L-02A	IC, 74HC74, Dual D-Type Flip-Flop, C-MOS	MX6616	702A1756M0074
L-02C/ L-03C	LSI, HD61830, LCD Controller, C-MOS	MX6645	855A0421F0038
L-04C	LSI, HM6264LP-15, Static, RAM, C-MOS	MX6640	804A0021F6301
L-05A	IC, 74HC00, Quad 2-Input NAND Gates, C-MOS	MX6616	702A1756M0000
L-05B	IC, 74HC386, 2-INPUT EXCLUSIVEOR, C-MOS	MX6678	702A1721M0386
L-05C	IC, 74HC390, DECADE COUNTERS, C-MOS		702A1721M0390
Resistor			
L-R 1	NAS1/4U, 100kΩJ, 1/4W, 5%	NO371EEC	R4LP-8621-104

FDD PCB ASSEMBLY

Ref. No.	Description	RS Part No.	Mfr's Part No.
Resistor Array			
F-BR 1	M08-1-R10K, Carbon, 10kΩ x 7, 0.125W, 10%	RX0005	SM08-1-R10K
Capacitors			
F-C 1- F-C 3	Laminated Ceramic, 25V, 0.1μF, +80, -20%	CC104ZFCP	SD33Y5V1E104
F-C 4/ F-C 5	Ceramic, 50V, 470PF, ±5% or ±10%	CC471KJCP	SRXU-04B471K
F-C 6	Ceramic, 50V, 1500PF, ±5% or ±10%	CC152KJCP	SRXU-05B152K
F-C 7	Ceramic, 50V, 1000PF, ±5% or ±10%	CC102JJCP	SUAT04X102K
F-C 9/ F-C10	Ceramic, 50V, 330PF, ±5% or ±10%	CC331KJCP	SROU04B331K
F-C12/ F-C15	Tantalum Electrolytic, 35V, 1μF, ±20%	CC105KGTP	SDN1V010M1S
F-C16/ F-C20	Tantalum Electrolytic, 35V, 0.15μF, ±20%	CC154MGTP	SDN1VR15M1S
F-C21	Ceramic, 16V, 0.047μF, +80/-20%	CC473ZDCP	SRXE06D473M
F-C30	Tantalum Electrolytic, 35V, 1μF, ±20%	CC105KGTP	SDN1V010M1S
F-C32- F-C34	Ceramic, 16V, 0.047μF, +80/-20%	CC473ZDCP	SRXE-06D473Z
F-C36	Electrolytic, 16V, 22μF, ±20%	CC226MDAP	S16MS5-22
F-C37	Ceramic, 16V, 0.047μF, +80/-20%	CC473ZDCP	SRXE-06D473Z
F-C38	Electrolytic, 16V, 22μF, ±20%	CC226MDAP	S16MS5-22
F-C39	Ceramic, 16V, 0.047μF, +80/-20%	CC473ZDCP	SRXE-06D473Z
F-C40	Mylar* Film 6.3V, 0.047μF, ±10%	CC473KBMP	SMMH473K63
F-C41	Ceramic, 16V, 0.047μF, +80/-20%	CC473ZDCP	SRXE-06D473Z
F-C42	Ceramic, 50V, 33PF, ±5% or ±10%	CC330JJCP	SRAU04SL330J
F-C43	Ceramic, 16V, 0.047μF, +80/-20%	CC473ZDCP	SRXE-06D473Z
F-C44	Tantalum Electrolytic, 16V, 4.7μF, ±20%	CC475MDTP	SDN1C4R7M1S
Connectors			
F-CON 1	BCP209434, Male, 34 pins or PS34PED4LT1PN1	AJ0003	SBCP209434
F-CON 2	BCP209304, Male, 4 pins or 171826-4	AJ0004	SBCP209304
F-CON 3	BCP203405, Male, 5 pins or 65532-405	AJ0005	SBCP203405
F-CON 4/ F-CON 5	BCP202304, Male, 4 pins or ILG-4P-S3T2E	AJ0006	SBCP202304
F-CON 6	BCP202306, Male, 6 pins or ILG-6P-S3T2E	AJ0007	SBCP202306

* Mylar is a registered trademark of E.I.Du Pont de Nemours and Company.

Ref. No.	Description	RS Part No.	Mfr's Part No.
Oscillator			
F-CSC 1	Ceramic, KMFC1001T, 3.58 MHz	CA0012	SKMFC1001T
Diodes			
F-D 1- F-D10	Silicon, 1SS-176	DX2331	S1SS-176
Diode Arrays			
F-DA 1- F-DA 6	MA154WK, Cathode, Common	DX2597	SMA154WK
ICs			
F-IC 1	HA16642NT, Read Write	MX2022	SHA16642NT
F-IC 2	µPD1514C, N channel, N-MOS, 4 Bit CPU	MX2023	SµPD1514C
F-IC 3/ F-IC 4	MB3763P, Motor Drive	MX2024	SMB3763P
F-IC 5	TC4023BP, Triple 3-Input, NAND Gates, C-MOS or MC14023B	MX2039	STC4023BP
F-IC 6	HD-74LS14P, Hex Schmitt Trigger Inverters or SN74LS14N	MX2040	SHD74LS14P
F-IC 7	HD-14584BP or MC14584B, Schmitt Trigger Inverters, C-MOS	MX2041	SHD14584BP
F-IC 8	HD-7438P, Quand 2-Input NAND Buffer (Open-Collector) or SN7438N	MX2042	SHD7438P
F-IC 9	74LS08P, Quand 2-Input AND Gates or SN74LS08N	MX2043	SHD74LS08P
Coils and Inductors			
F-L 1/ F-L 2	Coil LAL03KH391K 390µH ±10%	CA0013	SLAL03KH391K
F-L 3	Inductor, 330µH	CA0015	SLAL03KH331K
F-L 4	Inductor, LAL04-NA101K, 100µH ±10%	CA0014	SLAL04NA101K
LED			
F-LED 1	Red, GL-9PR2	L1374	SGL-9PR2
Resistor Array			
F-MR	M09-1-R1K, Carbon, 1kΩ x 8, 0.125W, 10%	RX0004	SM09-1-R1K
Sensor			
F-PT 1	Photo-Micro, EE-SJ3WB	ACS0001	SEE-SJ3-WB

Ref. No.	Description	RS Part No.	Mfr's Part No.
Resistors			
F-R 1/ F-R 2	RD16SM-33K, Carbon, 33kΩ, 0.16W, 5%	NO324EAC	SRD16SM-33K
F-R 3/ F-R 4	RD16SM-4.7K, Carbon, 4.7kΩ, 0.16W, 5%	NO247EAC	SRD16SM-4.7K
F-R 5/ F-R 6	RD16SM-470, Carbon, 470Ω, 0.16W, 5%	NO169EAC	SRD16SM-470
F-R 7	RD16SM-2.2K, Carbon, 2.2kΩ, 0.16W, 5%	NO216EAC	SRD16SM-2.2K
F-R14	RD16SM-10K, Carbon, 10kΩ, 0.16W, 5%	NO281EAC	SRD16SM-10K
F-R15	RD16SM-4.7K, Carbon, 4.7kΩ, 0.16W, 5%	NO247EAC	SRD16SM-4.7K
F-R16	RD16SM-6.8K, Carbon, 6.8kΩ, 0.16W, 5%	NO262EAC	SRD16SM-6.8K
F-R17	RD25S-330, Carbon, 330Ω, 0.16W, 5%	NO159EAC	SRD25S-330
F-R20	RD16SM-22K, Carbon, 22kΩ, 0.16W, 5%		SRD16SM-22K
F-R21/ F-R22	RD16SM-1K, Carbon, 1kΩ, 0.16W, 5%	NO196EAC	SRD16SM-1K
F-R23	RD16SM-10K, Carbon, 10kΩ, 0.16W, 5%	NO281EAC	SRD16SM-10K
F-R24/ F-R25	RD16SM-4.7K, Carbon, 4.7kΩ, 0.16W, 5%	NO247EAC	SRD16SM-4.7K
F-R30	RD16SM-22K, Carbon, 22kΩ, 0.16W, 5%		SRD16SM-22K
F-R31	RD16SM-100K, Carbon, 100kΩ, 0.16W, 5%	NO371EAC	SRD16SM-100K
F-R32	RD16SM-22K, Carbon, 22kΩ, 0.16W, 5%		SRD16SM-22K
F-R33	RD16SM-1K, Carbon, 1kΩ, 0.16W, 5%	NO196EAC	SRD16SM-1K
F-R34	RD16SM-10K, Carbon, 10kΩ, 0.16W, 5%	NO281EAC	SRD16SM-10K
F-R35	RD16SM-470, Carbon, 470Ω, 0.16W, 5%	NO169EAC	SRD16SM-470
F-R36	RD16SM-470K, Carbon, 470kΩ, 0.16W, 5%	NO423EAC	SRD16SM-470K
F-R37	RD16SM-2.2K, Carbon, 2.2kΩ, 0.16W, 5%	NO216EAC	SRD16SM-2.2K
F-R38	RD16SM-470, Carbon, 470Ω, 0.16W, 5%	NO169EAC	SRD16SM-470
F-R39	RD16SM-200K, Carbon, 220kΩ, 0.16W, 5%	NO396EAC	SRD16SM-220K
F-R40	RD16SM-10K, Carbon, 10kΩ, 0.16W, 5%	NO281EAC	SRD16SM-10K
F-R41	RD16SM-4.7K, Carbon, 4.7kΩ, 0.16W, 5%	NO247EAC	SRD16SM-4.7K
F-R42	RD16SM-2.2K, Carbon, 2.2kΩ, 0.16W, 5%	NO216EAC	SRD16SM-2.2K
F-R43	RD16SM-10K, Carbon, 10kΩ, 0.16W, 5%	NO281EAC	SRD16SM-10K
F-R44	RD16SM-470, Carbon, 470Ω, 0.16W, 5%	NO169EAC	SRD16SM-470
F-R45	RD16SM-10K, Carbon, 10kΩ, 0.16W, 5%	NO281EAC	SRD16SM-10K
F-R46	RD16SM-470, Carbon, 470Ω, 0.16W, 5%	NO169EAC	SRD16SM-470

Ref. No.	Description	RS Part No.	Mfr's Part No.
F-R50	RD16SM-100K, Carbon, 100kΩ, 0.16W, 5%	NO371EAC	SRD16SM-100K
F-R64	RD16SM-22K, Carbon, 22kΩ, 0.16W, 5%		SRD16SM-22K
F-R72	RD16SM-2.2K, Carbon, 2.2kΩ, 0.16W, 5%	NO216EAC	SRD16SM-2.2K
F-R80/ F-R81/ F-R83/ F-R90	RD16SM-22K, Carbon, 22kΩ, 0.16W, 5%		SRD16SM-22K
F-R91	RD16SM-100K, Carbon, 100kΩ, 0.16W, 5%	NO371EAC	SRD16SM-100K
F-R93	RD16SM-10K, Carbon, 10kΩ, 0.16W, 5%	NO281EAC	SRD16SM-10K
Dip Switch			
F-SW 1	BSD200504, Device Select or PSS704	AS0003	SBSD200504
Connectors			
F-TPA	BCP208105, Male, 5 pins or IMSA9202B-1-5T	AJ0009	SBCP208105
F-TPB	BCP208103, Male, 3 pins or IMSA9202B-1-3T	AJ0008	SBCP208103
Test Pin			
F-TPG	Pin, Test, MRAMC002701		SMRAMC002701
Transistors			
F-TR 2	DTC114, NPN TR Resistor Include or UN1211	MX2053	SDTC114
F-TR 3- F-TR 7	2SB790, PNP TR	2SB790	S2SB790Q,S
F-TR 8	DTA114, PNP TR Resistor Include or UN1111	MX2050	SDTA114
F-TR 9	2SD636R, NPN TR	2SD636R	S2SD636RQ,S
Rsistors			
F-VR 1/ F-VR 2	Semi-Fixed, GF06P50K, Carbon, 50kΩ, 0.5W, B Type, 50kΩ	AD0001	SGF06P50K
Miscellaneous			
F-25	Guide, Lead Wire	ART0004	SMYA201701
F-26	Insulating Plate		SBVS200601

LCD UNIT ASSEMBLY

Ref. No.	Description	RS Part No.	Mfr's Part No.
Capacitors			
LU-C 1	Tantalum, 10V, 15μF, ±20%	CC156MCTP	H20531150
LU-C 2	Tantalum, 50V, 3.3μF, ±20%	CC335MJTP	H20535033
Diodes			
LU-D 1/ LU-D 2	Silicon, IS2348	DX2633	H27101100
ICs			
LU-IC 1/ LU-IC 2	HD61103, 100 pin, Common Driver, C-MOS	MX2019	H28420086
LU-IC 3- LU-IC14	HD61100, 100 pin, Segment Driver, C-MOS	MX2020	H28420087
LU-IC15	HA17902MP, Ope. AMP., Linear IC	MX2021	H28420028
Resistors			
LU-R 1- LU-R 4	Metal, 3kΩ, 1/8W, ±1%	NO224BBD	H19531302
LU-R 5	Metal, 9.1kΩ, 1/8W, ±1%	NO276BBD	H19531912
LU-R 6- LU-R11	Metal, 15Ω, 1/8W, ±1%	NO074BBD	H19531150
Transistor			
LU-TR 1	2SA673APKC, PNP	2SA673A	H27207072
Miscellaneous			
P-38	Connector, Male, 12 pins	AJ0001	224A3358P0120

MECHANICAL AND ASSEMBLY PARTS

Ref. No.	Description	RS Part No.	Mfr's Part No.
A- 1	Upper Cover w/Nameplate	AZ7224	2PA4016-2018G1
A- 2	Top Cover Kit	AZ7225	4YA3516-1089G1
A- 3	LCD Cover Kit	AZ7226	4YA3516-1090G1
A- 4	Ass'y, LCD Unit	AXX0242	4YB4060-4002P1
A- 5	Cable, LCD Connection	AW3295	3YS4011-4643G1
A- 6	Fulcrum Bracket Kit		4YA3516-1092G1
A- 8	Ass'y, Keyboard Unit		2YX4014-1113G1
A- 9	PCB Ass'y, Keyboard	AX9524	2YU5006-1021G1
A-10	Key Top (56 Keys)		4YB4014-1131G1
A-11	Lower Cover Kit	AZ7228	4YA3516-1091G1
A-12	Cable, FDD Power	AW3297	4YS4011-4640G1
A-13	PCB Ass'y, Main	AX9525	2YU5003-4004G1
A-14	PCB Ass'y, LCD Controller	AX9526	4YA3516-1048G1
A-15	Ass'y, FDD Unit		4YA4030-1011G1
A-16	Ass'y, IC Carrier		4YX3516-1054G1
A-20	Keyboard Maintenance Kit		4YA3516-1087G1
F- 1	Case, Shield		SMBB212801
F- 2	Ass'y - Front Bezel	AZ0006	SSBM045601
F- 3	PCB Ass'y, FDD	AXX5047	SSBP018605
F- 4	Button, Eject	AK2097	SMYB219001
F- 5	Ass'y - Spindle Motor	AM0001	SSBE017601
F- 6	Lever, Write-protect	ART0005	SMYB225801
F- 7	Spring, Leaf, Write-protect Lever	ARB0001	SMBA223101
F- 8	Stepping Motor, MSHD200A71	AM0002	SBMP200801
F- 9	Snap, Stepping Motor	AHC0008	SMFA213101
F-10	Guide Plate, A, Carriage M		SMBF211801
F-11	*Ass'y, Carriage, Head seek		SSWB001803
F-12	*Shaft, Long, Head seek		SMRF207801
F-13	*Shaft, Short, Head seek		SMRF207901
F-14	Snap, Shaft		SMBA222701
F-15	Belt, Head Carriage	AB0001	SMFB203701
F-16	Fitting, Belt	AHC0009	SMBA226202
F-17	Stopper Plate, Stepping Motor	ART0006	SMFA213602
F-18	Sensor, TR00 Position	ACS0002	SSBE018001
F-19	Lever E, Eject		SMBB214401
F-20	Carriage M, Disk Guide		SSBM054201
F-21	Ass'y - Damper, Disk Drop Shock Absorber		SSBM032701
F-22	Ass'y - Guide Plate B, Carriage M		SSBM032101
F-23	Spring, Coil, Carriage M		SMST204002
F-24	*Ass'y, Frame		SSBM032401
F-51	Screw, M3 x 6, Flat Head	AHD0003	SKSC13006010
F-52	Screw, M2.5 x 6, Binding Head	AHD0004	SKSB12506010
F-53	Screw, M2.5 x 4, with SW, Pan Head	AHD0005	SKDP12250410

Note: * shows the part not included in the whole Parts List.

Ref. No.	Description	RS Part No.	Mfr's Part No.
F-54	Screw, M2.5 x 6, with SW, Pan Head	AHD0006	SKDP12250610
F-55	Screw, M2.6 x 6, with SW, Pan Head	AHD0007	SKDP12606012
F-56	Screw, M2.5 x 6, with SW+W, Pan Head	AHD0008	SKDP82250625
F-57	Screw, M3 x 8, with SW, Pan Head	AHD0009	SKDP12300810
P- 1	LCD Cover	AHC3165	3PP4020-5051G1
P- 2	Holder, LCD Cable	AHC3166	4PP4020-5054P1
P- 3	Cover, LCD Cable	AZ7227	4PB4020-5055P1
P- 4	Cushion, LCD Unit Up/Down		4LM-13685-125
P- 5	Cushion, LCD Unit Right/Left		4LM-13685-126
P- 6	Spring, Cable Protection	ARB0002	4LB-192700-7
P- 7	*Button Holder		3PB4020-5058P1
P- 7-1	*Lock Button (R)		03PB4020-5056P1
P- 7-2	*Lock Button (L)		03PB4020-5057P1
P- 8	Battery Mounting Plate		4PP4020-5059P1
P- 9	Tube, Transparent, Vinyl, Spring Cover		ϕ5 = 29
P-10	E-Ring, LCD Hinge		RE4-SK
P-11	Fulcrum Shaft, LCD Hinge		4PP4020-5060P1
P-12	Battery Pack		4YB3516-1027G1
P-16	Lower Cover	AZ7229	2PB4020-5065P1
P-17	ROM Cover	ART5629	3PB4020-5066P1
P-18	FDD Mounting Plate		4PP4020-5068P1
P-19	Rubber Foot, Bottom Case	AF0378	4PB4018-1883P1
P-25	Connector Cover, FDD	AHC3168	4PB4020-5069P1
P-26	Connector Cover, Printer	AHC3169	4PB4020-5070P1
P-27	Adapter	AW3298	4YB4049-1028P1
P-31	Label, User ID		4PB4012-5080P1
P-32	ROM, Mask, HN613256PS66, 256K	MX3339	817A8322F0166
P-33	ROM, Mask, HN613256PS67, 256K	MX3342	817A8322F0167
P-34	ROM, Mask, HN613256PS68, 256K	MX3343	817A8322F0168
P-35	ROM, Mask, HN613256PS98, 256K	MX3344	817A8322F0198
P-36	ROM, Mask, HN613256PS99, 256K	MX3322	817A8322F0199
P-37	Carrier, IC Chip	MX3323	4LP-5461-2
S- 1	Screw, Machine, Braizer with Spring Washer & Washer, 3 x 8	AHD0012	⊕ P(SW+W)3-8-HHC
S- 4/ S- 5	Screw, Machine, Braizer with Spring Washer & Double Size Washer, 3 x 8		⊕ P(SW+2W)3-8-HHC
S- 9	Screw, Machine, Braizer with Spring Washer & Double Size Washer, 3 x 10		⊕ P(SW+2W)3-10-HHC
S-10	Hardware Kit	AHW2603901	4YA3516-1088G1

Section 8
CIRCUIT DIAGRAMS

SECTION 8 – – CIRCUIT DIAGRAMS

8.1 Circuit Diagrams

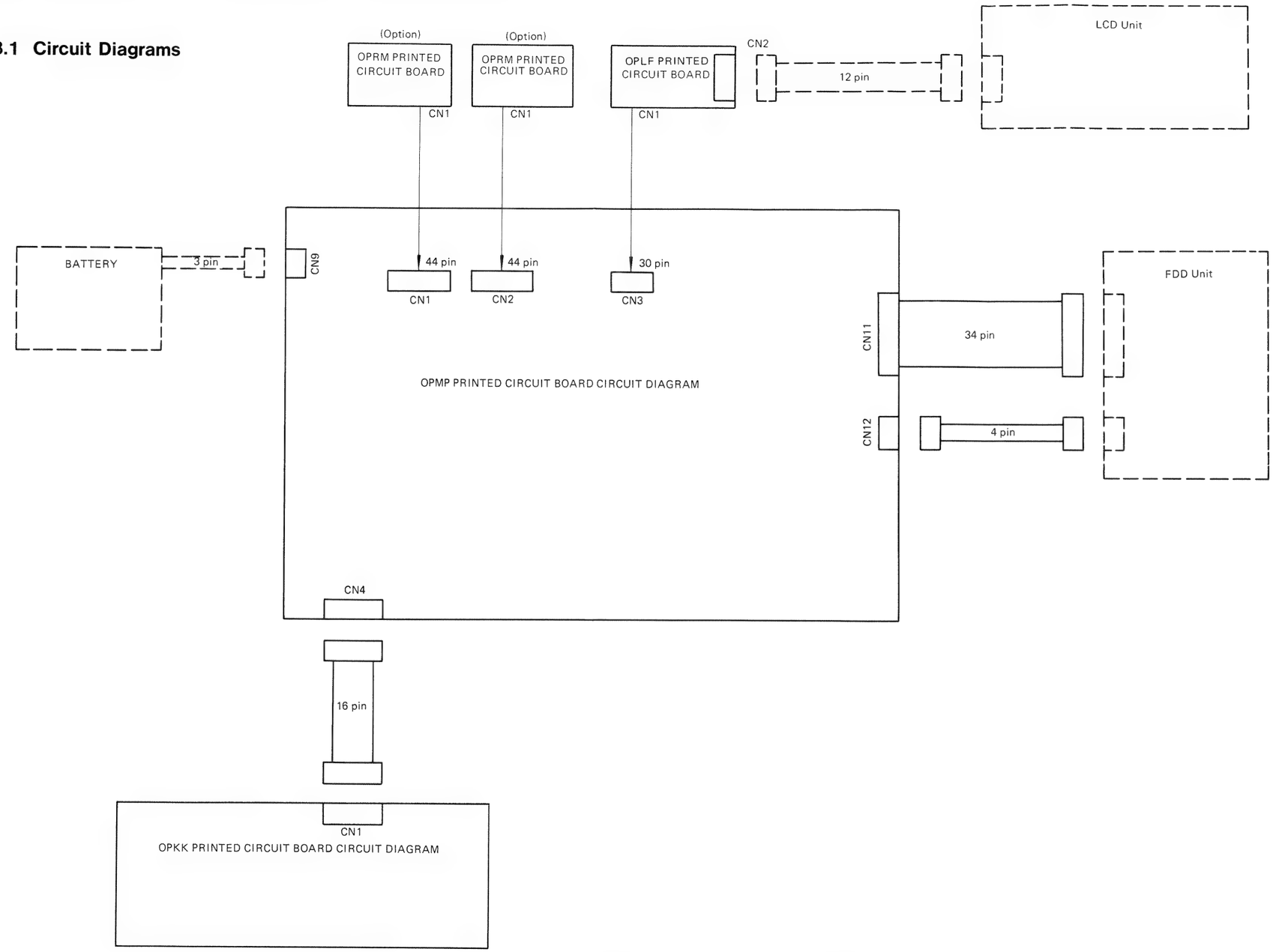
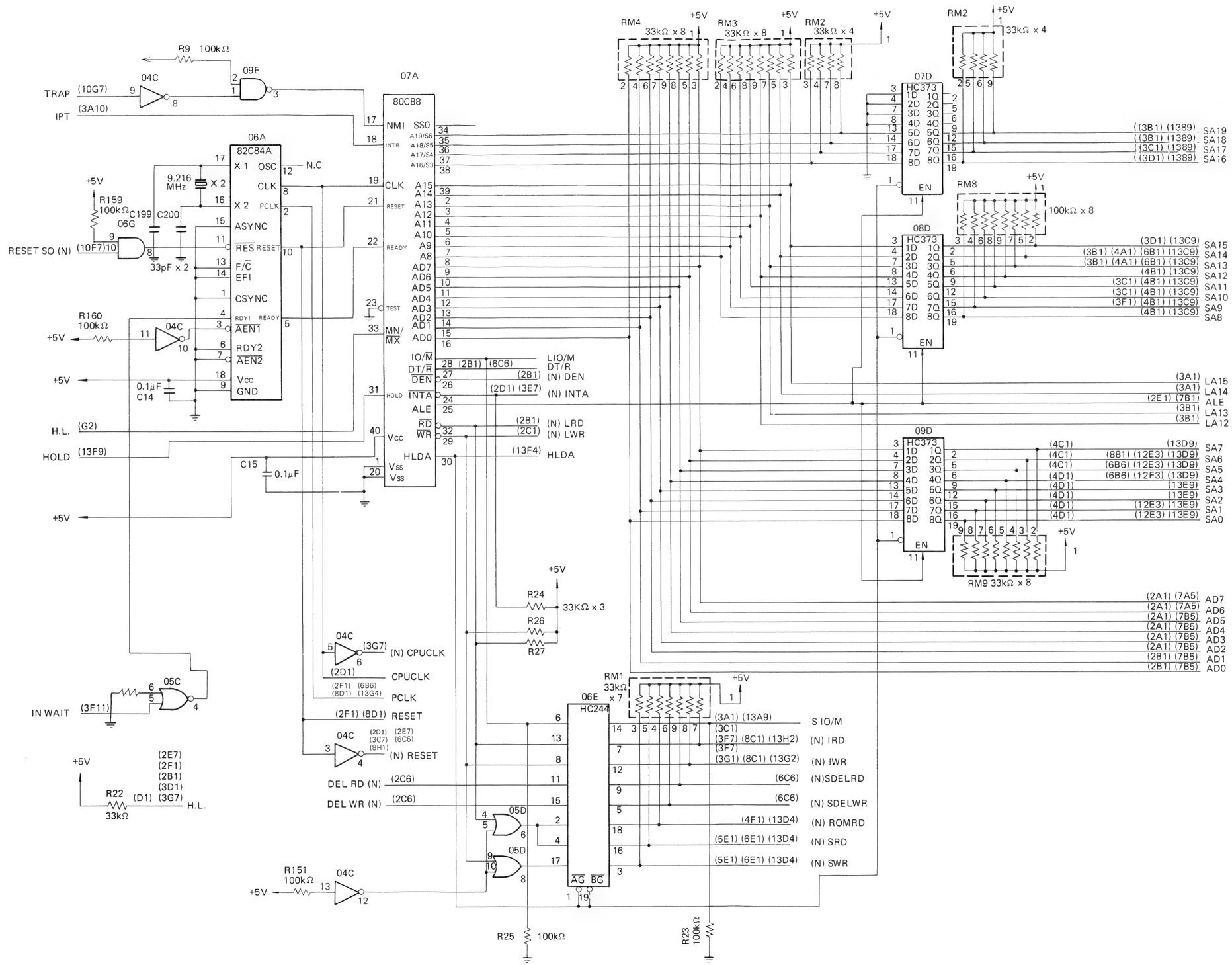
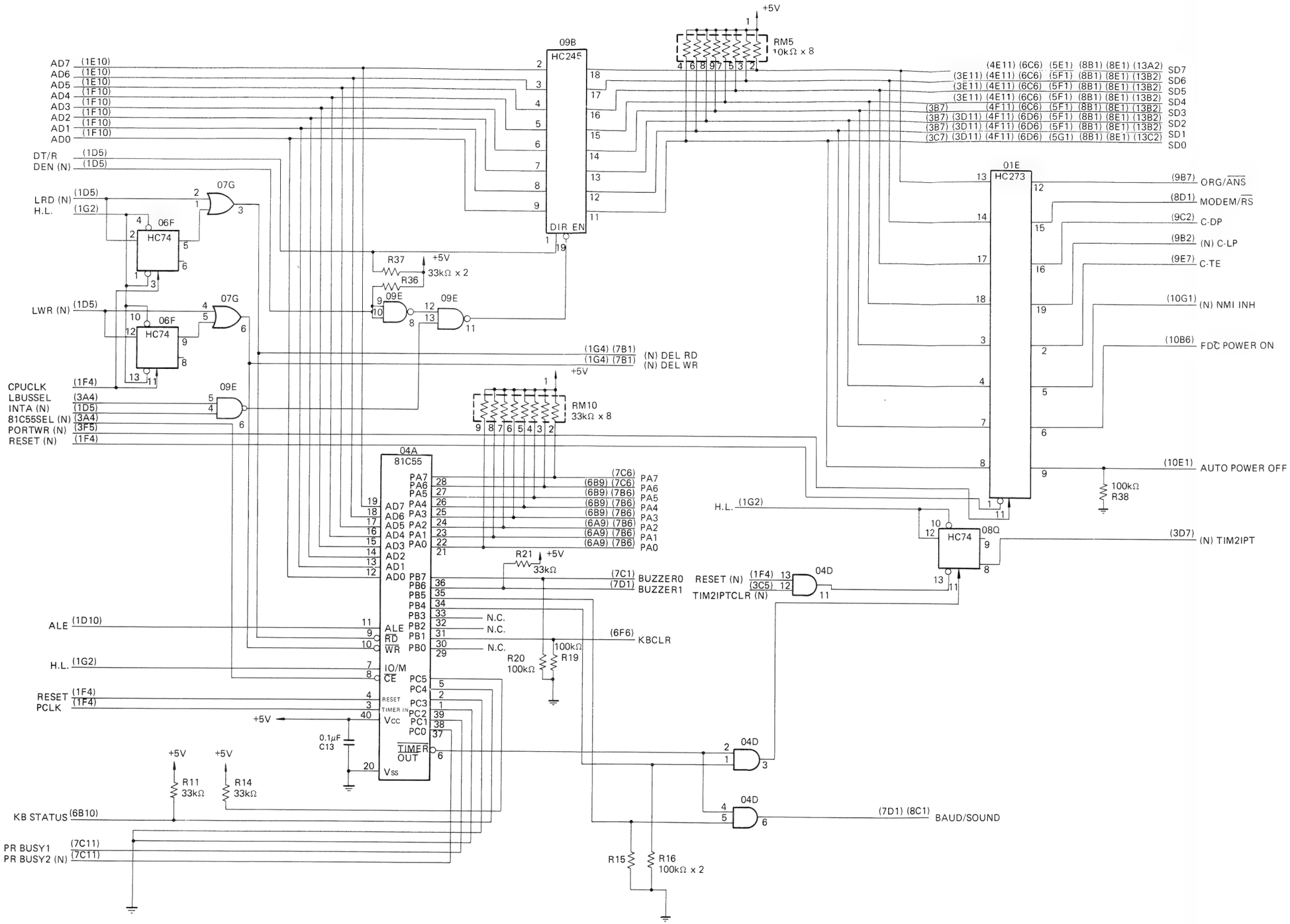


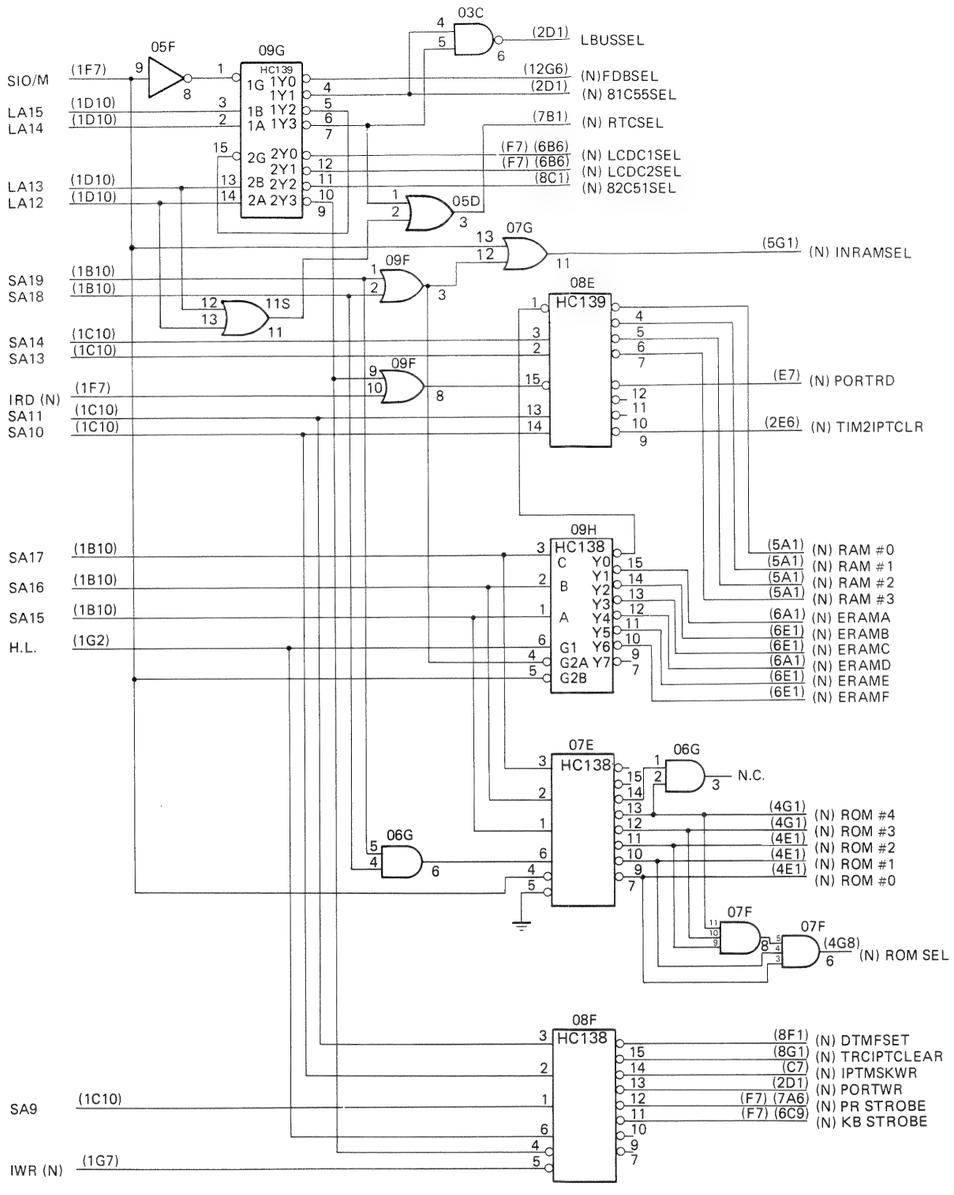
Figure 8-1 General Circuit Diagram

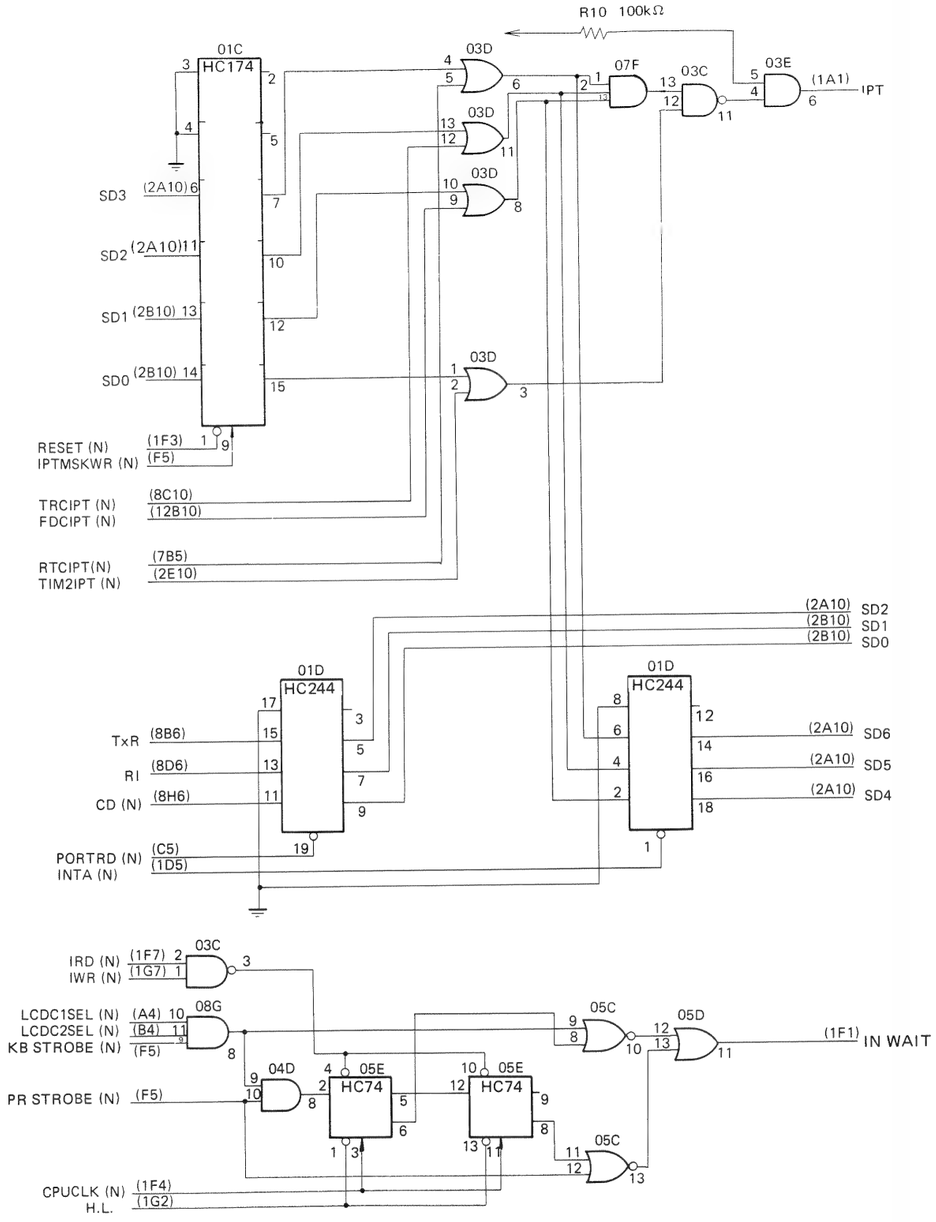


MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– CPU

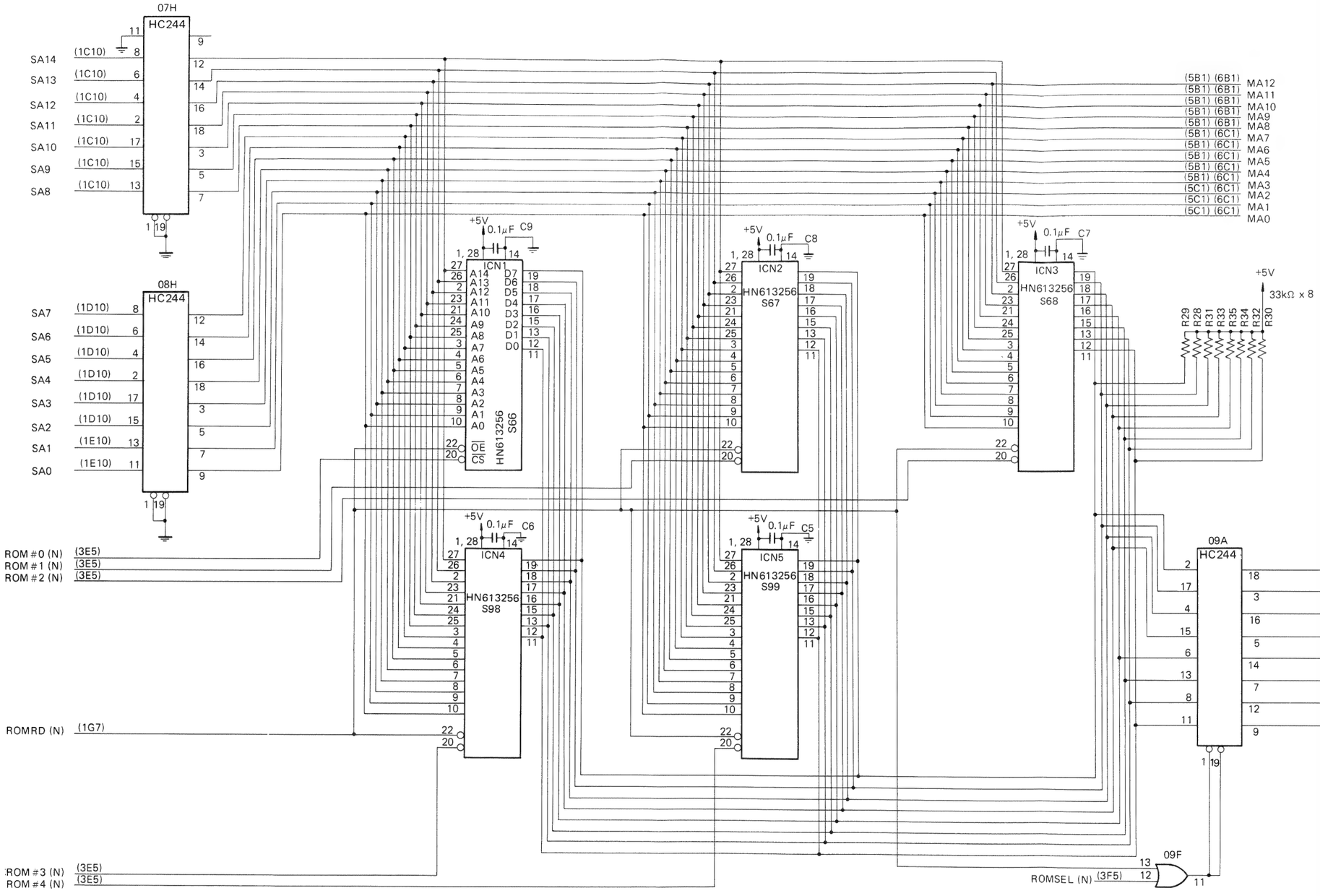


MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– PORT

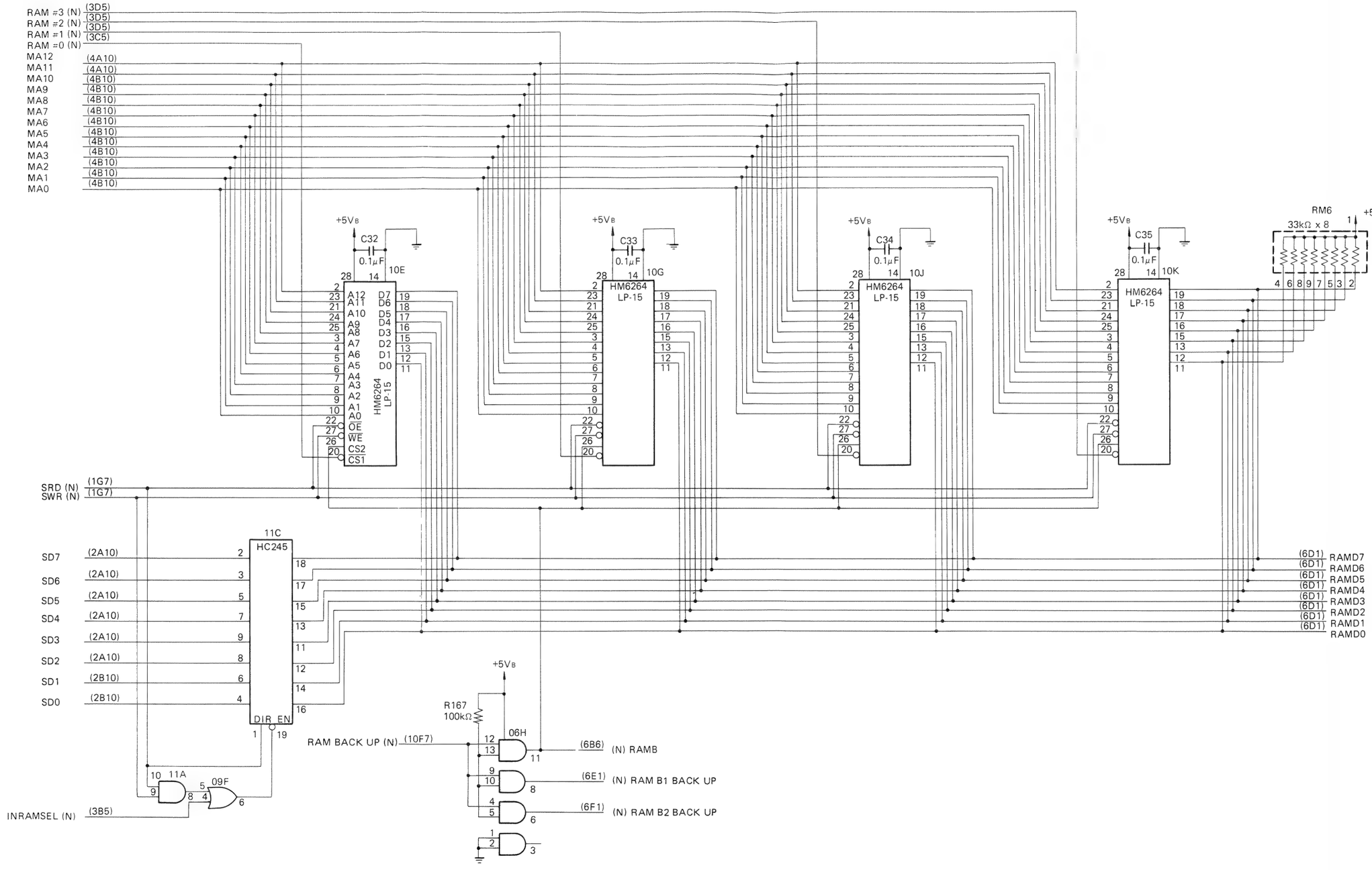




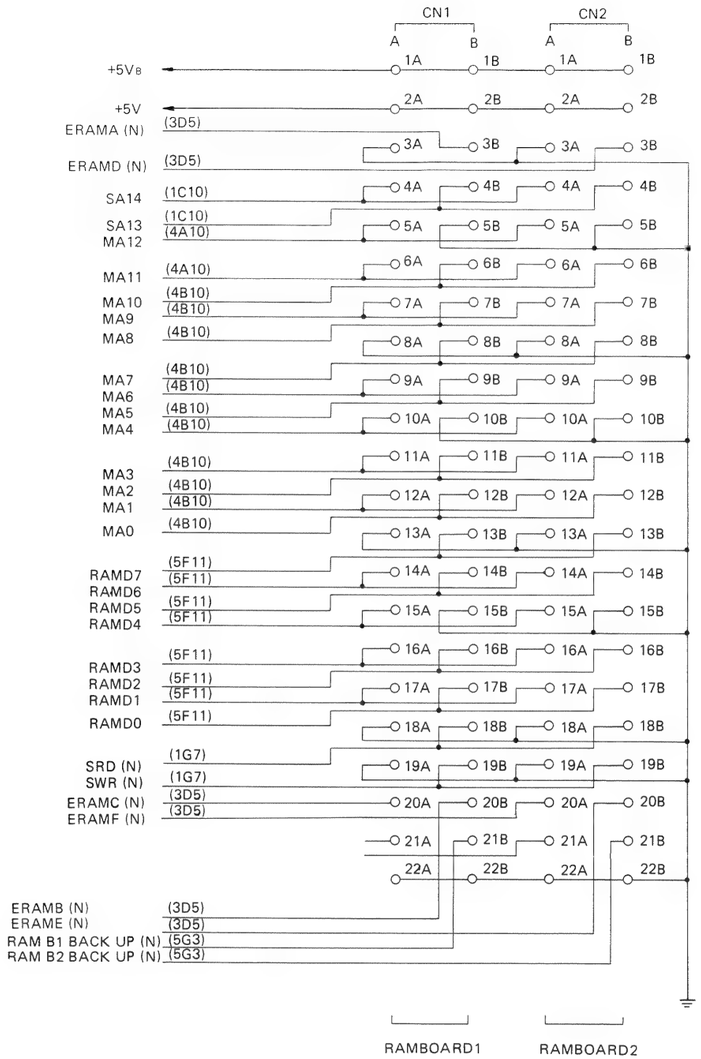
MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– CHIP SEL & IPT

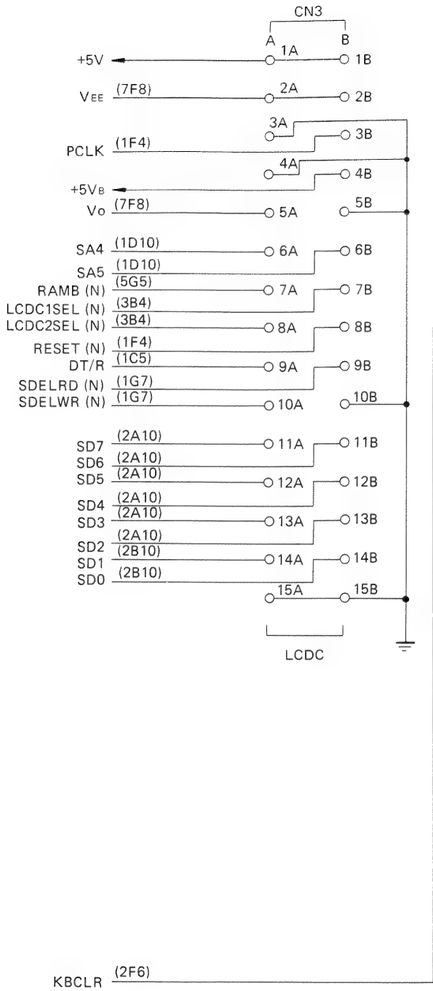


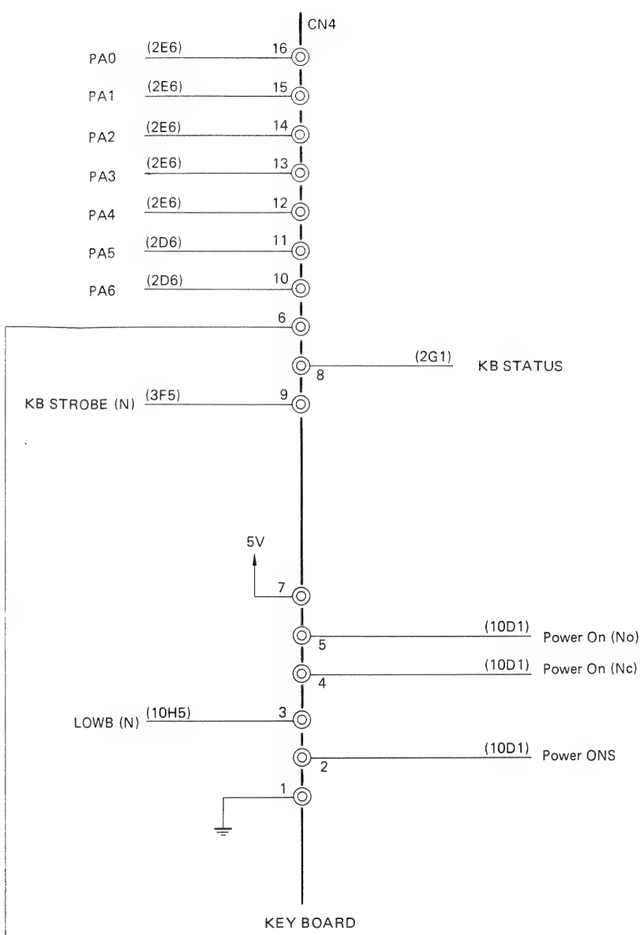
MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– ROM



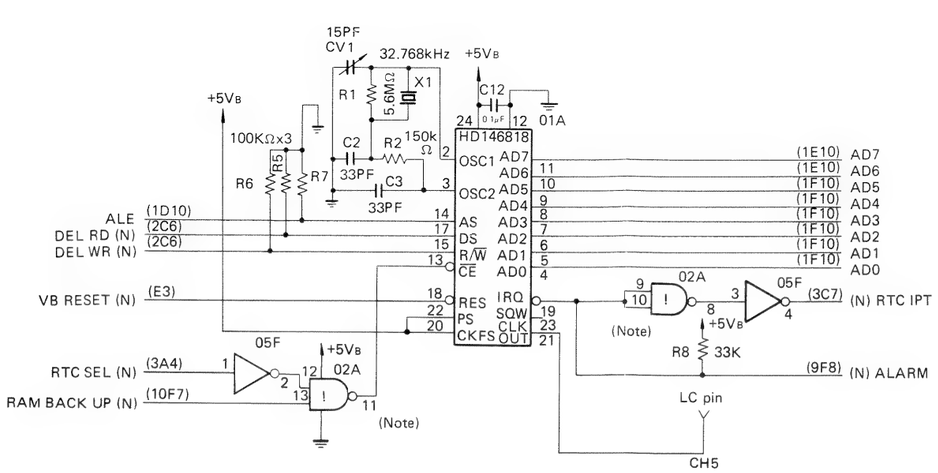
MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– RAM





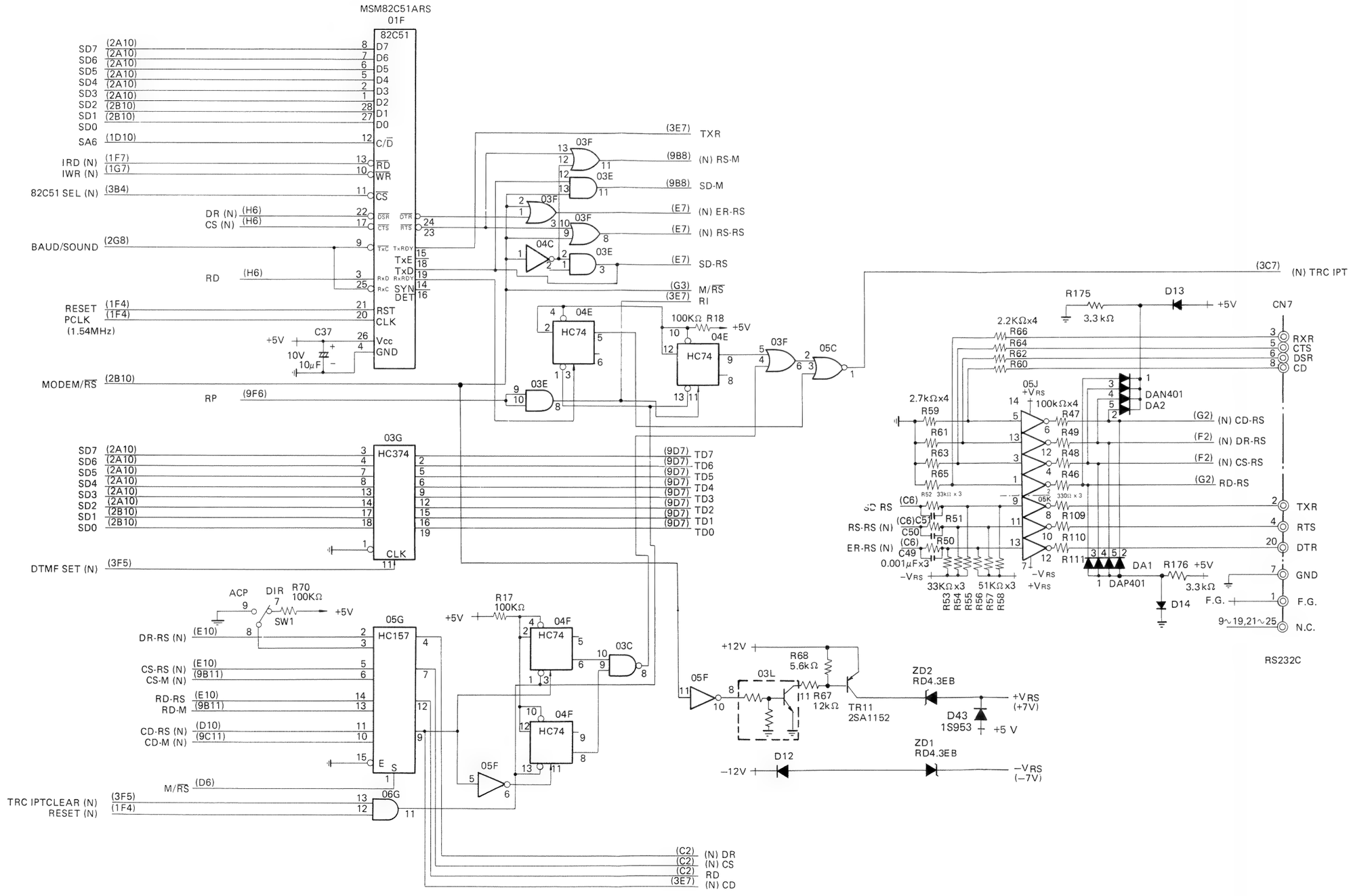


MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– CONNECT

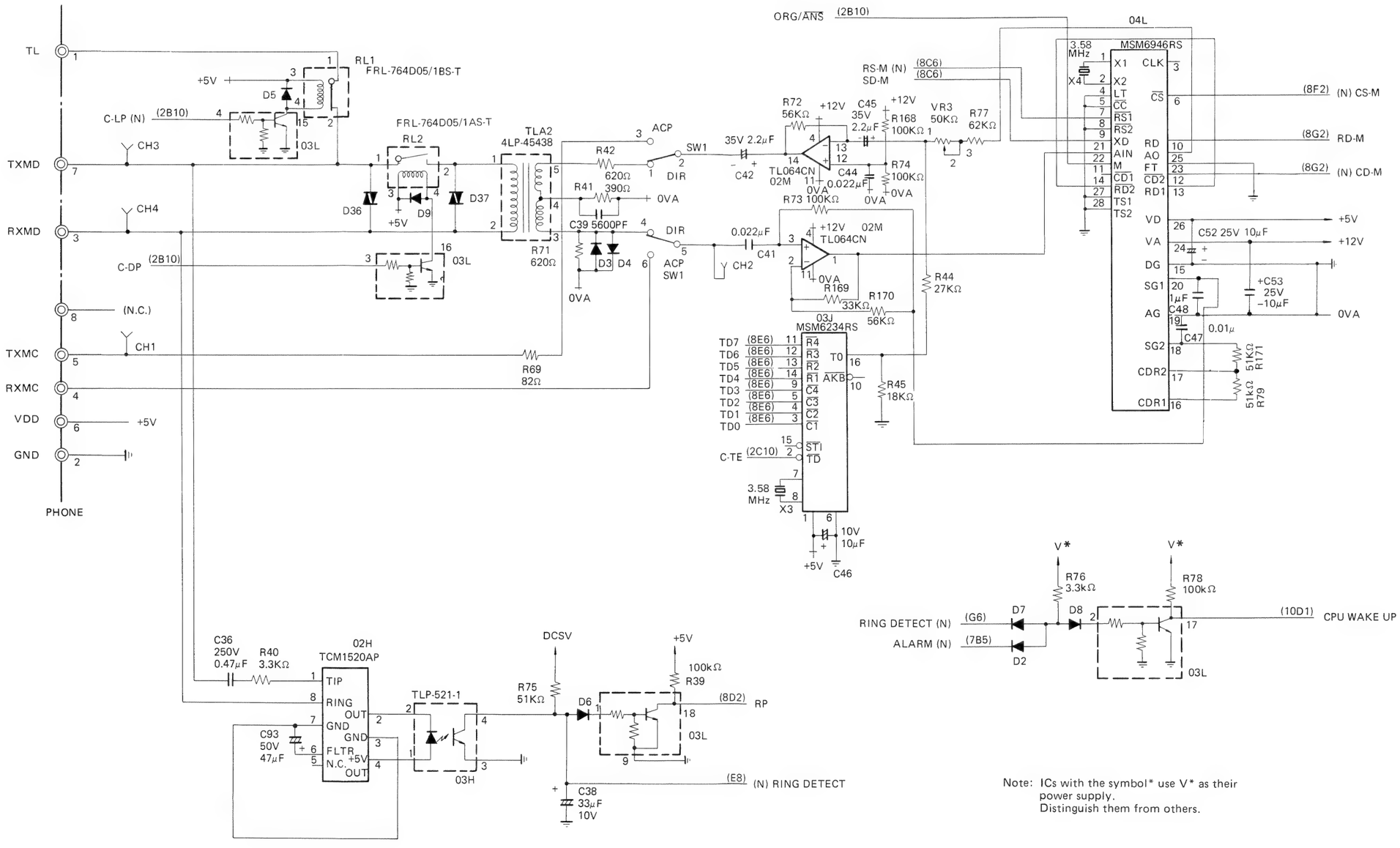


Note: In this IC (shown by "!"), connect +5V_B to pin 14 and the ground to pin 7.

MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– RTC, BUZZER, Pr, LCD

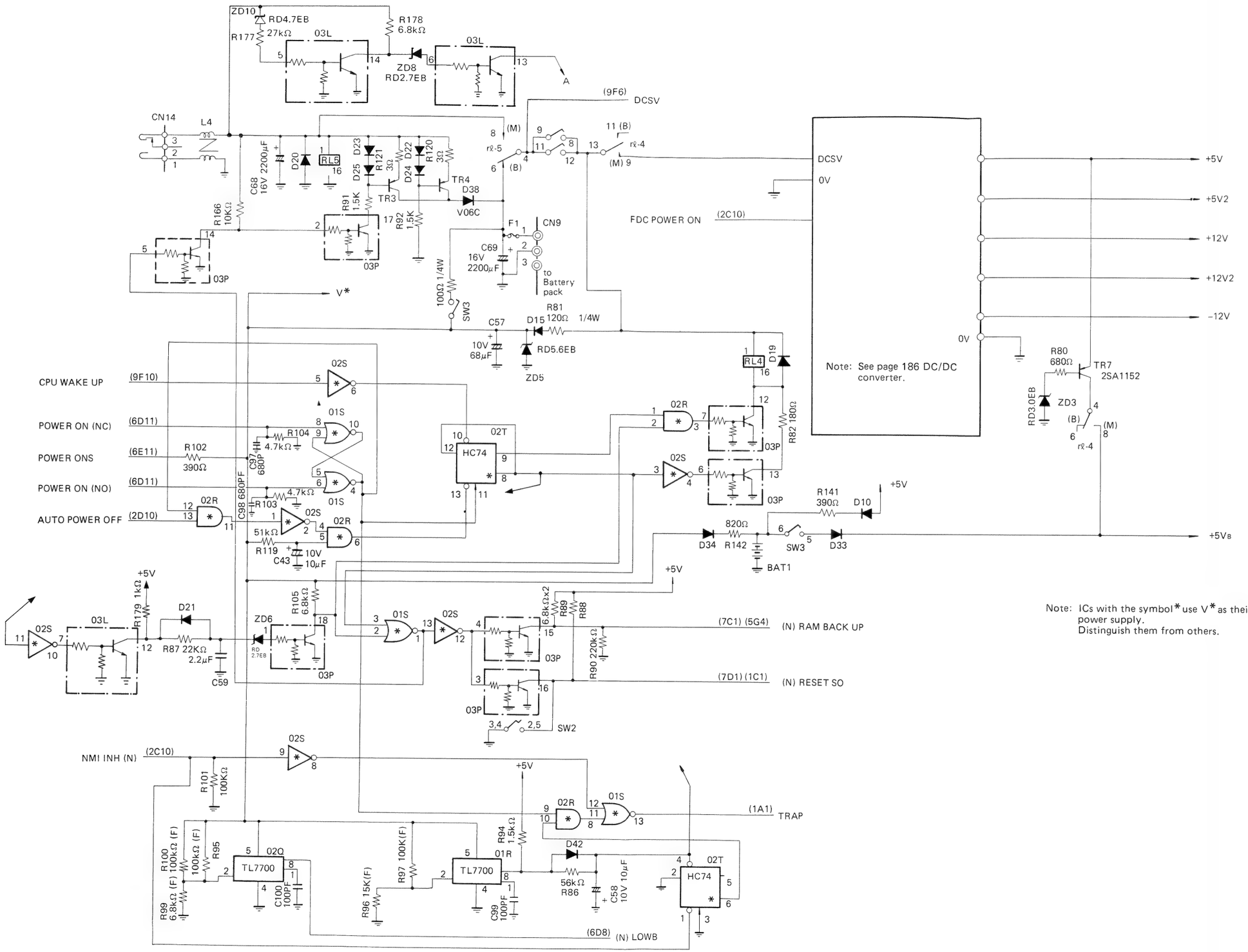


MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– NCU, RS232C



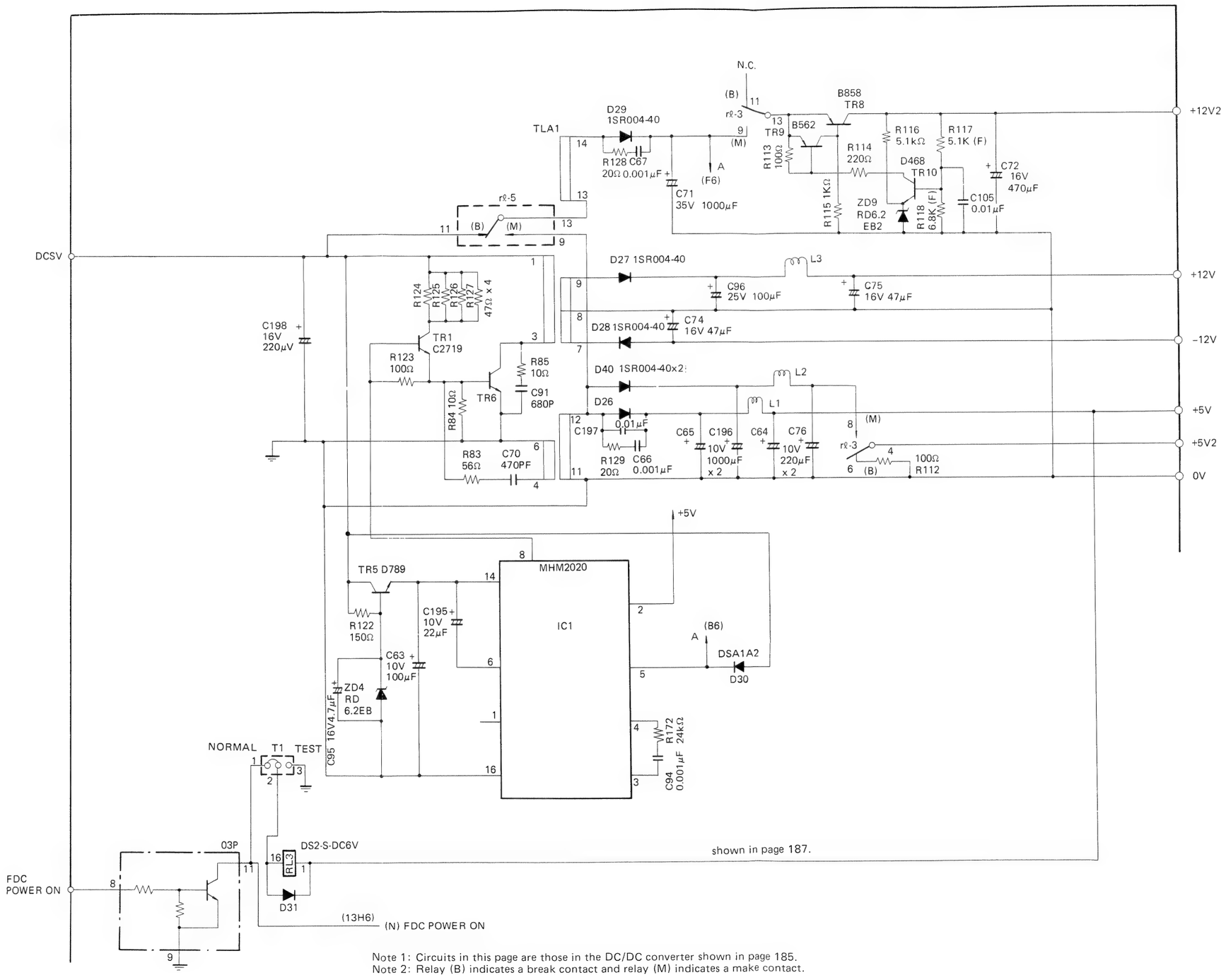
Note: ICs with the symbol* use V* as their power supply.
Distinguish them from others.

MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– TEL CONTROL, MODEM



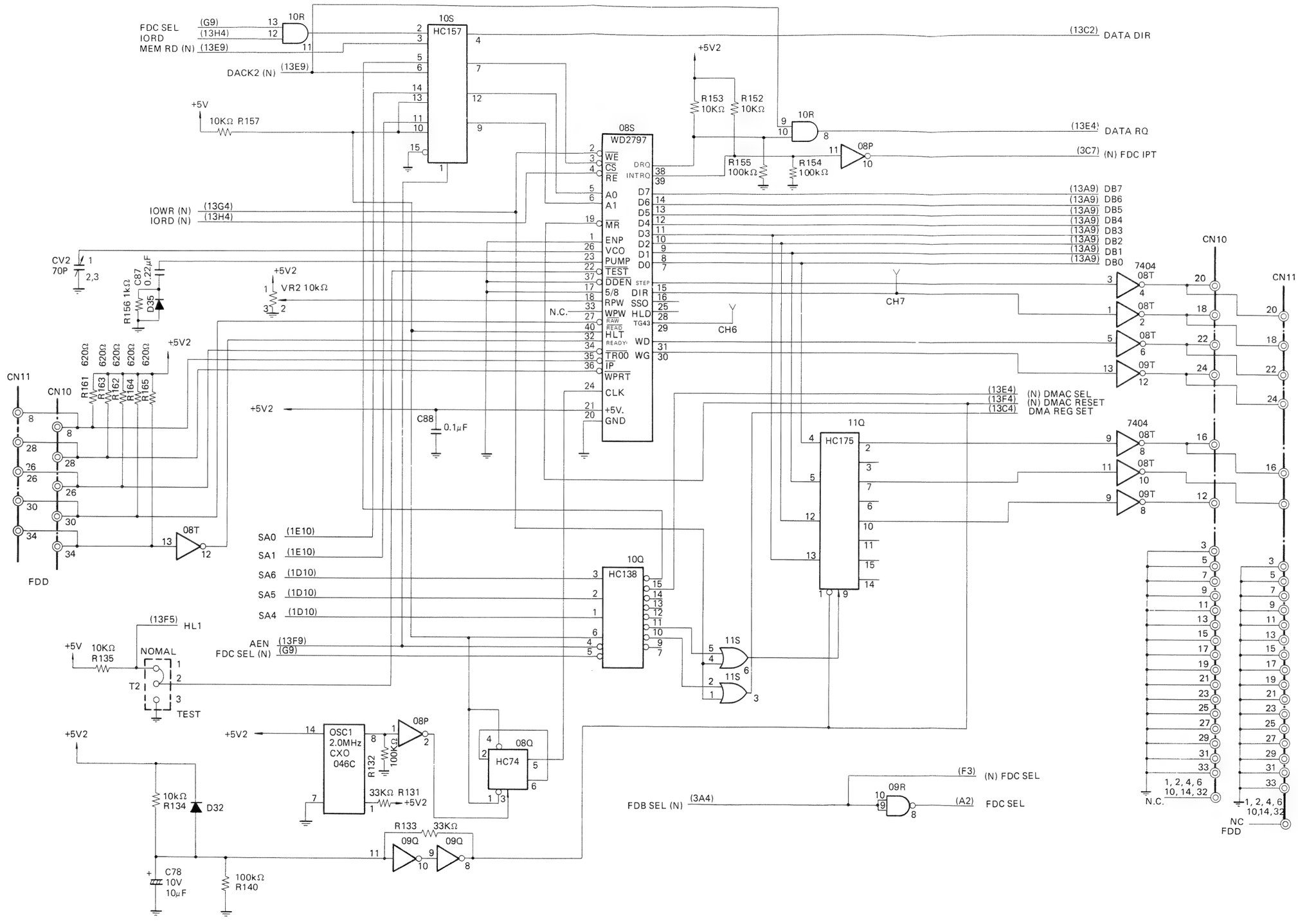
Note: ICs with the symbol * use V* as their power supply.
Distinguish them from others.

MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– POWER CONTROL

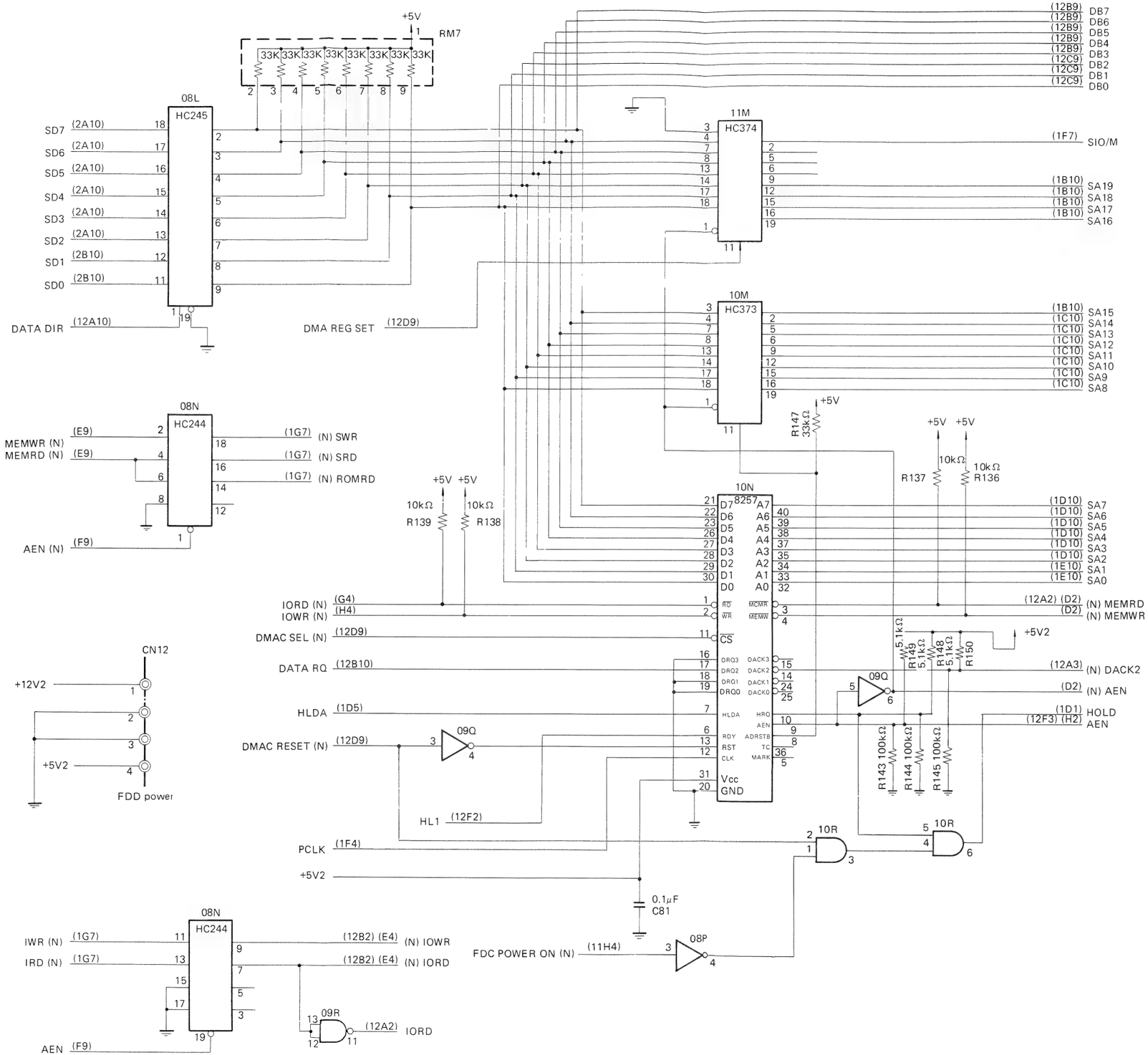


Note 1: Circuits in this page are those in the DC/DC converter shown in page 185.
Note 2: Relay (B) indicates a break contact and relay (M) indicates a make contact.

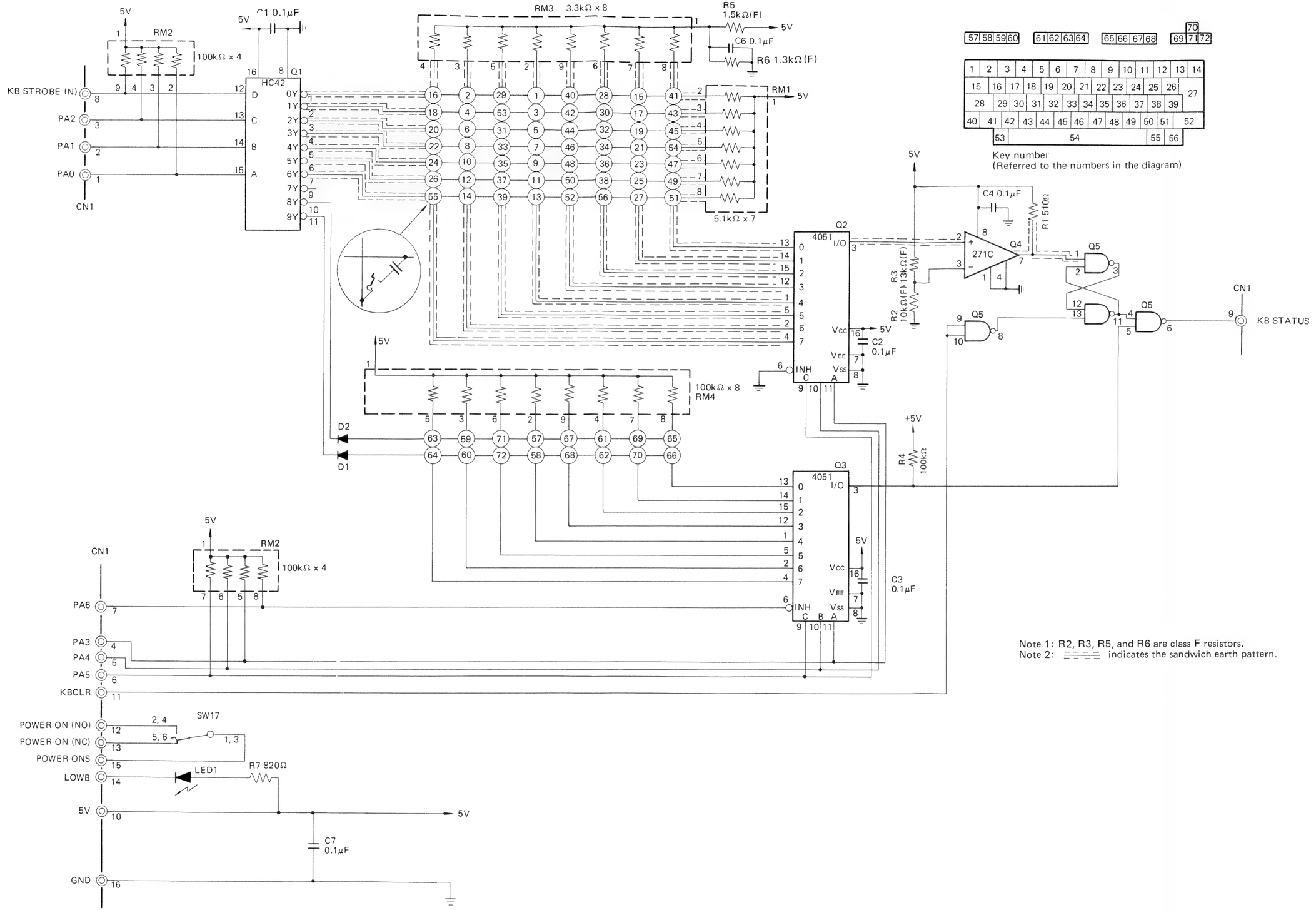
MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– DC/DC CONVERTER



MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– FDD CONTROL, etc.

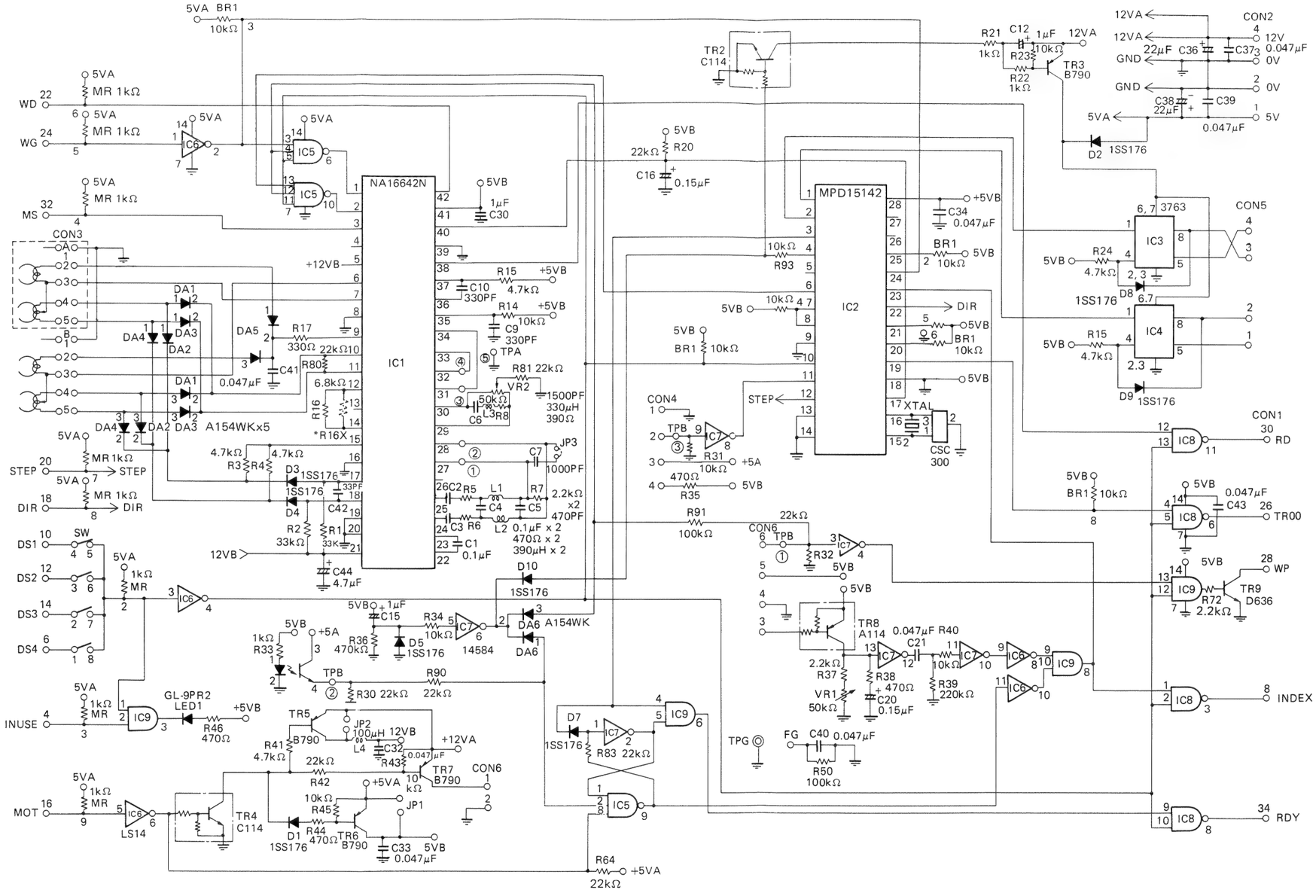


MAIN PCB (OPMP BOARD) CIRCUIT DIAGRAM –– DMA CONTROL, etc.

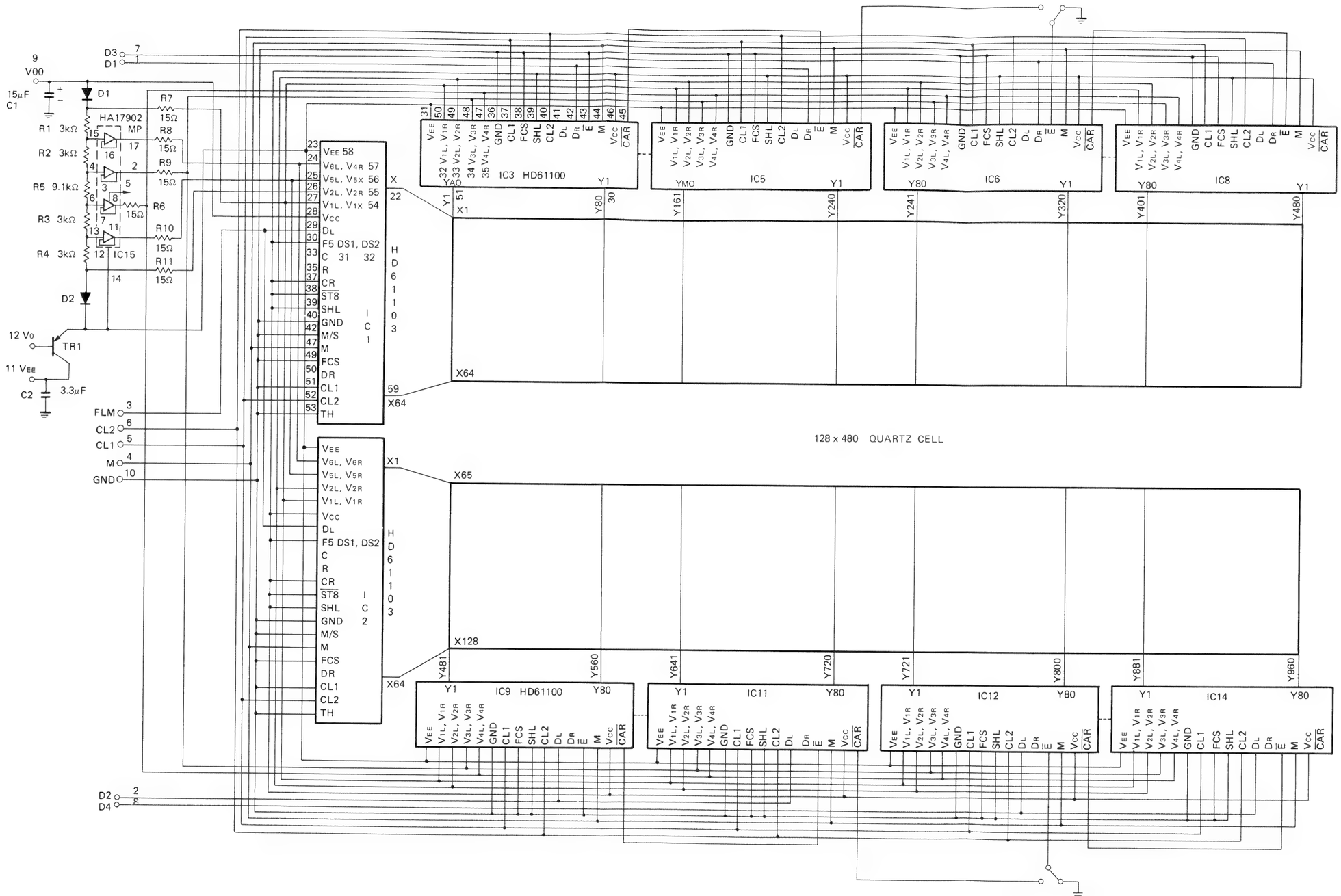


Note 1: R2, R3, R5, and R6 are class F resistors.
Note 2: ⩸ indicates the sandwich earth pattern.

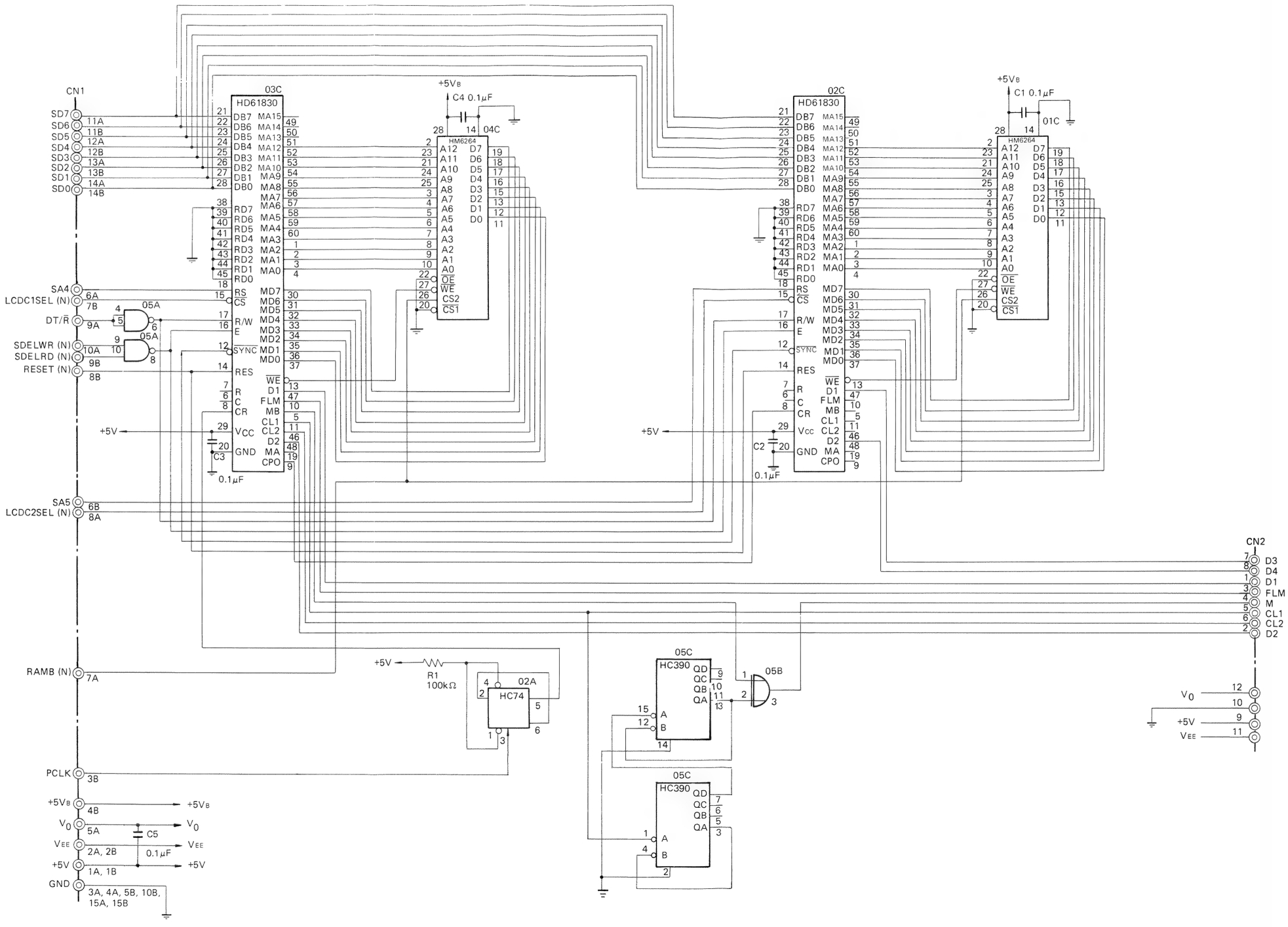
KEYBOARD PCB (OPKK BOARD) CIRCUIT DIAGRAM



FDD CIRCUIT DIAGRAM



LCD CIRCUIT DIAGRAM



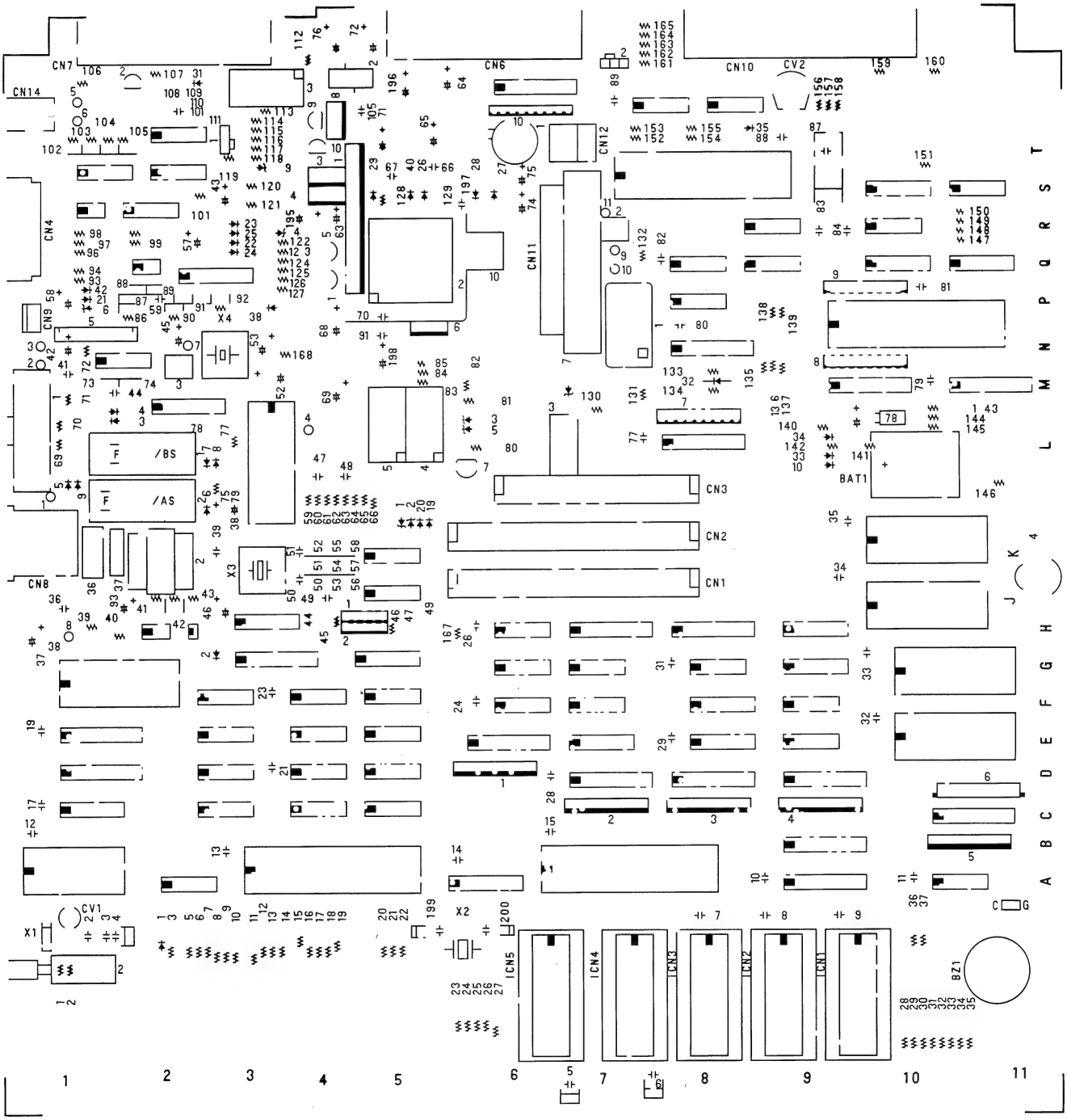
LCD CONTROLLER (OPLF BOARD) CIRCUIT DIAGRAM

Section 9
PCB VIEWS

SECTION 9 – PCB VIEWS

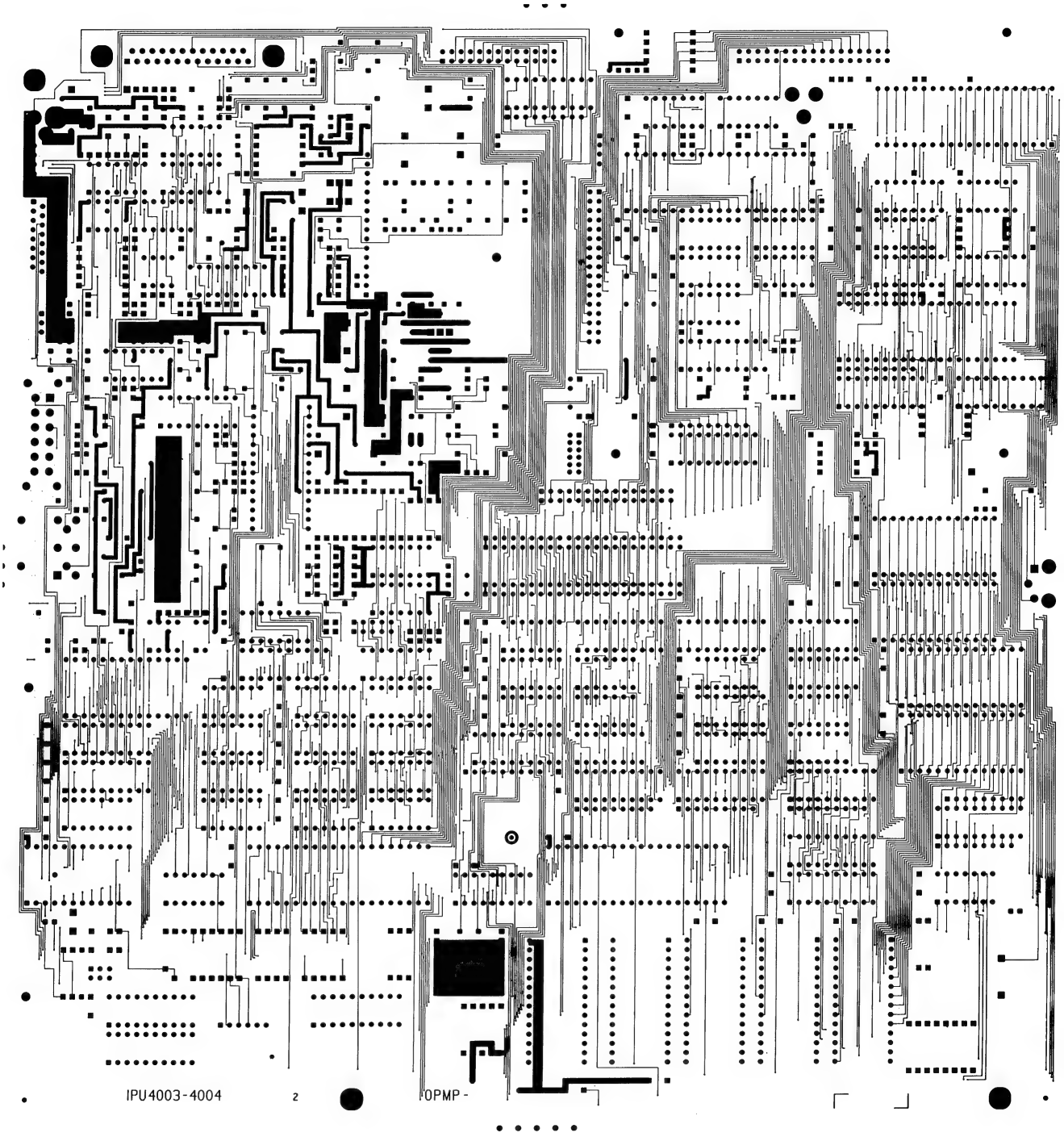
9.1 Main PCB Views

9.1.1 Silk Screen Print Side (Top view)

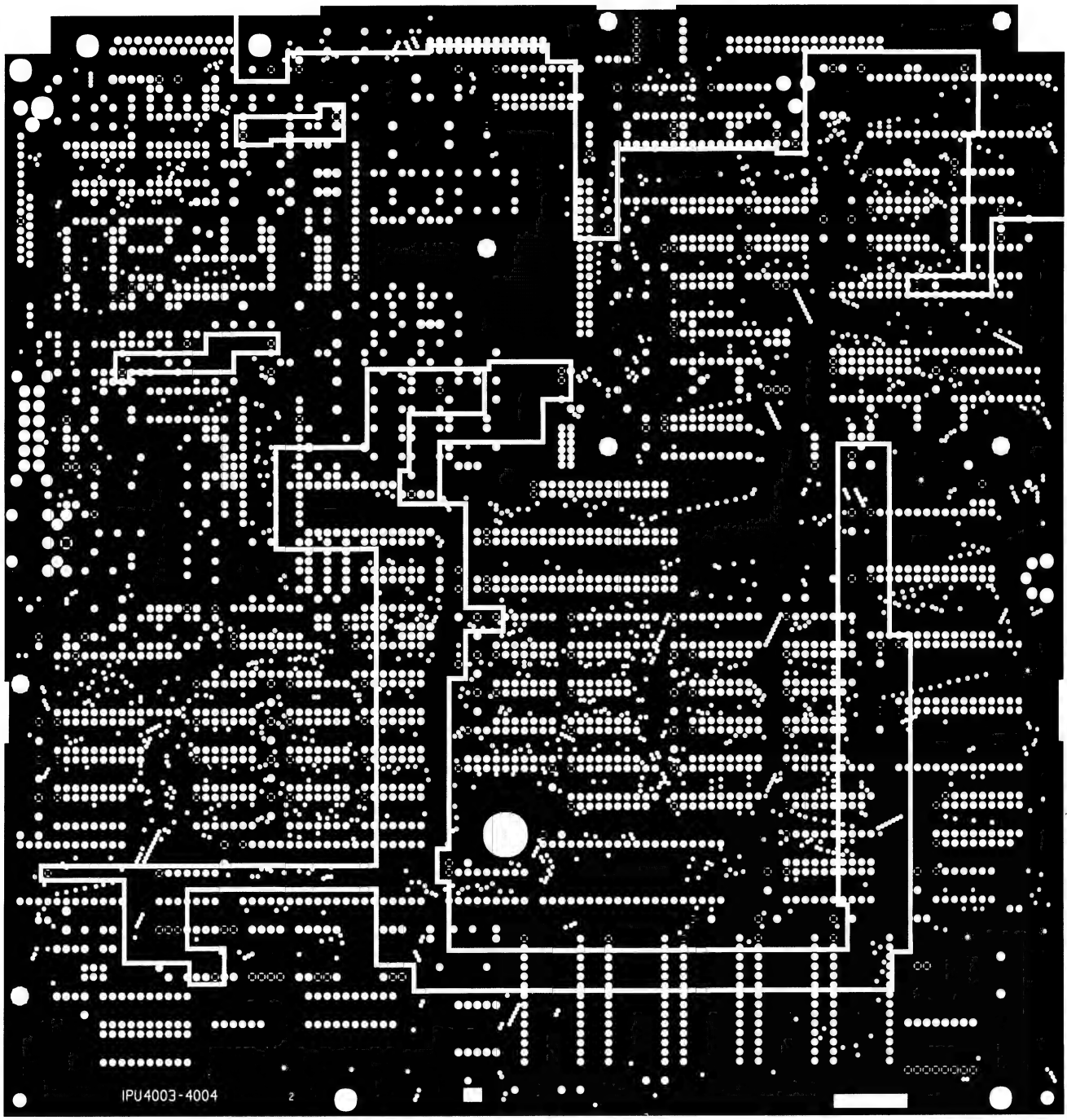


IPU4003-4004 S 59.9.12

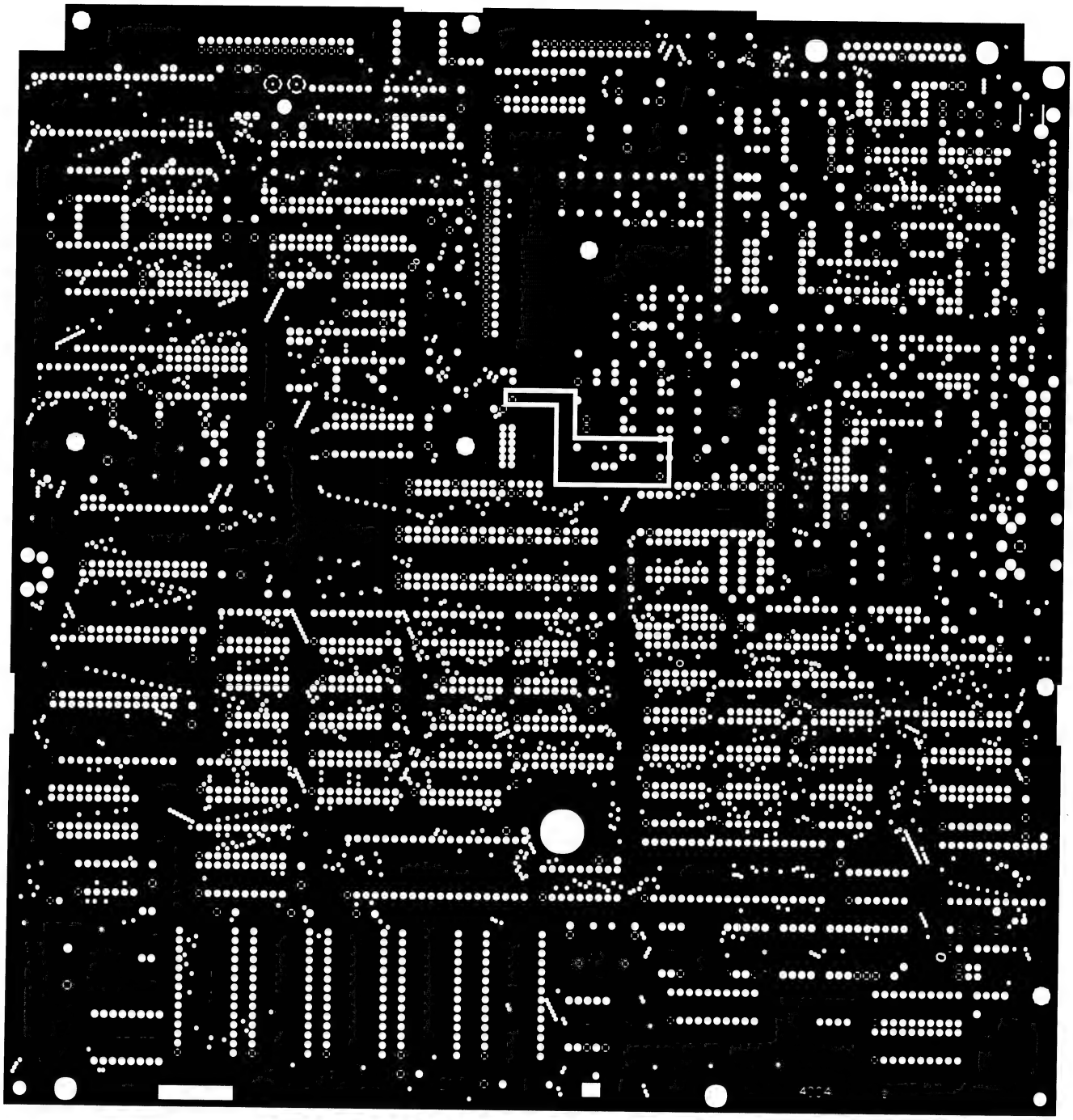
9.1.2 Component Side (Bottom view)



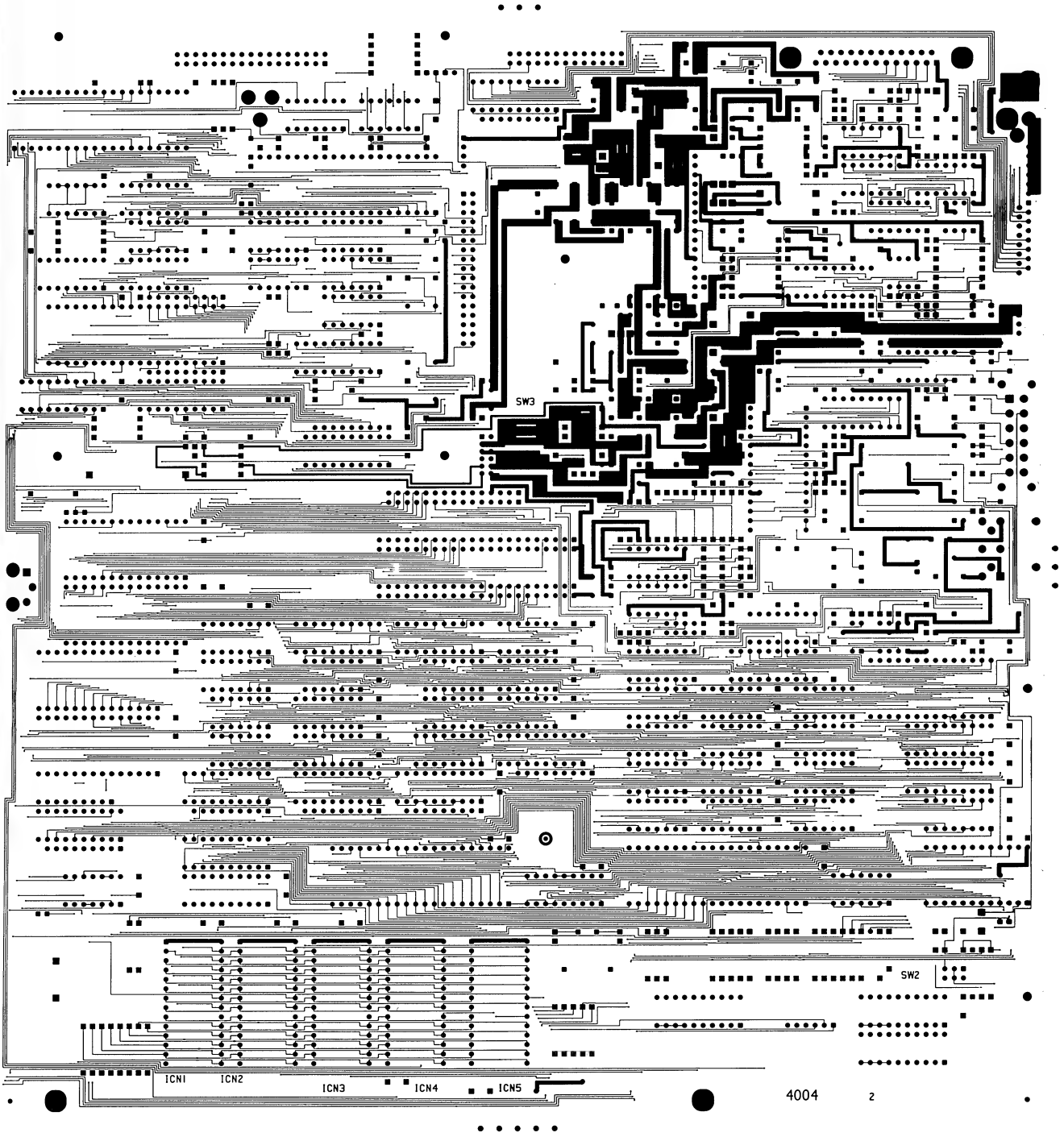
9.1.3 Intermediate Layers (1/2)



9.1.3 Intermediate Layers (2/2)

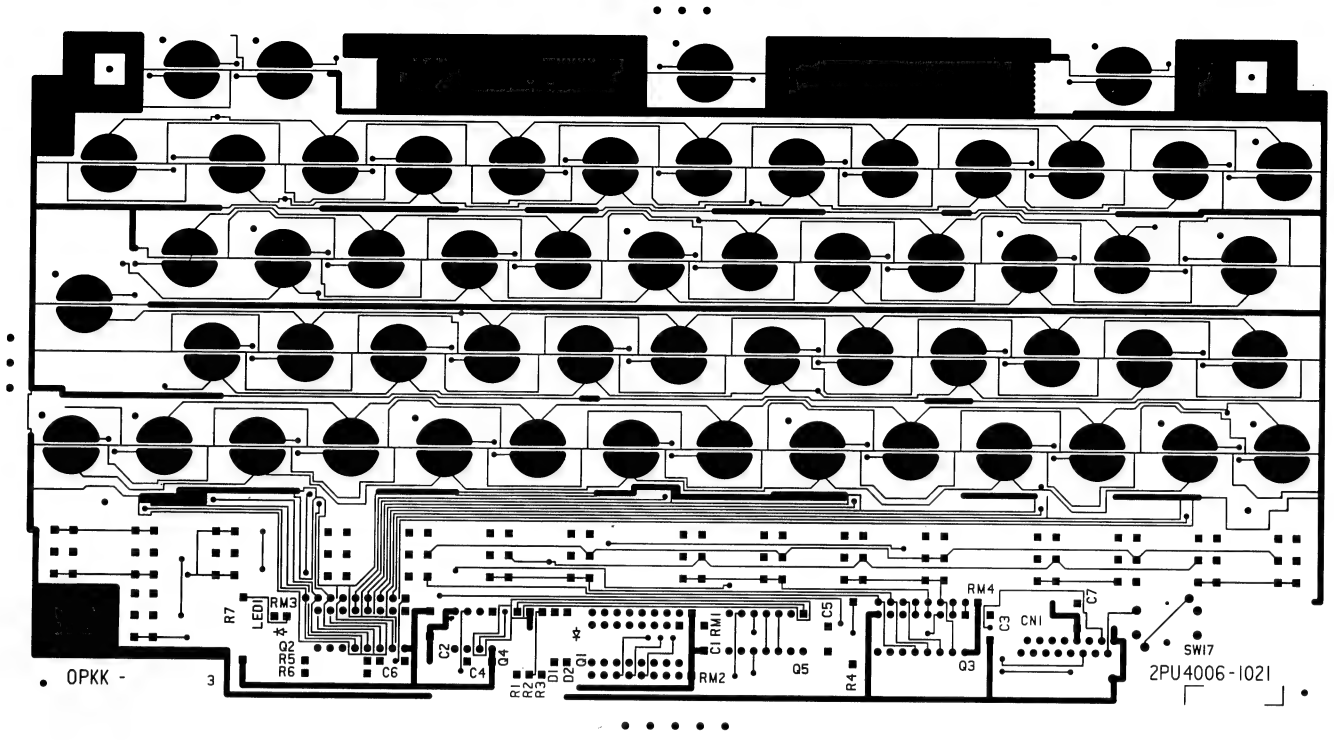


9.1.4 Circuit Side

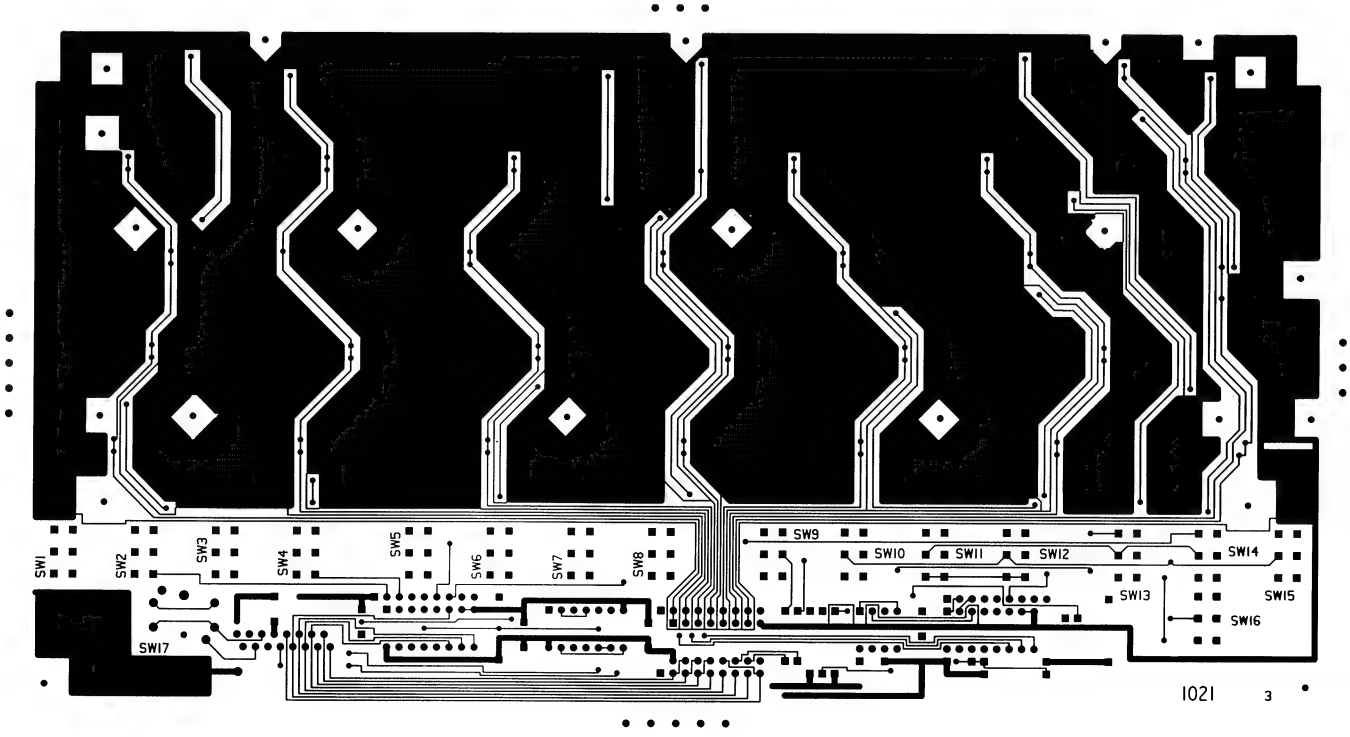


9.2 Keyboard PCB Views

9.2.1 Component Side (Top view)

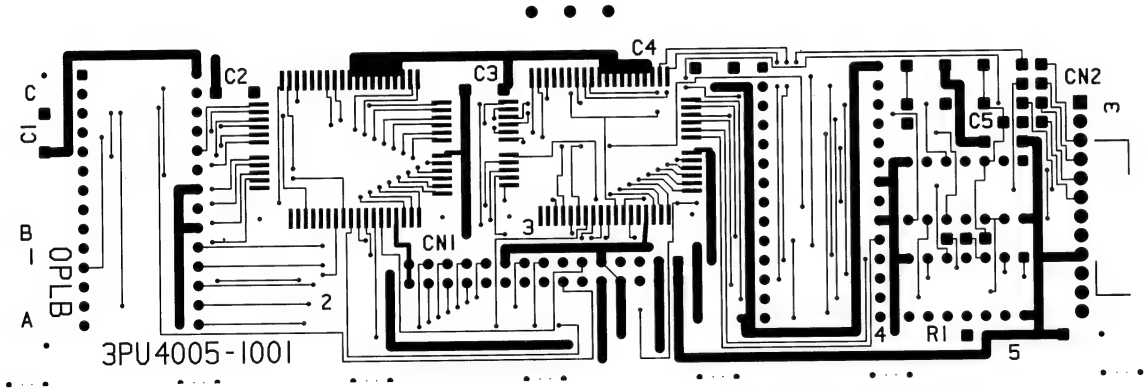


9.2.2 Circuit Side (Bottom view)

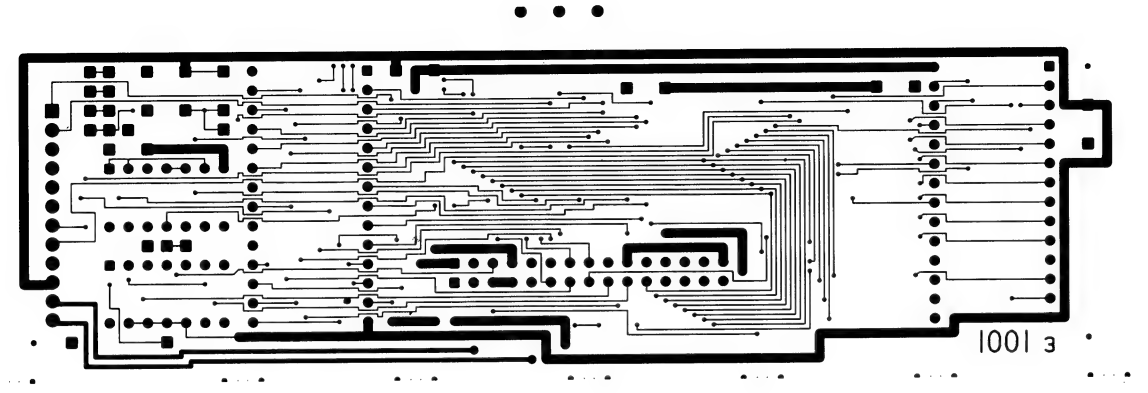


9.3 LCD Controller Board Views

9.3.1 Component Side (Top view)



9.3.2 Circuit Side (Bottom view)



APPENDICES

APPENDIX A

APPENDIX A – – DESCRIPTION OF I/O COMMANDS

(1) Instruction Format

There are two types of CPU I/O commands: IN (input) commands and OUT (output) commands. Data is passed between I/O devices in 8-bit length via the AL register. I/O devices are specified (DVA: device address) using the DX register.

(2) Device Address

Device addresses are expressed in 16 bits and are not fully decoded. The values shown in the table are only representative values. The "don't care" address bit (symbol "X" in the table) may be either a "0" or a "1."

(3) Device Address Map

Block	Representative DVA	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OUT	INP
	3000	0	0	X	X	X	X	0	0	0	X	X	0	0				FDC Command Reg. Set	FDC Status Reg. Read
	3001	0	0	X	X	X	X	0	0	0	X	X	0	1				FDC Track Reg. Set	FDC Track Reg. Read
	3002	0	0	X	X	X	X	0	0	0	X	X	1	0				FDC Sector Reg. Set	FDC Sector Reg. Read
	3003	0	0	X	X	X	X	0	0	0	X	X	1	1				FDC Data Reg. Set	FDC Data Reg. Read
	3014	0	0	X	X	X	X	0	0	1	0	1	0	0				DMAC Address Set	
	3015	0	0	X	X	X	X	0	0	1	0	1	0	1				DMAC TC Set	
	3018	0	0	X	X	X	X	0	0	1	1	0	0	0				DMAC Mode Set	DMAC Status Reg. Read
	3050	0	0	X	X	X	X	1	0	1	X	X	X	X				EXT FF Set	
	3060	0	0	X	X	X	X	1	1	0	X	X	X	X				DMA Transfer Reg. Set	
	4000	0	1	X	X	X	X	X	X	X	X	0	0	0				Port 1 Command Set	Port 1 Status Read
	4001	0	1	X	X	X	X	X	X	X	X	0	0	1				Out Port A Data Set	Out Port A Data Read
	4002	0	1	X	X	X	X	X	X	X	X	0	1	0				Out Port B Data Set	Out Port B Data Read
	4003	0	1	X	X	X	X	X	X	X	X	0	1	1					In Port C Data Read
	4004	0	1	X	X	X	X	X	X	X	X	1	0	0				Timer Count Low Set	Timer Count Low Read
	4005	0	1	X	X	X	X	X	X	X	X	1	0	1				Timer Count High Set	Timer Count High Read
	8000	1	0	0	0	X	X	X	X	0	X							LCDC1 Data Set	LCDC1 Data Read
	8010	1	0	0	0	X	X	X	X	1	X							LCDC1 Instruction Set	
	9000	1	0	0	1	X	X	X	0	X	X							LCDC2 Data Set	LCDC2 Data Read
	9020	1	0	0	1	X	X	X	1	X	X							LCDC2 Instruction Set	

Block	Representative DVA	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OUT	INP
82C51	A000	1	0	1	0	X				X	0	X	0	X				USART Data set	USART Data Read
	A040	1	0	1	0	X				X	1	X	0	X				USART Command SET	USART Status Read
I/O	B000	1	0	1	1	0	0	X	X	X				X					In Port E Data Read
	B000	1	0	1	1	0	0	0	X	X				X				DTMF Set	
	B200	1	0	1	1	0	0	1	X	X				X				TRC IPT Clear	
	B400	1	0	1	1	0	1	0	X	X				X				IPT Mask Set	
	B600	1	0	1	1	0	1	1	X	X				X				Out Port D Data Set	
	B800	1	0	1	1	1	0	0	X	X				X				Printer Strobe	
	BA00	1	0	1	1	1	0	1	X	X				X				KB Strobe	
	BC00	1	0	1	1	1	1	X	X	X				X					81C55 Timer IPT Clear
HD146818	C000	1	1	X	X	X				0	0	0	0	0	0	0	0	Seconds Set/Read	
	C001	1	1	X	X	X				0	0	0	0	0	0	0	1	Seconds Alarm Set/Read	
	C002	1	1	X	X	X				0	0	0	0	0	0	1	0	Minutes Set/Read	
	C003	1	1	X	X	X				0	0	0	0	0	0	1	1	Minutes Alarm Set/Read	
	C004	1	1	X	X	X				0	0	0	0	0	1	0	0	Hours Set/Read	
	C005	1	1	X	X	X				0	0	0	0	0	1	0	1	Hours Alarm Set/Read	
	C006	1	1	X	X	X				0	0	0	0	0	1	1	0	Day of the Week Set/Read	
	C007	1	1	X	X	X				0	0	0	0	0	1	1	1	Date of the Month Set/Read	
	C008	1	1	X	X	X				0	0	0	0	1	0	0	0	Month Set/Read	
	C009	1	1	X	X	X				0	0	0	0	1	0	0	1	Year Set/Read	
	C00A	1	1	X	X	X				0	0	0	0	1	0	1	0	Control Register A	
	C00B	1	1	X	X	X				0	0	0	0	1	0	1	1	Control Register B	
	C00C	1	1	X	X	X				0	0	0	0	1	1	0	0	Control Register C	
	C00D	1	1	X	X	X				0	0	0	0	1	1	0	1	Control Register D	
	C00E ∫ C03F	1	1	X	X	X				0E ~ 3F								User RAM	

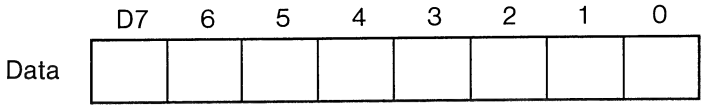
Status Register bit	TYPE I	TYPE II		TYPE III			TYPE IV		Master Reset
	All Commands	Read Data	Write Data	Read Address	Read Track	Write Track	Other Command Being Executed	No Command Being Executed	
STR 7	Not Ready	←	←	←	←	←	←	←	In accordance with TYPE I
STR 6	Write Protect	0	Write Protect	0	0	Write Protect	Same status bit as that of the command being executed until now	Write Protect	
STR 5	Head Engaged	Record Type	Write Fault	0	0	Write Fault		Head Engaged	
STR 4	Seek Error	Record Not Found	←	←	0	0		0	
STR 3	CRC Error	←	←	←	0	0		0	
STR 2	Track "00"	Lost Data	←	←	←	←		Track "00"	
STR 1	Index	DRQ	←	←	←	←		Index	
STR 0	Busy	←	←	←	←	←	0	0	

Table A-1. Contents of WD2797 Status Register

Status Bit Meanings

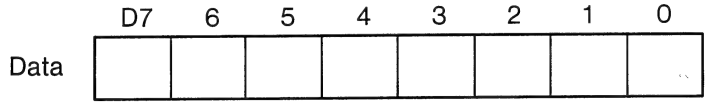
Status bit	Meaning
Not Ready	NOT READY = "1" indicates that the FDD is not operational.
Write Protect	WRITE PROTECT = "1" indicates that the FDD is write disabled.
Seek Error	SEEK ERROR = "1" indicates that a seek error has occurred.
CRC Error	CRC ERROR = "1" indicates that a CRC error has occurred in the ID field or the DATA field.
Busy	BUSY = "1" indicates that the FDC is currently executing a command.
Write Fault	WRITE FAULT = "1" indicates that the WRITE FAULT FOCUS signal was received from the FDD while writing onto the disk.
Record Not Found	Indicates that the track and sector specified by RECORD NOT FOUND = "1" could not be found.
Lost Data	LOST DATA = "1" means that read or write (1 byte) could not be performed.

Command	FDC Command Reg. Set		
Address	3000H	I/O	OUT



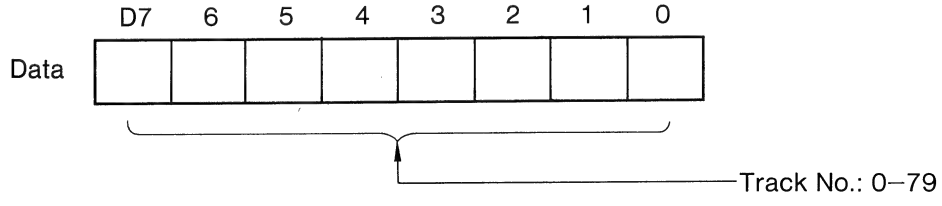
This command is used to set the WD2797 command register. There are four types of command, types I-IV.

Command	FDC Status Reg. Read		
Address	3000H	I/O	INP



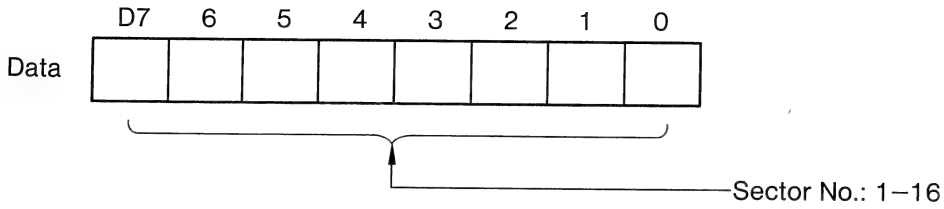
This command is used to read the status register for WD2797.
The contents of the status register are shown in Table A-1.

Command	FDC Track Reg. Set/FDC Track Reg. Read		
Address	3001H	I/O	OUT/INP



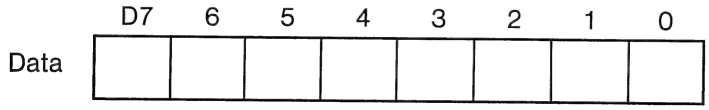
This command is used to read from or write into the track register for WD2797.

Command	FDC Sector Reg. Set/FDC Sector Reg. Read		
Address	3002H	**I/O**	OUT/INP



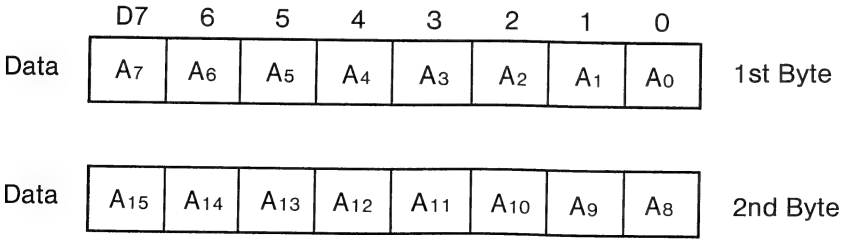
This command is used to read from or write into the sector register for WD2797.

Command	FDC Data Reg. Set/FDC Data Reg. Read		
Address	3003H	**I/O**	OUT/INP



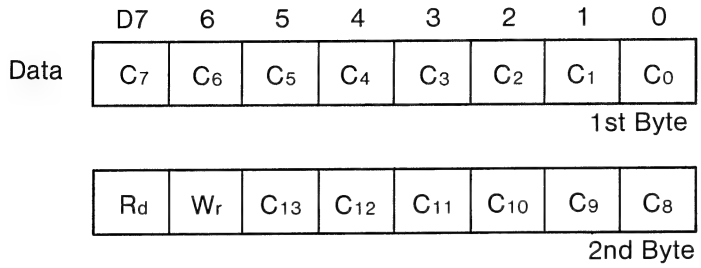
This command is used to read from or write into the data register for WD2797. The FDD read/write data is stored in this register.

Command	DMAC Address Set		
Address	3014H	**I/O**	OUT



This command is used to set the memory address (16-bit) for DMA transfer on DMAC (μPD8257C). DMA channel 2 is used for the transfer.

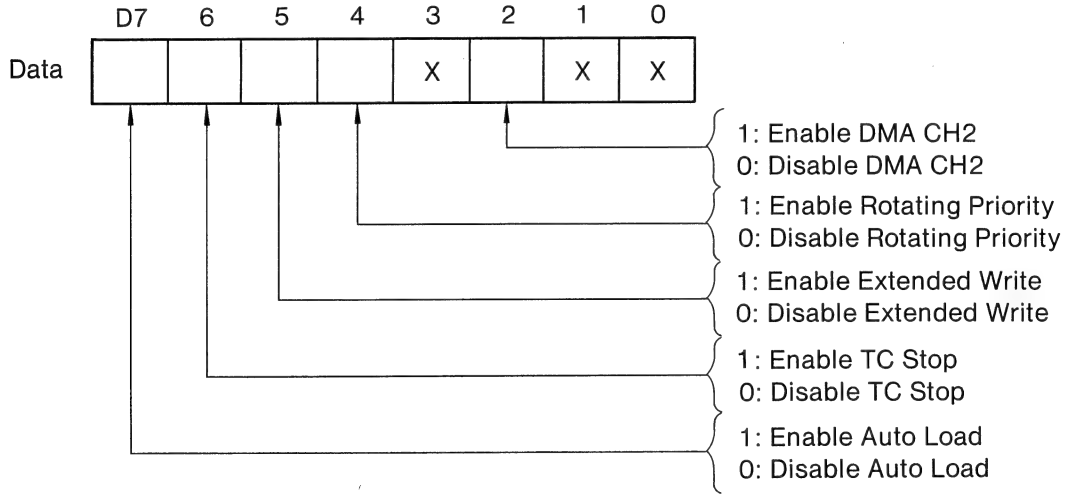
Command	DMAC TC Set		
Address	3015H	I/O	OUT



Rd	Wr	Operation
0	0	Verify DMA cycle
0	1	Write DMA cycle
1	0	Read DMA cycle
1	1	

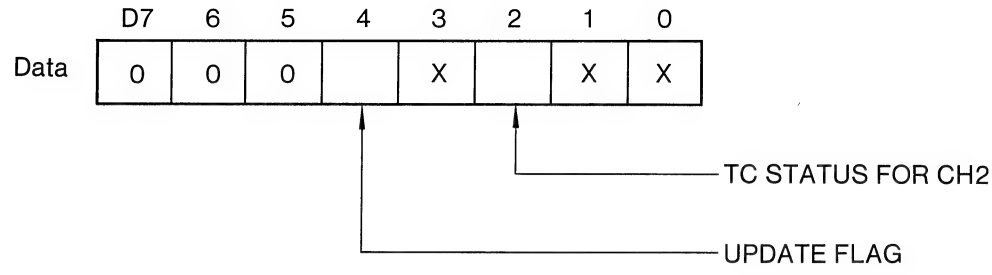
This command is used to set the initial value in the DMAC (μPD8257C) terminal counter (14-bit).
DMA channel 2 is used.

Command	DMAC Mode Set		
Address	3018H	I/O	OUT



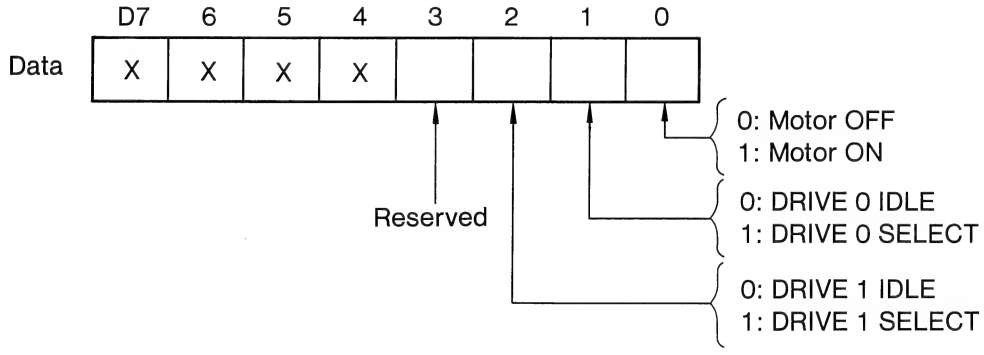
This command is used to set the mode set register for DMAC (μPD8257C). Normally, DISABLE TC STOP and DISABLE AUTO LOAD are set.

Command	DMAC Status Reg. Read		
Address	3018H	I/O	INP



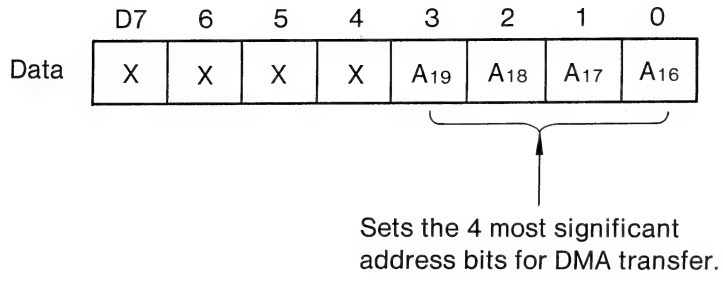
This command is used to read from the DMAC (μPD8237C) status register.

Command	EXT FF Set		
Address	3050H	I/O	OUT

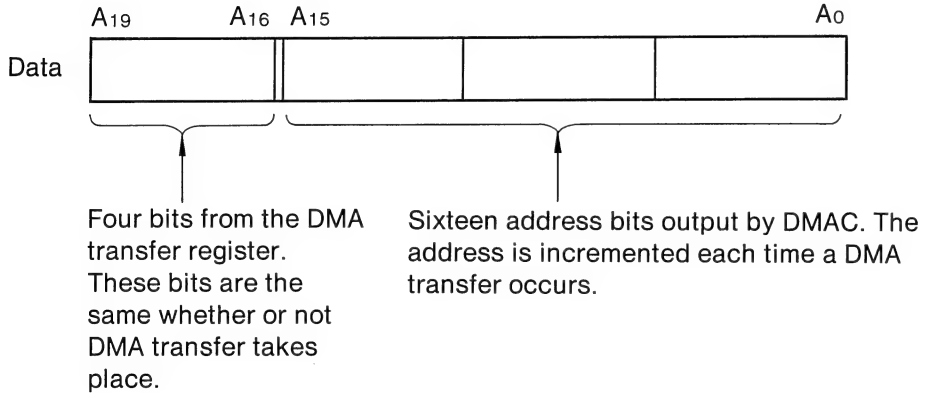


This command is used to turn the floppy-disk unit motor on and off, and to select the drive mode.

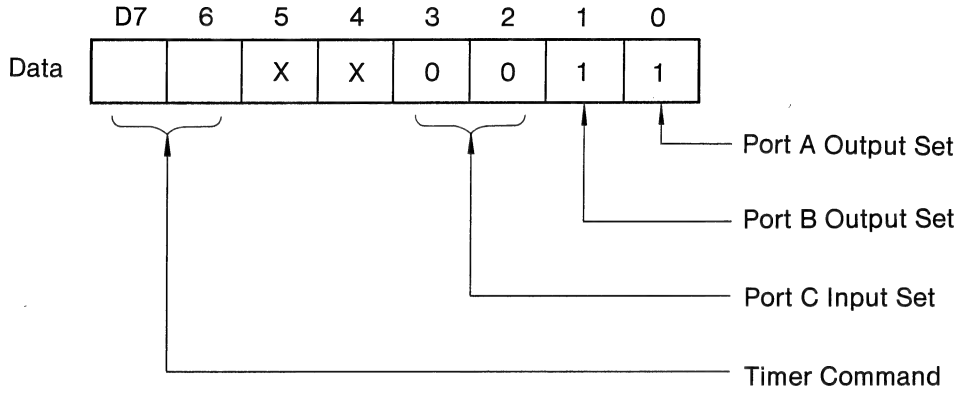
Command	DMA Transfer Reg. Set		
Address	3060H	**I/O**	OUT



This command is used to set the 4 most significant memory address bits for use during DMA transfer.
The configuration of the memory address is shown below.



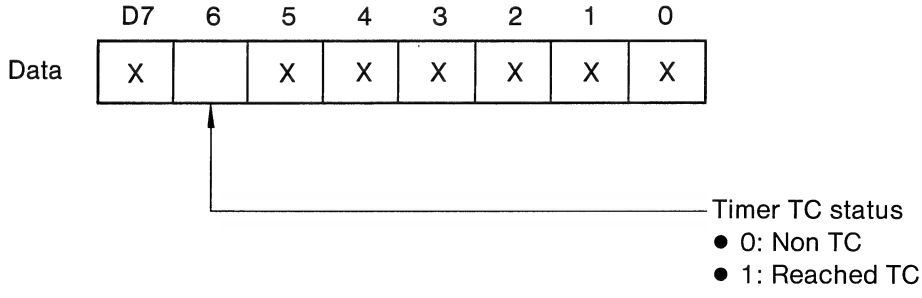
Command	Port 1 Command Set		
Address	4000H	I/O	OUT



D7	D6	
0	0	..... No Operation
0	1	..... Timer Stop
1	0	..... Stop after TC
1	1	..... Timer Start

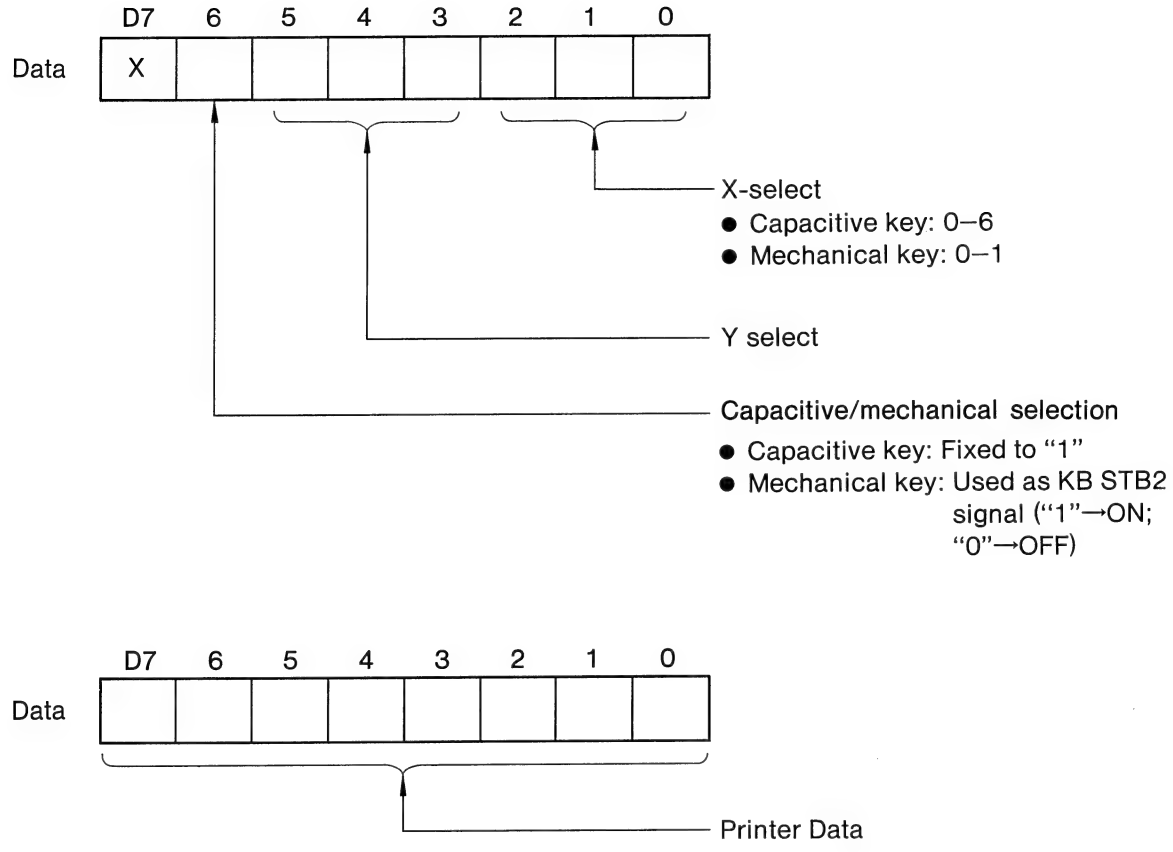
This command is used to define the 81C55 general-purpose port as an input or an output port, and to start and stop the built-in timer.

Command	Port 1 Status Read		
Address	4000H	I/O	INP



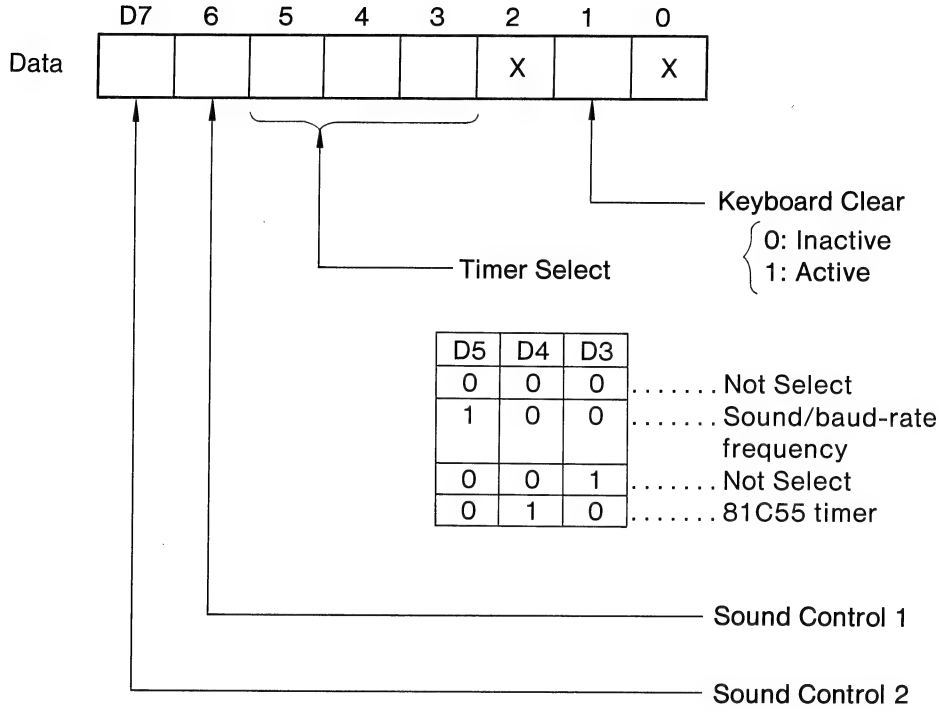
The timer TC status bit is set to "1" when the 81C55 timer is set.
The bit is automatically reset to "0" after the status bit is read.

Command	Out Port A Data Set/Out Port A Data Read		
Address	4001H	**I/O**	OUT/INP



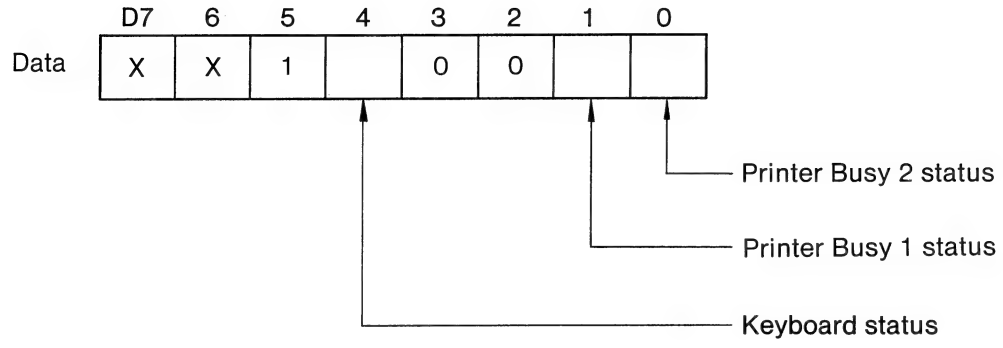
OUT PORT A is assigned to port A of 81C55, and handles two types of data:
(1) **KB address set.** Sets the address and executes the KB strobe command.
(2) **PRINT data set.** Sets the data and executes the printer strobe command.
Note: The data that is set by the OUT PORT A DATA SET command is read by the OUT PORT A DATA READ command.

Command	Out Port B Data Set/Out Port B Data Read		
Address	4002H	**I/O**	OUT/INP



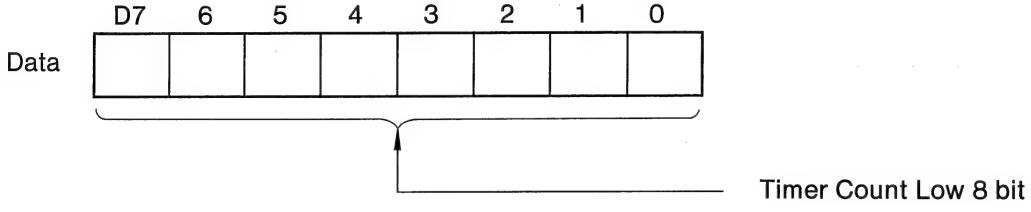
81C55 port B is assigned as OUT PORT B. Various I/Os are controlled through this port. The OUT PORT B DATA READ command is used to read the data that was set using the OUT PORT B DATA SET command.

Command	In Port C Data Read		
Address	4003H	**I/O**	INP



81C55 port C is assigned as IN PORT C.
The command is used to read the printer and keyboard status.

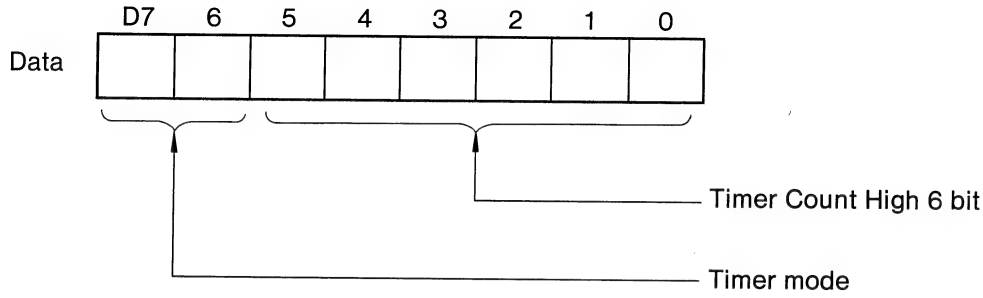
Command	Timer Count Low Set/Timer Count Low Read		
Address	4004H	**I/O**	OUT/INP



This count value of the 81C55 built-in timer is comprised of 14 bits.

- **TIMER COUNT LOW SET.** Sets the 8 least significant bits.
- **TIMER COUNT LOW READ.** Reads the 8 least significant bits of the current count value.

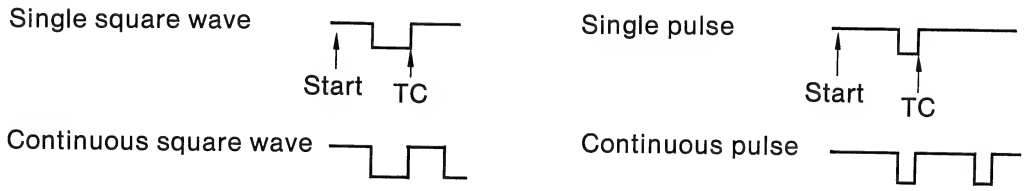
Command	Timer Mode Count High Set/Timer Mode Count High Read		
Address	4005H	**I/O**	OUT/INP



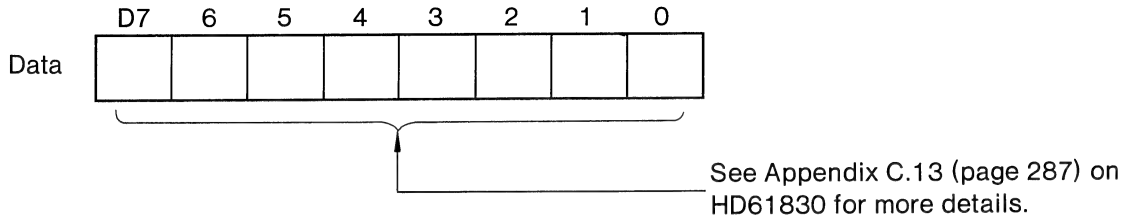
D6	D7	
0	0	..... Single square wave
0	1	..... Continuous square wave
1	0	..... Single pulse on TC
1	1	..... Continuous TC pulse

The data set in D0-D5 is used as the 4 most significant bits of the built-in timer's count value.
The data set in D6 and D7 defines the timer mode.

- **TIMER MODE-COUNT HIGH SET.** Sets the timer mode and the 4 most significant bits.
- **TIMER MODE-COUNT HIGH READ.** Relationship between the mode and output waveform:

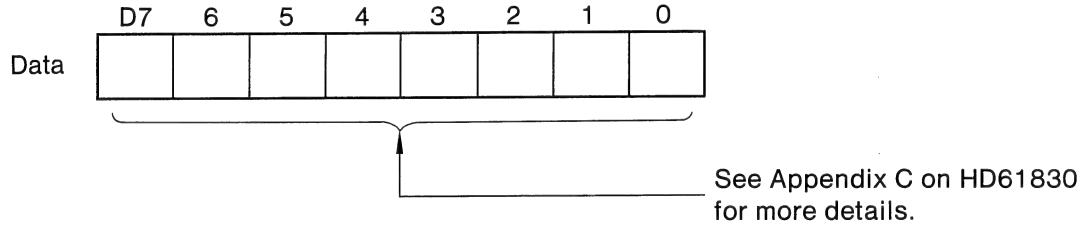


Command	LCDC1 Data Set/LCDC1 Data Read		
Address	8000H	**I/O**	OUT/INP



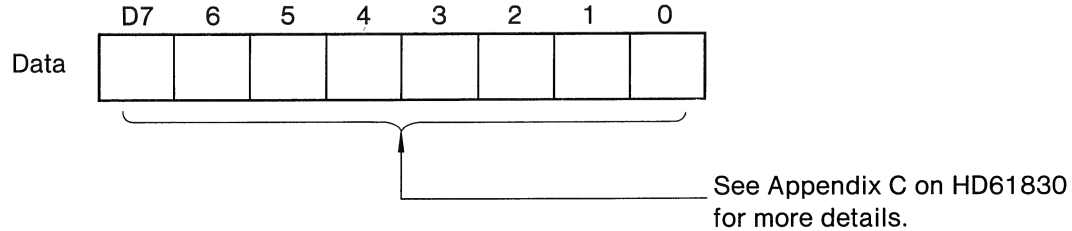
This is the data register for the master HD61830.

Command	LCDC1 Instruction Set		
Address	8010H	**I/O**	OUT



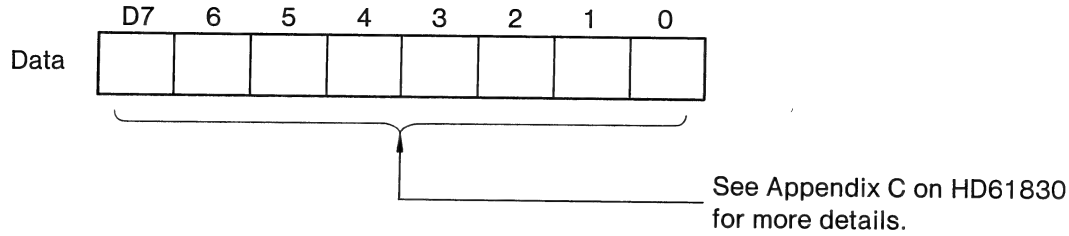
This is the instruction register for the master HD61830.

Command	LCDC2 Data Set/LCDC2 Data Read		
Address	9000H	**I/O**	OUT/INP



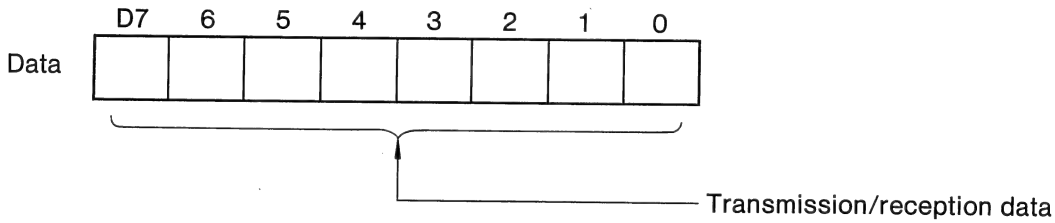
This is the data register for the slave HD61830.

Command	LCDC2 Instruction Set		
Address	9020H	I/O	OUT



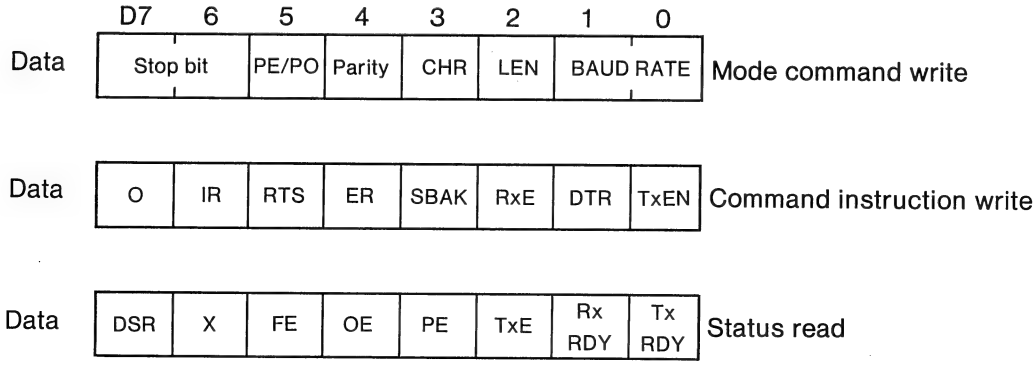
This is the instruction register for the slave HD61830.

Command	USART Data set/USART Data Read		
Address	A000H	I/O	OUT/INP



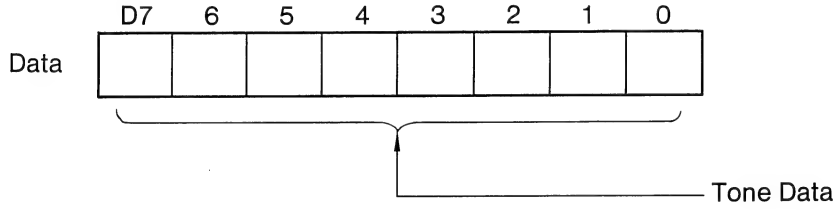
This is the data register for 82C51.

Command	USART Command Set/USART Status Read		
Address	A040H	I/O	OUT/INP



This is the control register/status register for 82C51.

Command	DTMF Set		
Address	B000H	**I/O**	OUT

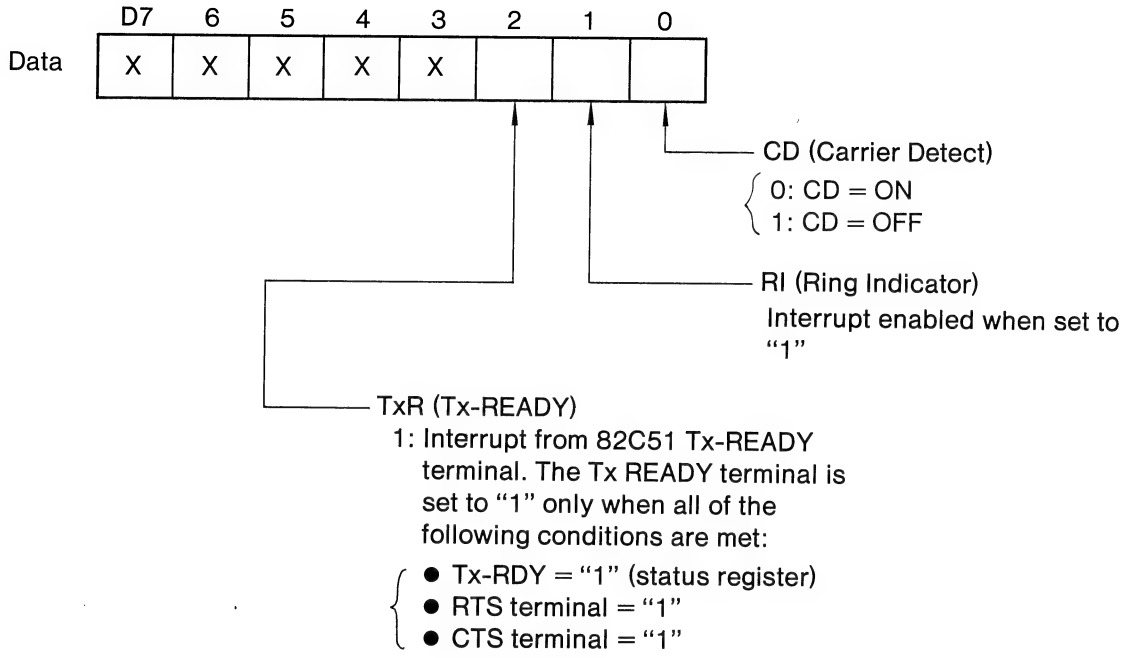


This command controls DTMF of MSM6234RS.

Telephone number	Tone Data	High frequency	Low frequency
0	7D	1336 (1331.7)	941 (948.0)
1	EE	1209 (1215.9)	697 (699.1)
2	ED	1336 (1331.7)	697 (699.1)
3	EB	1477 (1471.9)	697 (699.1)
4	DE	1209 (1215.9)	770 (766.2)
5	DD	1336 (1331.7)	770 (766.2)
6	DB	1477 (1471.9)	770 (766.2)
7	BE	1209 (1215.9)	852 (847.4)
8	BD	1336 (1331.7)	852 (847.4)
9	BB	1477 (1471.9)	852 (847.4)
*	7E	1209 (1215.9)	941 (948.0)
#	7B	1477 (1471.9)	941 (948.0)

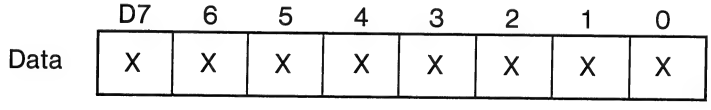
Note: The standard frequency is listed outside the parentheses. The designed frequency is enclosed in parentheses.

Command	In Port E Read		
Address	B000H	I/O	INP



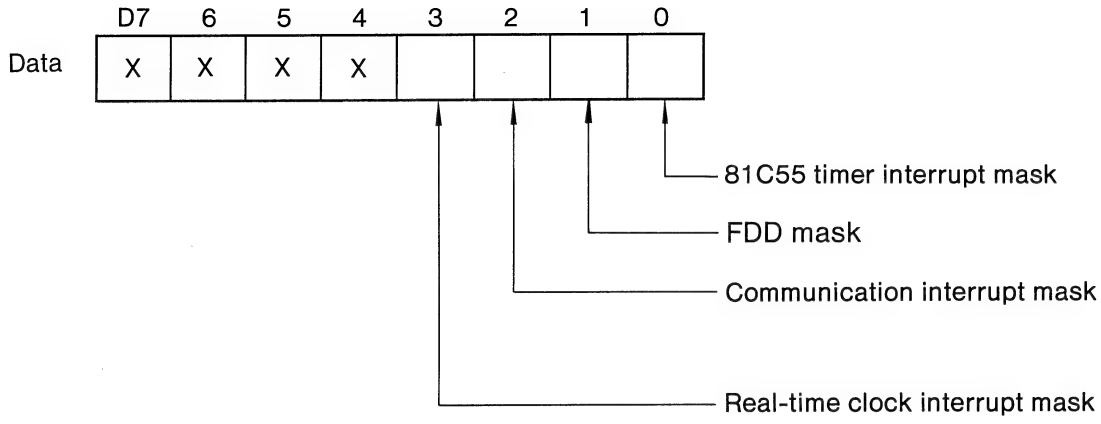
IN PORT E is assigned to an external register. The port senses a communication I/O interrupt generated by this command.

Command	TRC IPT Clear		
Address	B200H	I/O	OUT



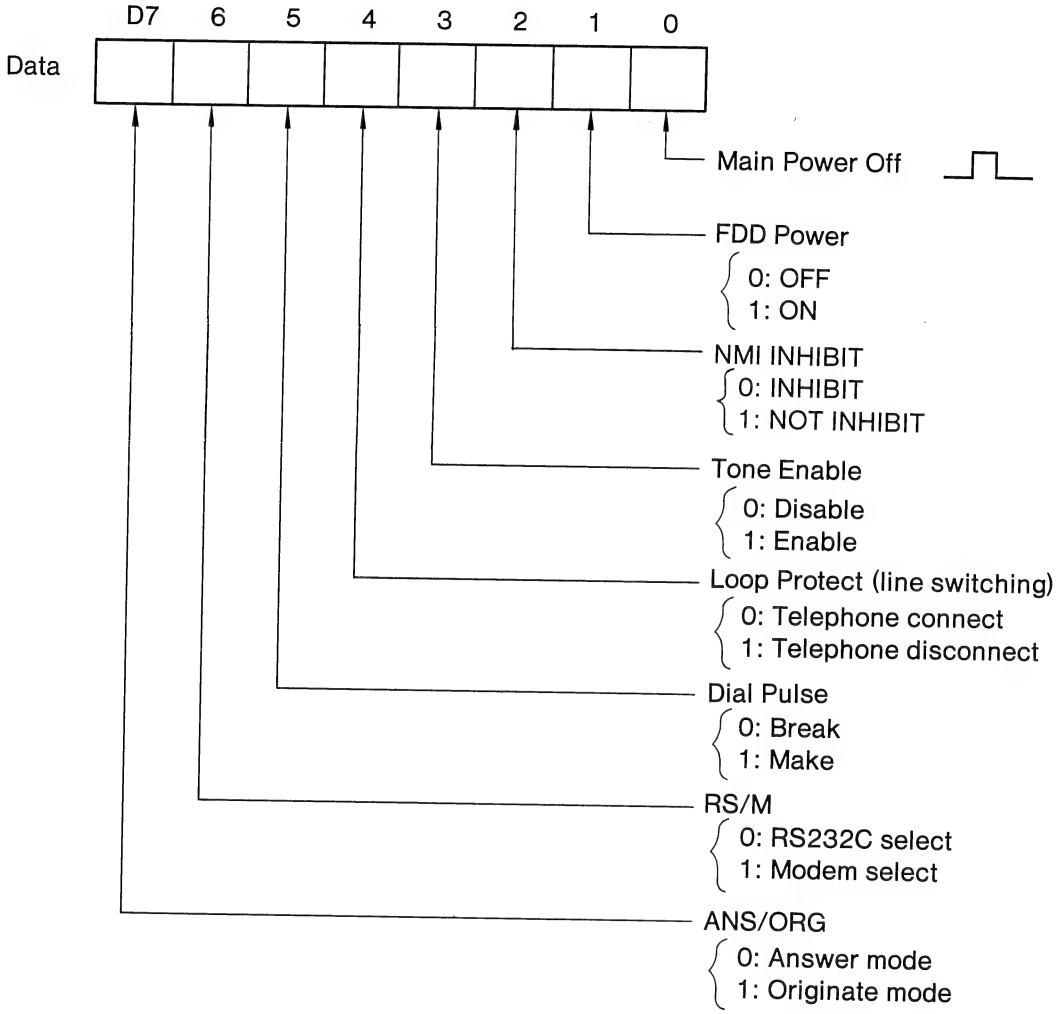
This command clears the communication I/O interrupt.

Command	IPT Mask Set		
Address	B400H	**I/O**	OUT



This command is used to mask interrupts.
By setting "1" in the bit for the appropriate interrupt to be masked, the corresponding I/O interrupt is disabled. All the bits are set to "0" when the power is turned on or when the system is reset.

Command	Out Port D Data set		
Address	B600H	I/O	OUT

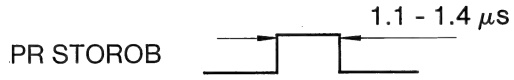


OUT PORT D is assigned to an external register, and is used to control communication and the power supply.

Command	Printer Strobe		
Address	B800H	I/O	OUT

	D7	6	5	4	3	2	1	0
Data	X	X	X	X	X	X	X	X

This command is executed to output the PR STROBE pulse for the printer interface.



Command	KB Strobe (for capacitive keys)		
Address	BA00H	I/O	OUT

	D7	6	5	4	3	2	1	0
Data	X	X	X	X	X	X	X	X

Keyboard KBSTB1 pulse is generated when this command is executed.

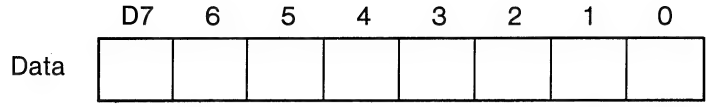


Command	81C55 Timer IPT Clear		
Address	BC00H	I/O	INP

	D7	6	5	4	3	2	1	0
Data	X	X	X	X	X	X	X	X

If the 81C55 timer is used as a general-purpose timer, the terminal count pulse is latched and the latched terminal count pulse is used as the interrupt signal. This command is used to clear the interrupt signal.

Command	HD146818 (RTC) Related Command		
Address	C000H ~ C03FH	**I/O**	OUT/INP



This command is used to access the HD146818 (RTC) 64-byte internal RAM. See Appendix C.4 (page 249) for details.

APPENDIX B

APPENDIX B – – CHARACTER CODE TABLE

Decimal	Hexa-decimal	Binary	Printed Character	Key Top Character
0	00	00000000	Space	[CTRL]+[2]
1	01	00000001	☺	[CTRL]+[A]
2	02	00000010	☻	[CTRL]+[B]
3	03	00000011	♥	[CTRL]+[C]
4	04	00000100	♦	[CTRL]+[D]
5	05	00000101	♣	[CTRL]+[E]
6	06	00000110	♠	[CTRL]+[F]
7	07	00000111	•	[CTRL]+[G]
8	08	00001000	Backspace	[CTRL]+[H]
9	09	00001001	Tab	[CTRL]+[I]
10	0A	00001010	◘	[CTRL]+[J]
11	0B	00001011	♂	[CTRL]+[K]
12	0C	00001100	♀	[CTRL]+[L]
13	0D	00001101	Carriage Return	[CTRL]+[M]
14	0E	00001110	♫	[CTRL]+[N]
15	0F	00001111	☼	[CTRL]+[O]
16	10	00010000	►	[CTRL]+[P]
17	11	00010001	◄	[CTRL]+[Q]
18	12	00010010	↕	[CTRL]+[R]
19	13	00010011	!!	[CTRL]+[S]
20	14	00010100	¶	[CTRL]+[T]
21	15	00010101	§	[CTRL]+[U]
22	16	00010110	▬	[CTRL]+[V]
23	17	00010111	↨	[CTRL]+[W]
24	18	00011000	↑	[CTRL]+[X]
25	19	00011001	↓	[CTRL]+[Y]
26	1A	00011010	→	[CTRL]+[Z]
27	1B	00011011	←	[ESC]
28	1C	00011100	∟	[CTRL]+[>]
29	1D	00011101	↔	[CTRL]+[ ]]
30	1E	00011110	▲	[CTRL]+[6]

Decimal	Hexa-decimal	Binary	Printed Character	Key Top Character
31	1F	00011111	▼	[CTRL]+[_]
32	20	00100000	(Space)	[Space]
33	21	00100001	!	[!]
34	22	00100010	"	[″]
35	23	00100011	#	[#]
36	24	00100100	$	[$]
37	25	00100101	%	[%]
38	26	00100110	&	[&]
39	27	00100111	′	[′]
40	28	00101000	(	[(]
41	29	00101001	)	[)]
42	2A	00101010	*	[*]
43	2B	00101011	+	[+]
44	2C	00101100	,	[’]
45	2D	00101101	−	[-]
46	2E	00101110	.	[·]
47	2F	00101111	/	[/]
48	30	00110000	0	[0]
49	31	00110001	1	[1]
50	32	00110010	2	[2]
51	33	00110011	3	[3]
52	34	00110100	4	[4]
53	35	00110101	5	[5]
54	36	00110110	6	[6]
55	37	00110111	7	[7]
56	38	00111000	8	[8]
57	39	00111001	9	[9]
58	3A	00111010	:	[:]
59	3B	00111011	;	[;]
60	3C	00111100	<	[<]
61	3D	00111101	=	[=]
62	3E	00111110	>	[>]
63	3F	00111111	?	[?]

Decimal	Hexa-decimal	Binary	Printed Character	Key Top Character
64	40	01000000	@	[@]
65	41	01000001	A	[A]
66	42	01000010	B	[B]
67	43	01000011	C	[C]
68	44	01000100	D	[D]
69	45	01000101	E	[E]
70	46	01000110	F	[F]
71	47	01000111	G	[G]
72	48	01001000	H	[H]
73	49	01001001	I	[I]
74	4A	01001010	J	[J]
75	4B	01001011	K	[K]
76	4C	01001100	L	[L]
77	4D	01001101	M	[M]
78	4E	01001110	N	[N]
79	4F	01001111	O	[O]
80	50	01010000	P	[P]
81	51	01010001	Q	[Q]
82	52	01010010	R	[R]
83	53	01010011	S	[S]
84	54	01010100	T	[T]
85	55	01010101	U	[U]
86	56	01010110	V	[V]
87	57	01010111	W	[W]
88	58	01011000	X	[X]
89	59	01011001	Y	[Y]
90	5A	01011010	Z	[Z]
91	5B	01011011	[	[[ ]
92	5C	01011100	\	[CTRL]+[/]
93	5D	01011101	]	[ ]]
94	5E	01011110	^	[ê]
95	5F	01011111	_	[_]
96	60	01100000	`	[è]

Decimal	Hexa-decimal	Binary	Printed Character	Key Top Character
97	61	01100001	a	[a]
98	62	01100010	b	[b]
99	63	01100011	c	[c]
100	64	01100100	d	[d]
101	65	01100101	e	[e]
102	66	01100110	f	[f]
103	67	01100111	g	[g]
104	68	01101000	h	[h]
105	69	01101001	i	[i]
106	6A	01101010	j	[j]
107	6B	01101011	k	[k]
108	6C	01101100	l	[l]
109	6D	01101101	m	[m]
110	6E	01101110	n	[n]
111	6F	01101111	o	[o]
112	70	01110000	p	[p]
113	71	01110001	q	[q]
114	72	01110010	r	[r]
115	73	01110011	s	[s]
116	74	01110100	t	[t]
117	75	01110101	u	[u]
118	76	01110110	v	[v]
119	77	01110111	w	[w]
120	78	01111000	x	[x]
121	79	01111001	y	[y]
122	7A	01111010	z	[z]
123	7B	01111011	{	[CTRL]+[9]
124	7C	01111100	¦	[CTRL]+[:]
125	7D	01111101	}	[CTRL]+[0]
126	7E	01111110	~	[CTRL]+[=]
127	7F	01111111	Space	[CTRL]+[BKSP]
128	80	10000000	Ç	[SHIFT]+[ALT]+[F]
129	81	10000001	ü	[SHIFT]+[CTRL]+[U]

Decimal	Hexa-decimal	Binary	Printed Character	Key Top Character
130	82	10000010	é	[SHIFT]+[CTRL]+[D]
131	83	10000011	â	[SHIFT]+[CTRL]+[1]
132	84	10000100	ä	[SHIFT]+[CTRL]+[Q]
133	85	10000101	à	[SHIFT]+[CTRL]+[Z]
134	86	10000110	å	[SHIFT]+[CTRL]+[A]
135	87	10000111	ç	[SHIFT]+[CTRL]+[F]
136	88	10001000	ê	[SHIFT]+[CTRL]+[3]
137	89	10001001	ë	[SHIFT]+[CTRL]+[E]
138	8A	10001010	è	[SHIFT]+[CTRL]+[C]
139	8B	10001011	ï	[SHIFT]+[CTRL]+[I]
140	8C	10001100	î	[SHIFT]+[CTRL]+[8]
141	8D	10001101	ì	[SHIFT]+[CTRL]+[<]
142	8E	10001110	Ä	[SHIFT]+[ALT]+[Q]
143	8F	10001111	Å	[SHIFT]+[ALT]+[W]
144	90	10010000	É	[SHIFT]+[ALT]+[D]
145	91	10010001	æ	[SHIFT]+[CTRL]+[X]
146	92	10010010	Æ	[SHIFT]+[ALT]+[X]
147	93	10010011	ô	[SHIFT]+[CTRL]+[9]
148	94	10010100	ö	[SHIFT]+[CTRL]+[O]
149	95	10010101	ò	[SHIFT]+[CTRL]+[>]
150	96	10010110	û	[SHIFT]+[CTRL]+[7]
151	97	10010111	ù	[SHIFT]+[CTRL]+[M]
152	98	10011000	ÿ	[SHIFT]+[CTRL]+[Y]
153	99	10011001	Ö	[SHIFT]+[ALT]+[O]
154	9A	10011010	Ü	[SHIFT]+[ALT]+[U]
155	9B	10011011	¢	[SHIFT]+[ALT]+[4]
156	9C	10011100	£	[SHIFT]+[ALT]+[3]
157	9D	10011101	¥	[SHIFT]+[CTRL]+[6]
158	9E	10011110	Pt	[SHIFT]+[CTRL]+[4]
159	9F	10011111	f	[SHIFT]+[ALT]+[C]
160	A0	10100000	á	[SHIFT]+[CTRL]+[A]
161	A1	10100001	í	[SHIFT]+[CTRL]+[K]
162	A2	10100010	ó	[SHIFT]+[CTRL]+[L]

Decimal	Hexa-decimal	Binary	Printed Character	Key Top Character
163	A3	10100011	ㄩ	[SHIFT]+[CTRL]+[J]
164	A4	10100100	ㄋ	[SHIFT]+[CTRL]+[N]
165	A5	10100101	ㄋ	[SHIFT]+[ALT]+[N]
166	A6	10100110	ㄦ	[SHIFT]+[CTRL]+[2]
167	A7	10100111	ㄛ	[SHIFT]+[CTRL]+[0]
168	A8	10101000	¿	[SHIFT]+[ALT]+[?]
169	A9	10101001	ㄱ	[SHIFT]+[ALT]+[6]
170	AA	10101010	ㄱ	[SHIFT]+[ALT]+[7]
171	AB	10101011	½	[SHIFT]+[CTRL]+[?]
172	AC	10101100	¼	[SHIFT]+[CTRL]+[P]
173	AD	10101101	¡	[SHIFT]+[ALT]+[1]
174	AE	10101110	«	[SHIFT]+[ALT]+[K]
175	AF	10101111	»	[SHIFT]+[ALT]+[L]
176	B0	10110000	⁞	[CTRL]+[ALT]+[1]
177	B1	10110001	⁞	[CTRL]+[ALT]+[Q]
178	B2	10110010	⁞	[CTRL]+[ALT]+[DEL]
179	B3	10110011	ㅣ	[CTRL]+[ALT]+[M]
180	B4	10110100	ㅓ	[CTRL]+[ALT]+[B]
181	B5	10110101	ㅕ	[CTRL]+[ALT]+[5]
182	B6	10110110	ㅢ	[CTRL]+[ALT]+[T]
183	B7	10110111	ㅋ	[CTRL]+[ALT]+[7]
184	B8	10111000	ㅋ	[CTRL]+[ALT]+[P]
185	B9	10111001	ㅢ	[CTRL]+[ALT]+[G]
186	BA	10111010	ㅣ	[CTRL]+[ALT]+[J]
187	BB	10111011	ㅋ	[CTRL]+[ALT]+[K]
188	BC	10111100	ㅠ	[CTRL]+[ALT]+[I]
189	BD	10111101	ㅠ	[CTRL]+[ALT]+[8]
190	BE	10111110	ㅓ	[CTRL]+[ALT]+[+]
191	BF	10111111	ㄱ	[CTRL]+[ALT]+[<]
192	C0	11000000	ㄴ	[CTRL]+[ALT]+[”]
193	C1	11000001	ㅗ	[CTRL]+[ALT]+[X]
194	C2	11000010	ㅜ	[CTRL]+[ALT]+[C]
195	C3	11000011	ㅏ	[CTRL]+[ALT]+[V]

Decimal	Hexa-decimal	Binary	Printed Character	Key Top Character
196	C4	11000100	─	[CTRL]+[ALT]+[Z]
197	C5	11000101	┼	[CTRL]+[ALT]+[N]
198	C6	11000110	╞	[CTRL]+[ALT]+[4]
199	C7	11000111	╟	[CTRL]+[ALT]+[R]
200	C8	11001000	╚	[CTRL]+[ALT]+[0]
201	C9	11001001	╔	[CTRL]+[ALT]+[L]
202	CA	11001010	╩	[CTRL]+[ALT]+[S]
203	CB	11001011	╦	[CTRL]+[ALT]+[D]
204	CC	11001100	╠	[CTRL]+[ALT]+[F]
205	CD	11001101	═	[CTRL]+[ALT]+[A]
206	CE	11001110	╬	[CTRL]+[ALT]+[H]
207	CF	11001111	╧	[CTRL]+[ALT]+[W]
208	D0	11010000	╨	[CTRL]+[ALT]+[2]
209	D1	11010001	╤	[CTRL]+[ALT]+[E]
210	D2	11010010	╥	[CTRL]+[ALT]+[3]
211	D3	11010011	╙	[CTRL]+[ALT]+[0]
212	D4	11010100	╘	[CTRL]+[ALT]+[ ]]
213	D5	11010101	╒	[CTRL]+[ALT]+[_]
214	D6	11010110	╓	[CTRL]+[ALT]+[9]
215	D7	11010111	╫	[CTRL]+[ALT]+[Y]
216	D8	11011000	╪	[CTRL]+[ALT]+[6]
217	D9	11011001	┘	[CTRL]+[ALT]+[:]
218	DA	11011010	┌	[CTRL]+[ALT]+[>]
219	DB	11011011	■	[SHIFT]+[ALT]+[E]
220	DC	11011100	▄	[SHIFT]+[ALT]+[R]
221	DD	11011101	▌	[SHIFT]+[ALT]+[H]
222	DE	11011110	▐	[SHIFT]+[ALT]+[Y]
223	DF	11011111	▀	[SHIFT]+[ALT]+[T]
224	E0	11100000	α	[SHIFT]+[CTRL]+[5]
225	E1	11100001	ß	[SHIFT]+[CTRL]+[B]
226	E2	11100010	Γ	[SHIFT]+[CTRL]+[G]
227	E3	11100011	π	[SHIFT]+[CTRL]+[ ]]
228	E4	11100100	Σ	[SHIFT]+[ALT]+[S]

Decimal	Hexa-decimal	Binary	Printed Character	Key Top Character
229	E5	11100101	σ	[SHIFT]+[CTRL]+[S]
230	E6	11100110	μ	[SHIFT]+[ALT]+[ ]]
231	E7	11100111	τ	[SHIFT]+[CTRL]+[T]
232	E8	11101000	Φ	[SHIFT]+[ALT]+[V]
233	E9	11101001	Θ	[SHIFT]+[ALT]+[G]
234	EA	11101010	Ω	[SHIFT]+[CTRL]+[H]
235	EB	11101011	δ	[SHIFT]+[CTRL]+[R]
236	EC	11101100	∞	[SHIFT]+[ALT]+[5]
237	ED	11101101	ø	[SHIFT]+[CTRL]+[V]
238	EE	11101110	∈	[SHIFT]+[ALT]+["]
239	EF	11101111	∩	[SHIFT]+[CTRL]+["]
240	F0	11110000	≡	[SHIFT]+[CTRL]+[+]
241	F1	11110001	±	[SHIFT]+[ALT]+[+]
242	F2	11110010	≥	[SHIFT]+[ALT]+[>]
243	F3	11110011	≤	[SHIFT]+[ALT]+[<]
244	F4	11110100	⌠	[SHIFT]+[ALT]+[:]
245	F5	11110101	⌡	[SHIFT]+[CTRL]+[:]
246	F6	11110110	÷	[SHIFT]+[ALT]+[9]
247	F7	11110111	≈	[SHIFT]+[CTRL]+[_]
248	F8	11111000	°	[SHIFT]+[ALT]+[0]
249	F9	11111001	∙	[SHIFT]+[ALT]+[|]
250	FA	11111010	·	[SHIFT]+[ALT]+[P]
251	FB	11111011	√	[SHIFT]+[ALT]+[_]
252	FC	11111100	n	[SHIFT]+[ALT]+[8]
253	FD	11111101	2	[SHIFT]+[ALT]+[2]
254	FE	11111110	■	[SHIFT]+[ALT]+[J]
255	FF	11111111	Space	[SHIFT]+[CTRL]+[BKSP]

APPENDIX C

APPENDIX C – – DOCUMENTATION OF MICROPROCESSOR AND LSI

C.1 MSM80C88

8-BIT CMOS Microprocessor

(1) Overview

– 8-bit data bus interface
– 16-bit internal architecture
– 1M byte directly addressable memory
– Software compatible with MSM80C86
– Internal 14-word by 16-bit register set
– 24 operand addressing mode
– Bit, byte, word and string operations
– 8- and 16-bit signed and unsigned arithmetic operation
– 5 MHz clock rate
– Low power dissipation

(2) Terminal Connection and Circuit Layout

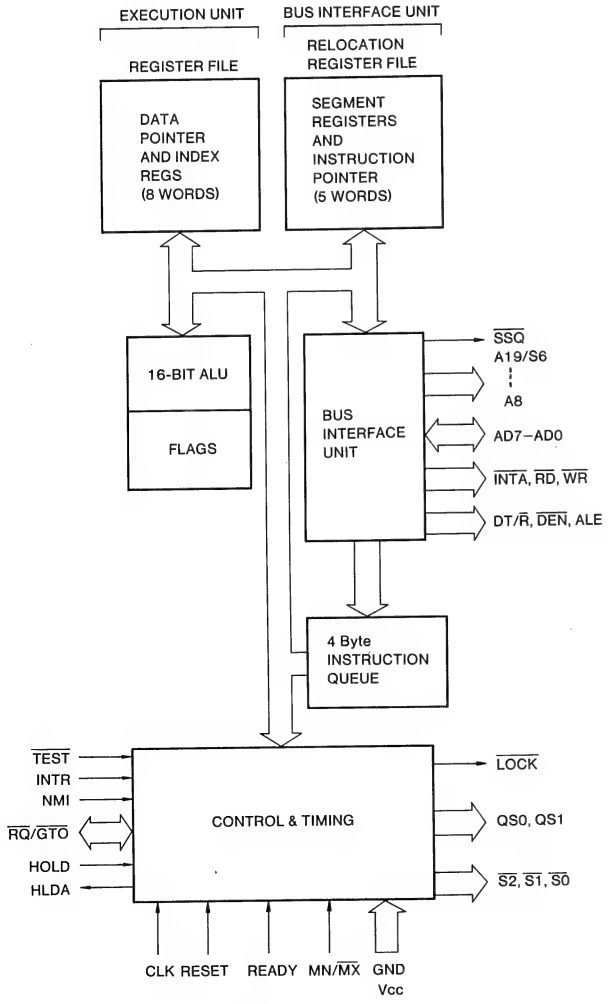


Figure C-1. MSM80C88 Block Diagram

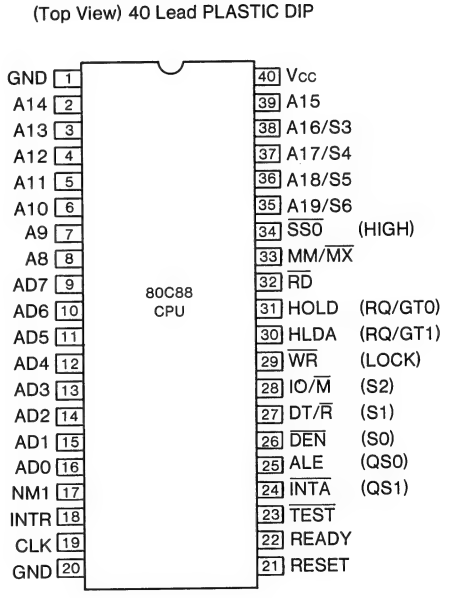


Figure C-2. MSM80C88 Pin Configuration

(3) Pin Description

AD0-AD7

ADDRESS/DATA BUS: Input/Output

These lines form a multiplexed address and data bus. The address bus uses the T1 cycle and the data bus uses the T2, T3, TW and T4 cycles. The impedance level on these lines is HIGH during interrupt acknowledge and hold acknowledge.

A8-A15

ADDRESS BUS: Output

These lines form an address bus for bits 8-15 at all cycles and need not be latched by the ALE signal. The impedance level is HIGH during interrupt acknowledge and hold acknowledge.

A16/S3, A17/S4, A18/S5, A19/S6

ADDRESS/STATUS: Output

These lines are for the four most significant addresses at the T1 cycle. When the impedance is LOW in the T1 cycle, they access the I/O port address. In the T2, T3, TW and T4 cycles, they are status lines. S5 indicates the interrupt enable flag. S3 and S4 are encoded as follows:

S3	S4	CHARACTERISTIC
0	0	Alternate data
1	0	Stack
0	1	Code or None
1	1	Data

Table C-1. S3 and S4 Signals

These lines are at a HIGH impedance level during hold acknowledge.

$\overline{RD}$

EAD: Output

This line indicates that the CPU is in the memory or the I/O read cycle. The line carries a read strobe signal when the CPU is reading data from memory or an I/O device. The line is active when the impedance level is LOW; it is on hold acknowledge when the impedance is HIGH.

READY

READY: Input

This line indicates to the CPU that an addressed memory or I/O device is ready to read or write. When the signal is HIGH, the line is active. If the setup and hold time are outside the specified range, an error results.

INTR
INTERRUPT REQUEST: Input
This line is for a level-triggered-interrupt-request signal that is sampled during the last clock cycle of an instruction or a string manipulation. It can be internally masked by software. The line is active when the signal is HIGH and internally synchronized.

$\overline{\text{TEST}}$
TEST: Input
This line is checked by the WAIT instruction. When TEST is HIGH, the CPU enters the idle cycle. When TEST is LOW, the CPU exits the idle cycle.

NMI
NON MASKABLE INTERRUPT: Input
This line causes a type-2 interrupt and is not maskable.

This signal is internally synchronized with the pulse width equal to two clock cycles.

RESET
RESET: Input
This signal causes the CPU to initialize immediately. This signal is active at HIGH and must be at least four clock cycles.

CLK
CLOCK: Input
This signal provide the basic timing for the internal circuits.

MN/$\overline{\text{MX}}$
MINIMUM/MAXIMUM: Input
This signal selects the CPU's operating mode. When Vcc is connected, the CPU operates in the minimum mode. When GND is connected, the CPU operates in the maximum mode.

VCC
VCC:
+3 – +6V supplied.

GND
GROUND

The following pin-function descriptions are for the minimum mode only. Other pin functions have already been described.

IO/$\overline{M}$
STATUS: Output
This line selects the memory or I/O address. When the signal on this line is LOW, the CPU selects a memory address. When this line is HIGH, the CPU selects an I/O address. The impedance level is HIGH during hold acknowledge.

$\overline{WR}$
WRITE: Output
This line indicates that the CPU is in a memory or I/O write cycle. When the CPU is writing data into memory or to an I/O device, the line is characterized by a write-strobe signal. A LOW signal indicates that the line is active. A HIGH impedance level indicates hold acknowledge.

$\overline{INTA}$
INTERRUPT ACKNOWLEDGE: Output
It is active at a LOW signal. A HIGH impedance level indicates hold acknowledge cycle.

ALE
ADDRESS LATCH ENABLE: Output
This line is used for latching an address into the 82C12 address latch. The pulse is positive and the trailing edge is used to strobe the address. This line is never floated.

DT/$\overline{R}$
DATA TRANSMIT/RECEIVE: Output
This line is used to control the direction of the bus transceiver. When the signal is HIGH, the CPU is transmitting data. When it is LOW, the CPU is receiving data. The impedance level is HIGH during hold acknowledge.

$\overline{DEN}$
DATA ENABLE: Output
This line is used to control the output enable for the bus transceiver. It is active at a LOW signal. The impedance level is HIGH at hold acknowledge.

HOLD
HOLD REQUEST: Input
This is the bus request line from other devices and is active at a HIGH signal level.

HLDA
HOLD ACKNOWLEDGE: Output
This is the bus grant line to other devices and is active at a HIGH signal level.

$\overline{SS0}$
STATUS: Output
This line is logically equivalent to S0 in the maximum mode.

S0, S1, S2
STATUS: Output
These lines indicate bus status and are used by the 82C88 bus controller to generate all memory and I/O access control signals. These lines are HIGH level during hold acknowledge. The status is encoded as follows:

S2	S1	S0	CHARACTERISTIC
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1 (HIGH)	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

Table C-2. S0, S1 and S2 Signals

$\overline{RQ}$/$\overline{GT0}$
$\overline{RQ}$/$\overline{GT1}$
REQUEST/GRANT: Input/Output
These lines are used for bus requests from other devices and bus grants to other devices. They are bidirectional and active when the signal is LOW.

$\overline{LOCK}$
LOCK: Output
This line is active when the signal is LOW, which indicates that another device could not gain control of the bus. The impedance level on this line is HIGH during hold acknowledge.

QS0/QS1
QUEUE STATUS: Output
These lines indicate the internal instruction queue status, as follows:

QS1	QS0	CHARACTERISTIC
0 (LOW)	0	No operation
0	1	First byte of op code from queue
1 (HIGH)	0	Empty queue
1	1	Subsequent byte from queue

Table C-3. QS0 and QS1 Signals

(4) Functional Description

■ General operation

The MSM80C88 consists of the Bus Interface Unit (BIU) and the Execution Unit (EU). These units operate together, but function as separate processors.

The BIU performs instruction fetch and queuing, operand fetch, DATA read and write address relocation, and basic bus control. By issuing a prefetch instruction while waiting for decoding and execution of the previous instruction, CPU performance is enhanced.

Up to four bytes of instruction stream can be queued.

The EU receives a prefetch instruction from the BIU queue, decodes and executes it, and provides an unrelocated operand address to the BIU.

■ Memory organization

The MSM80C88 is based on 20-bit, memory-addressing. Each address includes eight bytes of data. Memory is organized from 00000H to FFFFFH and is logically divided into four segments: code, data, external data and stack. The size of each segment is 64K bytes, located at a 16-byte boundary (see Figure C-3).

All memory references are relative to the segment register, based on the segment selection rule. Memory location FFFF0H is the beginning address after reset, while 00000H through 003FFH are reserved for interrupt pointers, of which there are 256.

Each interrupt type has a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address.

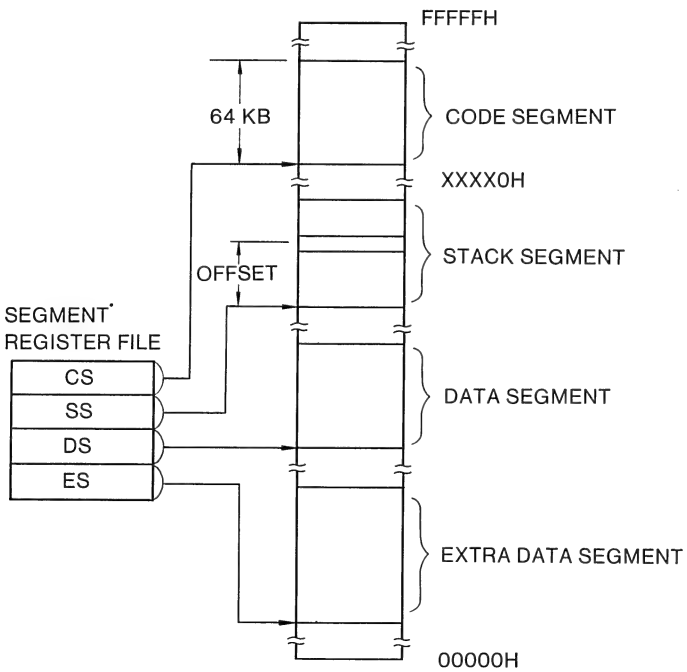


Figure C-3a. Memory Organization

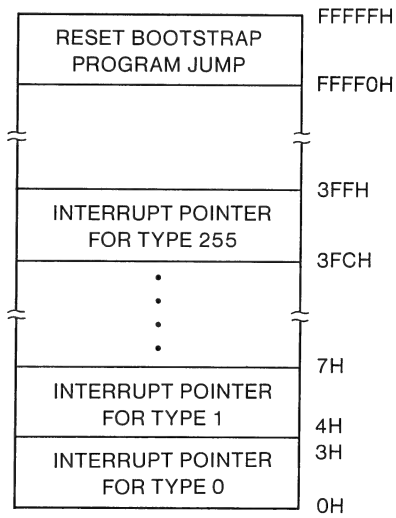


Figure C-3b. Reserved Memory Locations

Memory Reference	Segment Register	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all prefetch instructions.
Stack	STACK (SS)	For all stack pushes and pops. Memory references are relative to BP base register except for data references.
Local Data	DATA (DS)	Data references when relative to stack, destination of string operation are explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

Table C-4. Segment and Resister

■ Minimum and maximum modes

The 80C88 has two system modes: the minimum and the maximum mode. With the maximum mode, a multi-CPU system can be organized with the 82C88 bus controller generating the bus control signals.

The minimum mode is appropriate for a simple system that generates its own bus control signals. MN/$\overline{MX}$ is the mode-select pin. The definitions of pins 24-31 and 34 depend on the MN/$\overline{MX}$ pin.

■ Bus operation

MSM80C88 has a time-multiplexed address and data bus. If a non-multiplexed bus is desired for the system, it is only necessary to add address latching.

The CPU bus cycle consists of at least four clock cycles, T1, T2, T3 and T4 (see Figure C-4).

Address output occurs during T1 and data transfer occurs during T3 and T4. T2 is used for changing the direction of the bus for a read operation. When the device that is accessed by the CPU is not ready to transfer data and sends to the CPU NOT READY, TW cycles are inserted between T3 and T4.

When the bus cycle is not needed, T1 cycles are inserted. In the T1 cycle, the ALE signal is output from the CPU or the 82C88, depending on MN/MX. At the trailing edge of this pulse, a valid address may be latched. Status bits $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ are used in the maximum mode by the bus controller to recognize the type of bus operation, based on the following table:

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTIC
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction fetch
1	0	1	Read data from memory
1	1	0	Write data to memory
1	1	1	Passive (no bus cycle)

Table C-5. S0, S1 and S2 Signals

Status bits S3 through S6 are multiplexed with A16-A19, and are therefore valid during T2 through T4. S3 and S4 indicate which segment register was selected in the bus cycle, according to the following table:

S4	S3	CHARACTERISTIC
0 (LOW)	0	Alternate data (Extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S5 indicates the interrupt enable flag.

Table C-6. S3 and S4 Signals

■ I/O addressing

MSM80C88 has 64K byte I/O. When the CPU accesses an I/O device, addresses A0-A15 are in the same format as a memory access and A16-A19 are LOW.
I/O port addresses are the same as the memory.

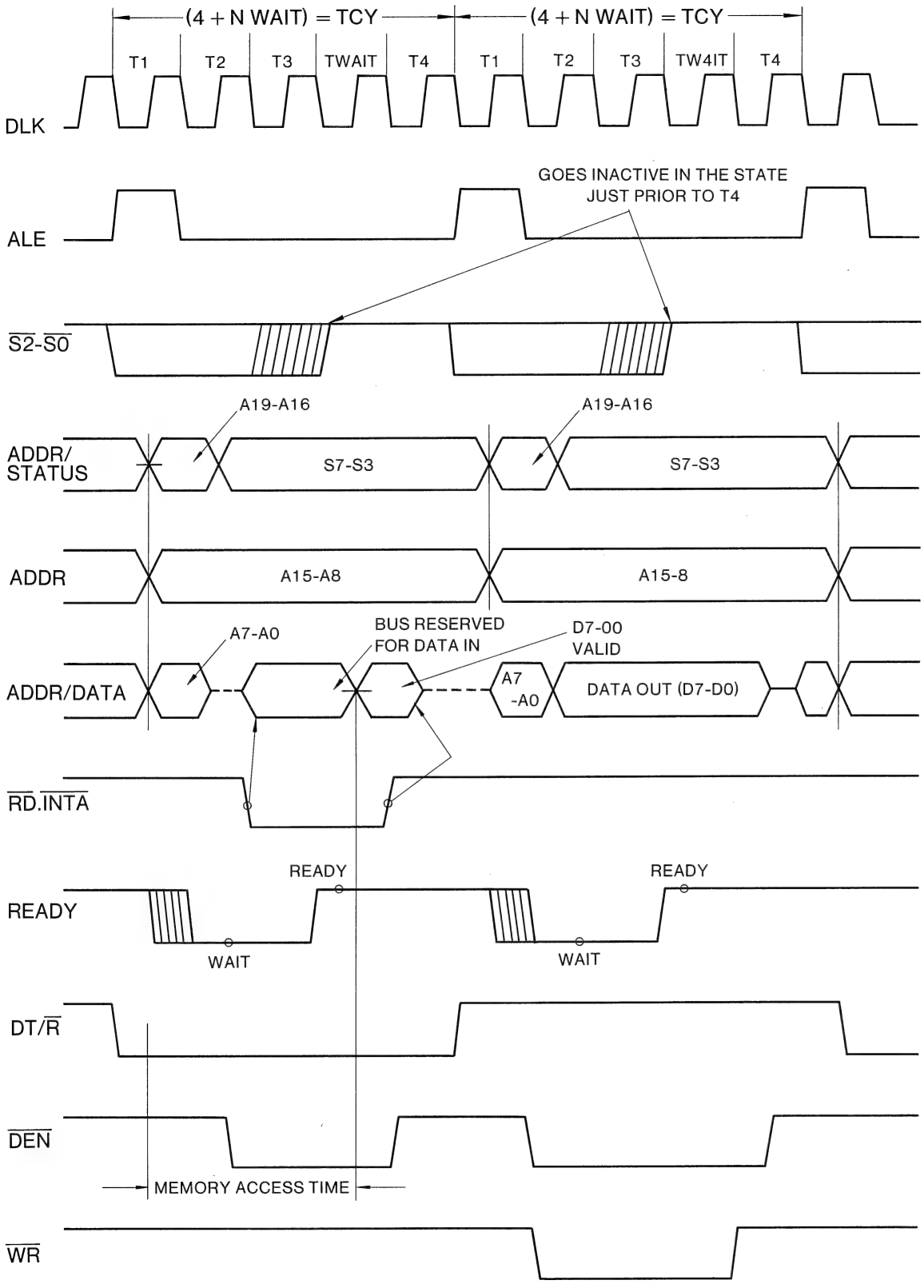


Figure C-4. Basic System Timing

External Interface

■ RESET

CPU initialization is executed by the RESET pin. In the 80C88, the RESET signal must be HIGH for more than four clock cycles. The rising edge terminates the present operation immediately; the falling edge triggers an internal reset sequence for approximately 10 clock cycles. Once the internal reset sequence is completed, normal operation begins from absolute location FFFF0H.

■ Interrupt Operations

An interrupt operation is classified as a software or a hardware interrupt. A hardware interrupt is further classified as maskable or nonmaskable.

An interrupt branches to a new program location, as defined in the interrupt pointer table on the basis of the type of interrupt. Absolute locations 00000H through 003FFH are reserved for the interrupt pointer table, which consists of 256 elements. Each element is four bytes in length and corresponds to an 8-bit number sent from the interrupt request device during the interrupt acknowledge cycle.

■ Nonmaskable Interrupt (NMI)

A nonmaskable interrupt (NMI) is of higher priority than a maskable interrupt request (INTR). An NMI request pulse width requires a minimum of two clock cycles. NMI is serviced at the end of the current instruction or between string manipulations.

■ Maskable Interrupt (INTR)

A maskable interrupt request (INTR) can be masked by software. INTR is triggered by the signal level, so it must be held until the interrupt request is acknowledged.

INTR is serviced at the end of the current instruction or between string manipulations.

■ Interrupt Acknowledge

During an interrupt-acknowledge sequence, further interrupts are disabled. The interrupt enable bit is reset by any interrupt after the flag register has been automatically pushed onto the stack. During an acknowledge sequence, the CPU issues a lock signal from T2 of the first bus cycle to T2 of the second bus cycle. In the second bus cycle, a byte is fetched from the external device as a vector for identifying the type of interrupt. This vector is multiplied by four which produces the interrupt pointer address (INTR only).

The interrupt return (IRET) instruction includes a flag pop operation that restores the original interrupt enable bit at the same time that it restores the flag.

■ Halt

When a halt instruction is executed, the CPU enters halt status. An interrupt request or RESET will force the 80C88 out of halt status.

■ **System Timing–Minimum Mode**

The T1 bus cycle begins with the ALE signal. The trailing edge of ALE is used to latch the address. From T1 to T4, the IO/M signal indicates a memory or I/O operation. From T2 to T4, the address data bus changes the address bus to a data bus.

The read ($\overline{RD}$), write ($\overline{WR}$) and interrupt acknowledge ($\overline{INTA}$) signals cause the addressed device to enable the data bus. These signals become active at the beginning of T2 and inactive at the beginning of T4.

■ **System Timing–Maximum Mode**

For the maximum mode, the 82C88 bus controller is incorporated into the system. The CPU sends status information to the bus controller, which generates bus timing signals. The bus timing is virtually the same as in the minimum mode.

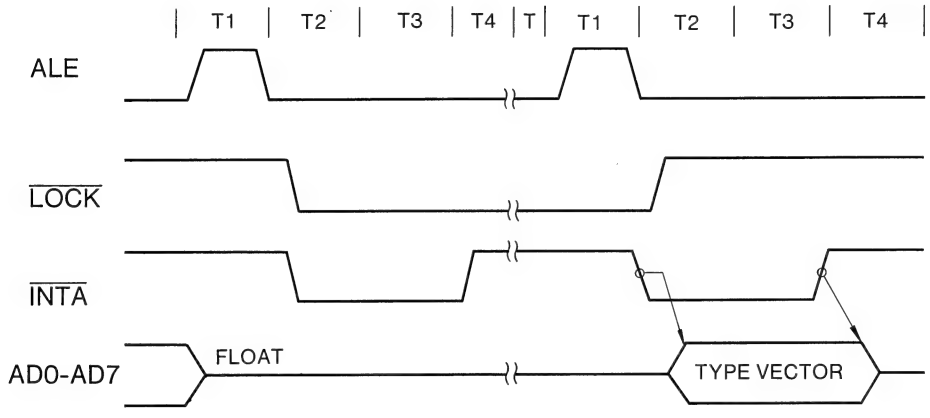


Figure C-5. Interrupt Acknowledge Sequence

C.2 MSM82C84ARS

(1) Overview

The 8086 clock generator supplies the clock signal to the 8086 and peripheral circuits, and synchronizes the READY signal from the peripheral circuits.

(2) Terminal Connection and Circuit Configuration

(Top View) 40 Lead Plastic DIP

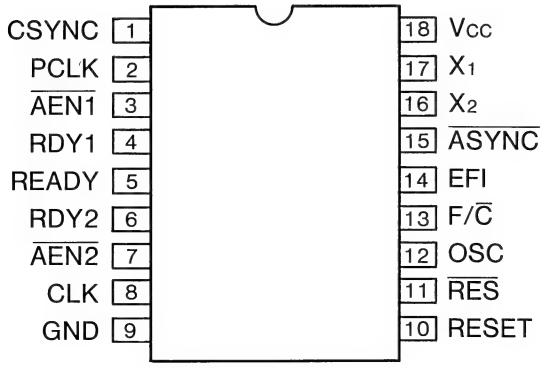


Figure C-6. MSM82C84ARS Terminal Connection

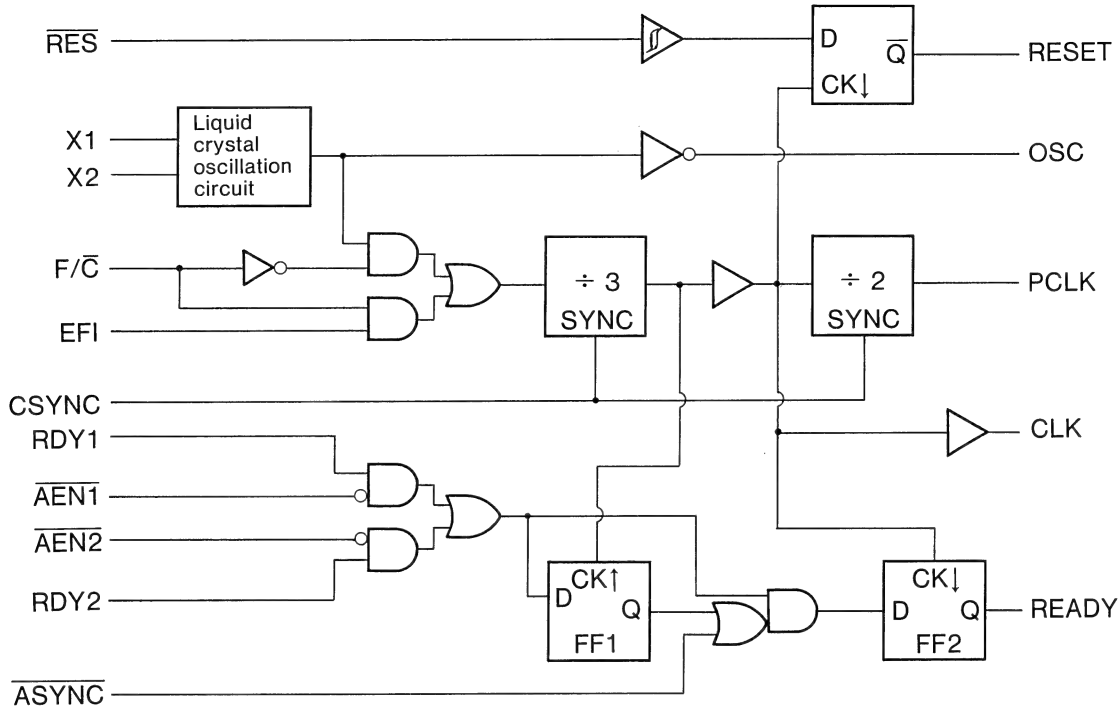


Figure C-7. MSM82C84ARS Circuit Configuration

(3) Terminal Description

Terminal name	Function
CSYNC	A synchronization signal used when outputting clocks with the same phase using two or more MSM82C84As. When this signal level is high, the internal counter is reset and the CLK level will be high. The internal counter starts its operation and a 1/3 duty CLK is output when the signal level is set to low.
PCLK	A clock signal used by the peripheral circuits. This clock is output with a 50% duty cycle and its frequency is one-half that of the CLK signal.
$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$	$\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$ are signals used to enable RDY1 and RDY2, respectively.
RDY1, RDY2	A RDY1 or RDY2 level set to high indicates that the connection to the system data bus has completed the data reception or is ready for data transmission. RDY is valid only when its corresponding $\overline{\text{AEN}}$ is enabled.
READY	This signal is the product of synchronizing the bus READY signal with the CLK signal. The READY status is represented by a high level with the same phase as the RDY input. Issuance of this signal guarantees the MSM80C86/80C88 CPU that the hold time will be maintained.

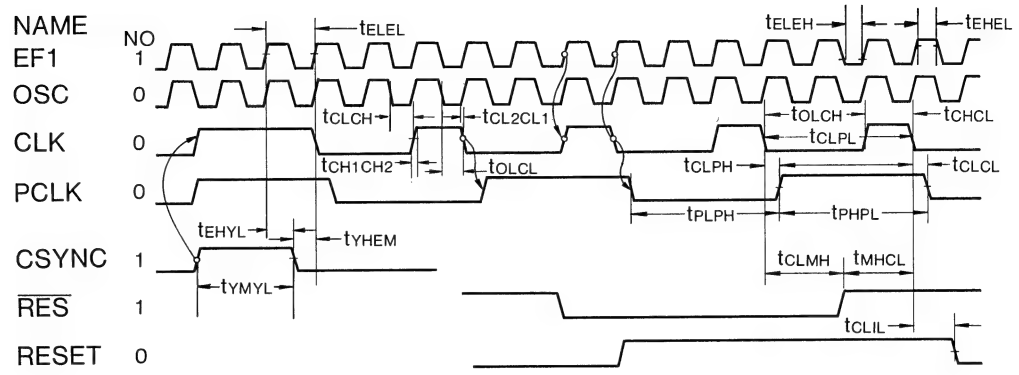
Terminal name	Function
CLK	This is a clock signal used by the CPU and the peripheral devices connected to the CPU local bus. The frequency of the output waveform will either be one-third of the oscillation frequency of the quartz oscillator connected to X1 or X2, or one-third of the EFI input frequency. The waveform will have a one-third duty cycle.
$\overline{\text{RES}}$	An input whose low level is used by the CPU to generate a reset signal. Since a Schmitt trigger circuit is used for this signal's input circuit, power on and reset can be performed by connecting a simple RC circuit.
RESET	A signal that is produced by synchronizing the signal that is input to $\overline{\text{RES}}$ with the CLK signal. This signal is output with the high level being active. This signal is used by the CPU as a system reset signal.
F/$\overline{\text{C}}$	This signal is used in selecting the basic signal to be used for producing the CLK signal. When a low level is selected, the CLK signal will use the output of the quartz oscillator circuit as the basic signal. When a high level is selected, the CLK signal will use the input signal to EFI as the basic signal.
EFI	When the F/$\overline{\text{C}}$ level is high, the CLK signal is generated using the signal that is input to this terminal. The frequency of the signal that is input is three times that of the required frequency of the CLK signal.
X1, X2	Quartz to be used as the quartz oscillator is connected here. The frequency of the quartz must be three times that of the required frequency of the CLK signal.
OSC	This is the output of the quartz oscillator, and the frequency of the output will be the same as the oscillation frequency of the quartz that is connected to X1 and X2. Even if the F/$\overline{\text{C}}$ level is high (for using the EFI input for generating the CLK signal), the quartz oscillation signal can be received from this terminal as long as a quartz is connected to X1 and X2.
$\overline{\text{ASYNC}}$	A signal used to select the synchronization mode for the READY signal generation circuit. If this signal level is low, the READY signal will be generated using two synchronization steps. If the level is high, the READY signal will be generated using one synchronization step. If this signal is open, the signal must be processed by an external device since the Tandy 600 is not equipped with built-in pull-up resistance.
Vcc	5V power supply
GND	GND

(4) Operation Description

[Omitted.]

(5) Timing Chart

(a) RESET and various clock signals



Note: All timing measurements are made at 1.5 volts, unless otherwise noted.

Figure C-8. MSM82C84ARS CLOCK and RESET Signals Timing Chart

(b) READY signal (when ASYNC level is low)

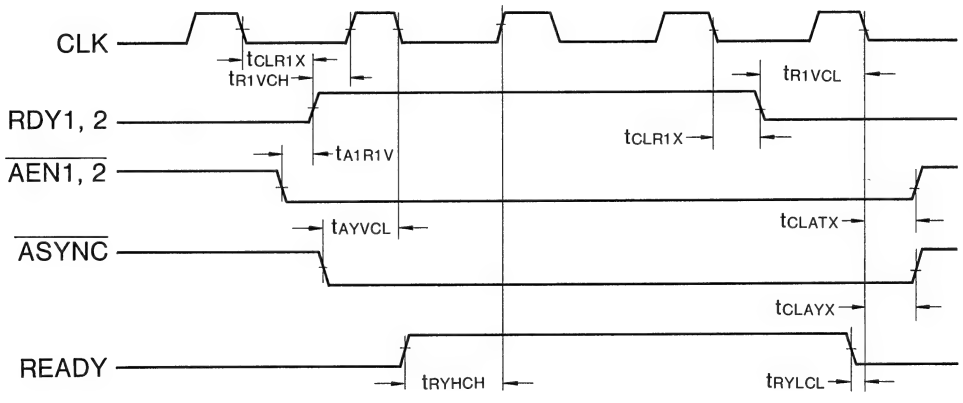


Figure C-9. MSM82C84ARS READY Signals Timing Chart

C.3 MSM81C55RS (PIO)

(1) Overview

The MSM8155RS/8156RS is a combination RAM and I/O device used by the microcomputer system. The RAM is a 2-Kbit static RAM with a 256-word by 8-bit configuration. The I/O is accomplished by two 8-bit ports and one 6-bit, general-purpose I/O port. If programming is performed using this general-purpose port (port C), two other ports (port A and port B) can be used in the handshake mode, etc. The MSM8155RS/8156RS is equipped with a built-in 14-bit programmable counter/timer that is used for counting the terminal counter pulse.

(2) Terminal Connection and Circuit Configuration

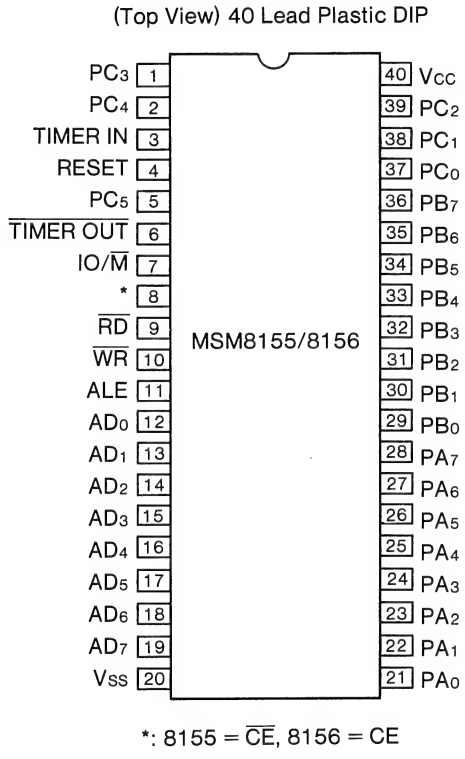


Figure C-10. MSM81C55RS Terminal Connection

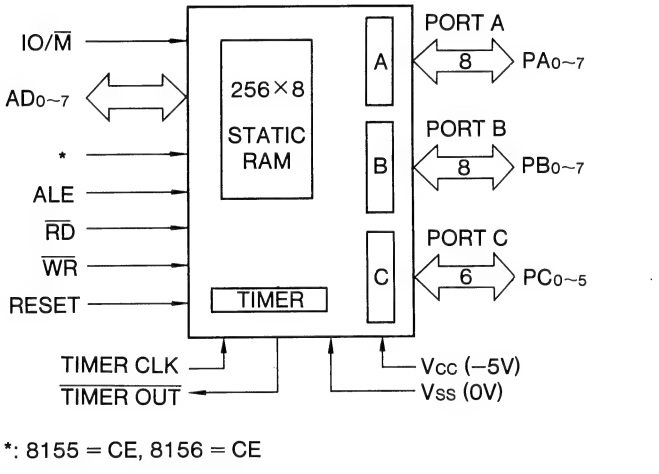


Figure C-11. MSM81C55 Circuit Configuration

(3) Terminal Description

Terminal name	Function
RESET	The signal that is fed from the 8085A. When the signal level is high, the system is reset and the three I/O ports are set to the input mode.
ALE	The falling edge of ALE (address latch enable) is used by the corresponding latch circuits as the timing for fetching AD_{0-7}, IO/M and CE (or $\overline{CE}$) signals.
AD_{0-7}	A bidirectional address/data bus with three states. An 8-bit address information is fetched by the latch circuit using the falling edge of ALE as the fetch timing. Depending on the status of the $\overline{WRITE}$ or $\overline{READ}$ input signal, it is possible to read an 8-bit data from or write an 8-bit data into a chip.
$\overline{CE}$, CE	Reading and writing are not performed when the $\overline{CE}$ level is high or the CE level is low.
IO/$\overline{M}$	I/O is selected when the level is high, and memory is selected when the level is low.
$\overline{RD}$	If the level is low, the memory information is written into AD_{0-7} when in the memory cycle, and the selected port information is written into AD_{0-7} when in the IO cycle.
$\overline{WR}$	If the level is low, the information in AD_{0-7} is written into the memory when in the RAM cycle, and the information in AD_{0-7} is written into the selected port when in the IO cycle.
$PA_{0\sim7}$ ($PE_{0\sim7}$)	General-purpose I/O terminals. The I/O direction is selected by programming the command/status register (C/S register).
$PC_{0\sim7}$	The terminals are used either as general-purpose I/O terminals or as control terminals for the PA or PB port. The following usages are possible when used as control terminals: PC_0: A INTR (port A interrupt) PC_1: A BF (port A buffer full) PC_2: $\overline{A\ STB}$ (port A strobe) PC_3: B INTR (port B interrupt) PC_4: B BF (port B buffer full) PC_5: $\overline{B\ STB}$ (port B strobe)
TIMER IN	Input signal for counter/timer.
$\overline{TIMER\ OUT}$	Timer output. A square wave pulse is issued in accordance with the control signal specification when the total count reaches a specified value.
V_{CC}	−5V power supply
V_{SS}	GND

(4) Operation Description

[Omitted.]

(5) Timing Chart

(a) Read cycle

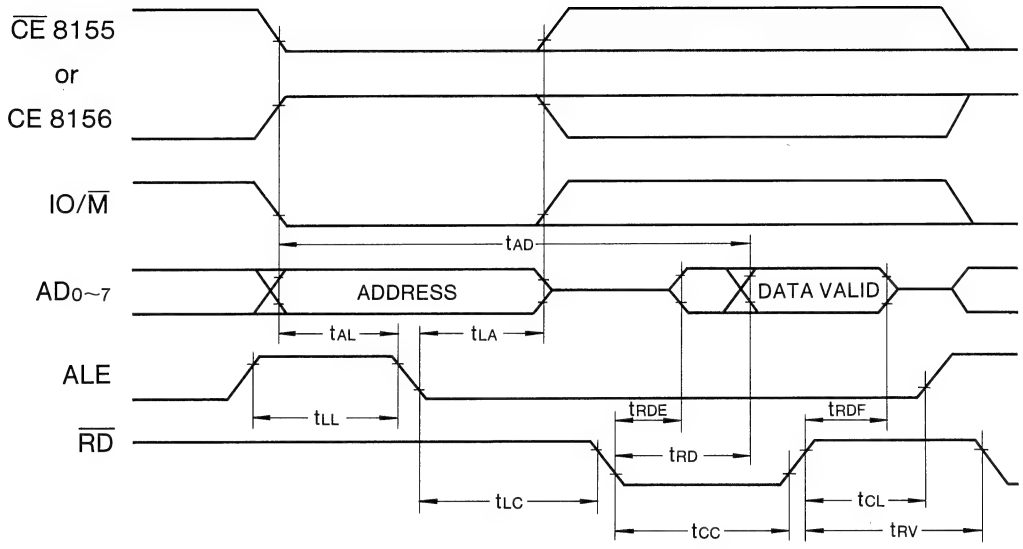


Figure C-12. MSM81C55 Read Cycle Timing Chart

(b) Write cycle

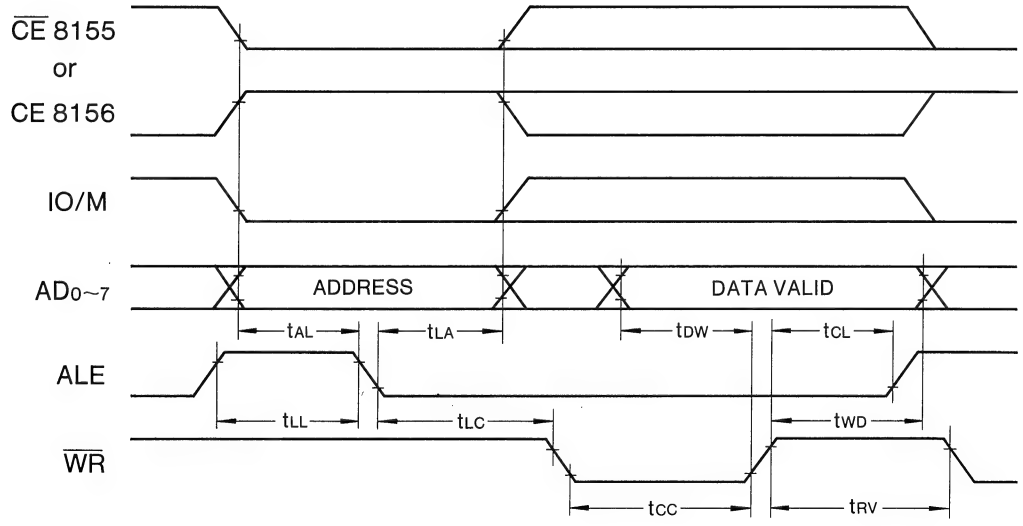


Figure C-13. MSM81C55 Write Cycle Timing Chart

(c) Strobed input mode

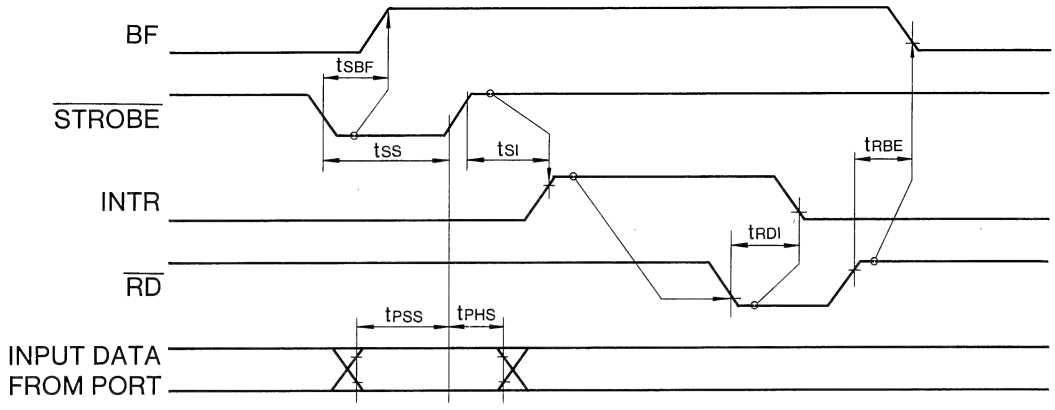


Figure C-14. MSM81C55 Strobed Input Mode Timing Chart

(d) Strobed output mode

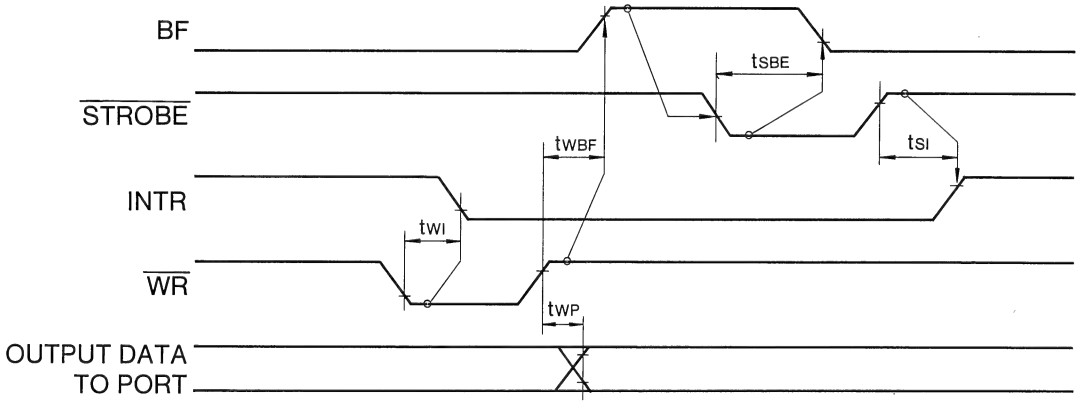


Figure C-15. MSM81C55 Strobed Output Mode Timing Chart

(e) Basic input mode

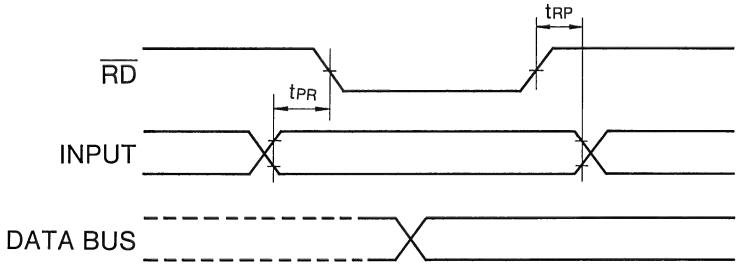


Figure C-16. MSM81C55 Basic Input Mode Timing Chart

(f) Basic output mode

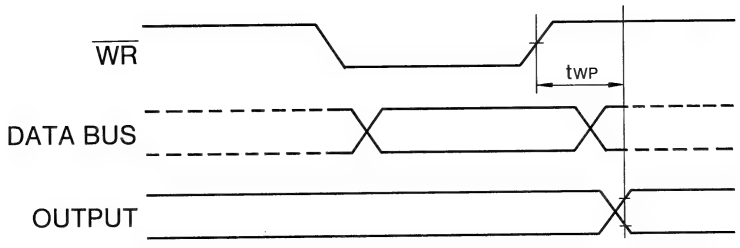
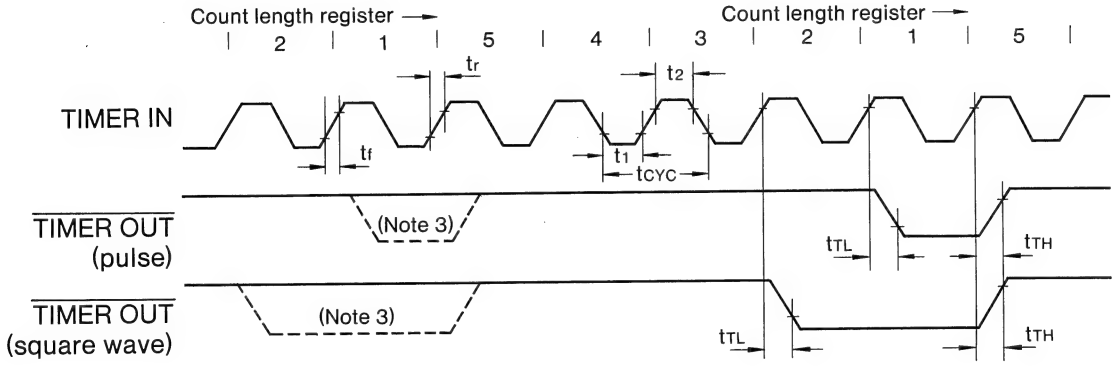


Figure C-17. MSM81C55 Basic Output Mode Timing Chart

* The data bus timing is the same as that for the read cycle and the write cycle.

(g) Timer waveform



Note: Output periodically depending on the contents of the output mode (M = 1) program.

Figure C-18. MSM81C55 Timer Timing Chart

C.4 HD146818 (Real-Time Clock Plus RAM)

(1) Overview

The HD146818 RTC is a peripheral LSI for use with the HMCS6800 microprocessor. It is equipped with a clock and a calendar function for keeping track of the year, month, day, day of week, time, etc.

The HD146818 RTC is equipped with a 50-byte user RAM area and timer functions that enable it to generate square waves and periodic interrupts.

(2) Terminal Connection Diagram and Circuit Configuration

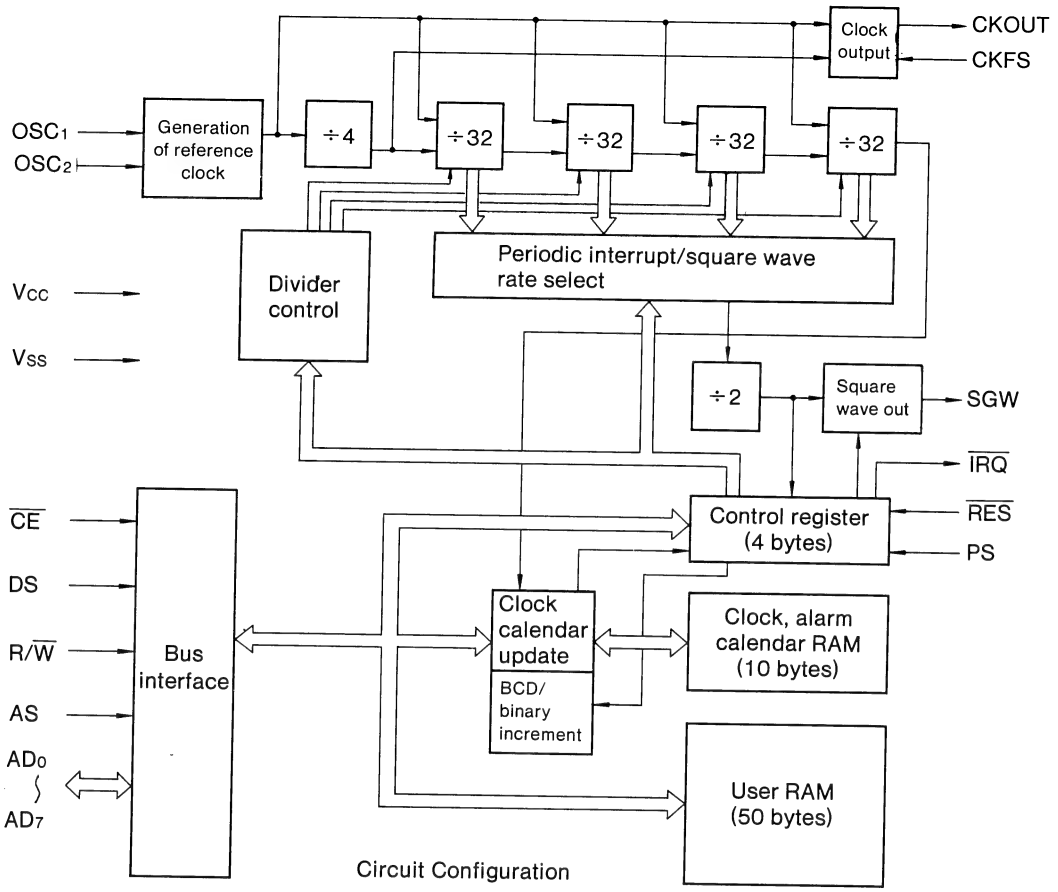


Figure C-19. HD146818 Circuit Configuration

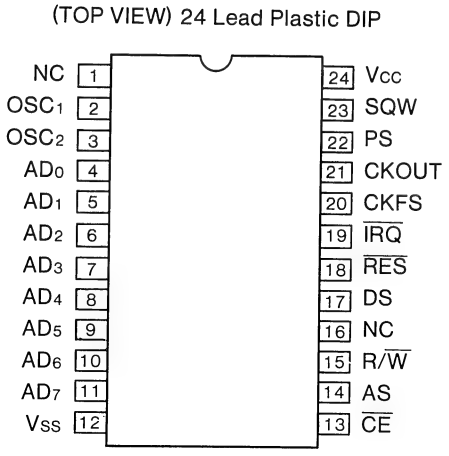


Figure C-20. HD146818 Terminal Connection Diagram

(3) Terminal Description

Terminal symbol	Function
V_{CC}, V_{SS}	V_{CC} is the positive power supply voltage; V_{SS} is the ground.
OSC1, OSC2 (Reference clock)	Input terminal for connecting a quartz oscillator or an external reference clock.
CKOUT (Clock out)	Clock with the same or 1/4 frequency of the reference clock is issued from this terminal. The frequency ratio is specified by CKFS.
CKFS (Clock out Frequency Select)	Connect this terminal to V_{CC} to direct to CKOUT a clock with the same frequency as that output from the OSC1 pin; connect this terminal to V_{SS} to direct to CKOUT a clock with a 1/4 frequency.
SQW (Square Wave)	Square waves generated in the internal divider circuit are output from this terminal. Bits RS0-RS3 of control register A select a 15-step output from the 22-step divider circuit, and direct the output to this terminal. The SQW output is enabled by setting the SQWE bit in control register B to 1. The output from this terminal will have a low level if the SQWE bit is set to 0.
AD_0-AD_7 (Multiplexed Address/Data Bus)	AD_0 through AD_7 are bidirectional buses used for data I/O and for transferring address information used by the processor for accessing RTC. The first half of the cycle is used for transferring the address information, and the last half is used for data transfer. Address information that is to be transferred must be established before the arrival of the falling edge of the AS signal. The three-state output buffer is used as the data bus driver. Unless data is being output by RTC, the impedance will be high.
AS (Multiplexed Address Strobe)	A strobe signal used for fetching the address information from the multiplexed address bus. The falling edge of this signal is used as the RTC address information fetch timing.
DS (Data Strobe)	An input terminal for the HMCS6800 system $\phi 2$ clock (E: enable) signal. Data to be read by the processor from RTC is output while the signal level is high. Data is written by the processor when the signal level falls. With the 8085 series, the terminal is used as the input terminal for the RD signal.
R/$\overline{W}$ (Read/Write)	An input terminal for the HMCS6800 system R/$\overline{W}$ signal. The signal level is set to high for the processor to read RTC. The signal level is set to low for the processor to write data in RTC. With the 8085 series, the terminal is used as an input terminal for the $\overline{WR}$ signal.
$\overline{CE}$ (Chip Enable)	An input terminal for setting the level to low for accessing this LSI. With this signal, the level must be set for one cycle. RTC is not accessed when this signal level is high.

Terminal symbol	Function
$\overline{\text{IRQ}}$ (Interrupt Request)	An active low-level signal for requesting an interrupt to the processor. The signal level becomes low and stays low if the interrupt enable bit is set and if an interrupt cause is set in the status bit. Normally, the processor reads control register C to release this signal. When the $\overline{\text{RES}}$ signal level is low, all pending interrupt causes are cleared, and this signal is released. If there is no interrupt request, this terminal will have a high impedance. This terminal can be connected to other $\overline{\text{IRQ}}$ signals by connecting a pull-up resistance.
$\overline{\text{RES}}$ (Reset)	An input signal that resets RTC. Reading from and writing into the internal registers and RAM are disabled when this signal level is low. Instead, the following operations are performed: (1) The periodic interrupt enable bit (PIE) is cleared to 0. (2) The alarm interrupt enable bit (AIE) is cleared to 0. (3) The update ended interrupt enable bit (UIE) is cleared to 0. (4) The interrupt request status flag is cleared to 0. (5) The periodic interrupt flag (PF) is cleared to 0. (6) The alarm interrupt flag (AF) is cleared to 0. (7) The update ended interrupt flag (UF) is cleared to 0. (8) The $\overline{\text{IRQ}}$ terminal will be in a high impedance state. (9) The square wave output enable bit (SQWE) is cleared to 0. The $\overline{\text{RES}}$ signal has no effect on the clock calendar or RAM functions.
PS (Power Sense)	The PS input signal is used along with the valid RAM and times (VRT) bit of control register D. When this signal level is low, the VRT bit is cleared to 0. Signal from the external power sense circuit is entered from this terminal.

C.5 MSM825C51ARS

(1) Overview

The MSM82C51ARS is a CMOS-type USART (universal synchronous/asynchronous receiver/transmitter) for data communication use.

(2) Terminal Connection and Circuit Configuration

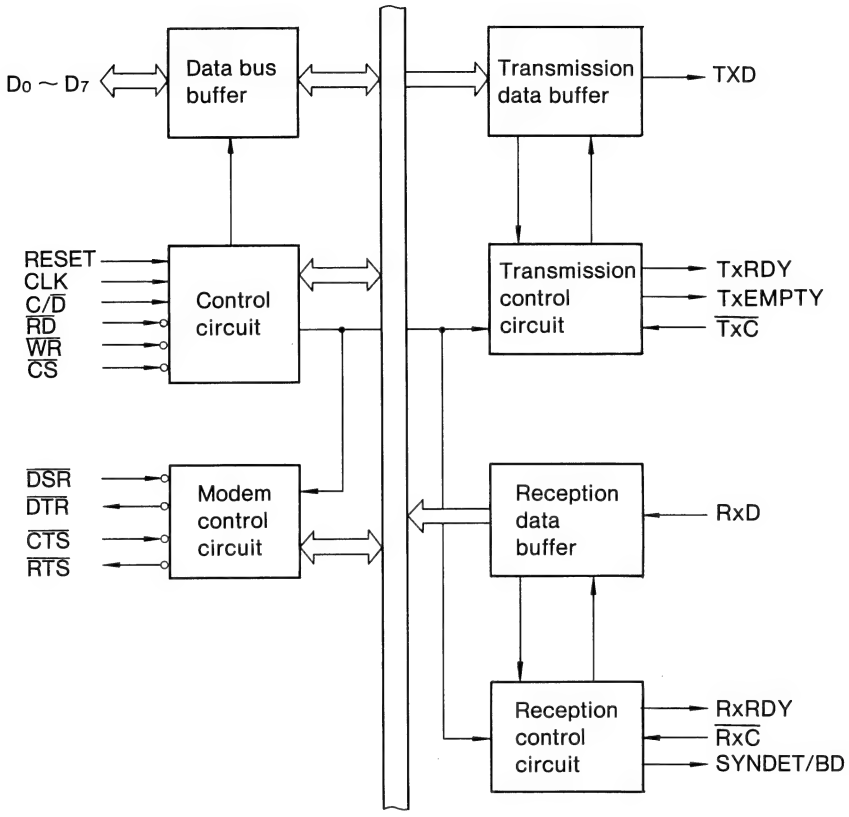


Figure C-21. MSM82C51ARS Circuit Configuration

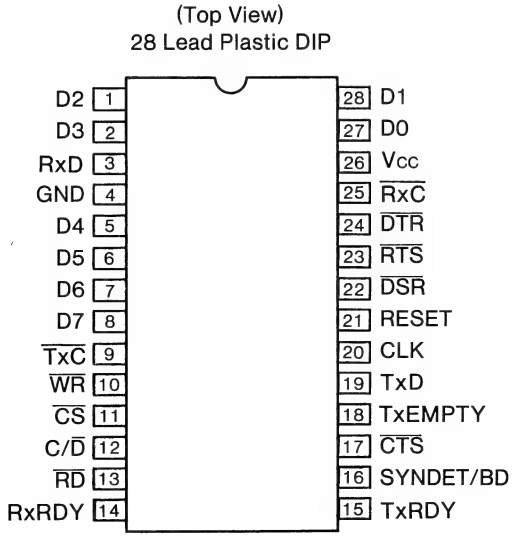


Figure C-22. MSM82C51ARS Terminal Connection

(3) Terminal Description

Terminal symbol	Function
D_0-D_7	A bidirectional data bus used for CPU I/O of data, commands, status, etc.
RESET	An active high terminal that resets 82C51A.
CLK	An input terminal for the 82C51 master clock.
$\overline{WR}$	A signal terminal for writing data or command.
$\overline{RD}$	A signal terminal for reading data or status.
C/$\overline{D}$	A signal terminal used in specifying whether the content of the data bus is data, command or status during read or write.
$\overline{CS}$	A terminal used for selecting 82C51A.
TxD	A transmission data output terminal.
TxRDY	A terminal that indicates that transmission data can be received from the CPU.
$\overline{TxE}$	A terminal that indicates the absence of data to be sent by 82C51A.
TxC	A transmission clock input terminal.
RxD	A reception data input terminal.
RxRDY	A terminal that indicates the presence of reception completed data in 82C51A.
$\overline{RxC}$	A reception clock input terminal.
SYNDET/BD	An input terminal for external synchronization detection, if in the external synchronization mode. An output terminal indicating synchronization detection, if in the internal synchronization mode. An output terminal for indicating break status detection, if in the asynchronous mode.
$\overline{DSR}$	An input port for modem interface.
$\overline{DTR}$	An output port for modem interface.
$\overline{CTS}$	An input terminal for modem interface used for controlling transmission.
$\overline{RTS}$	An output port for modem interface.
V_{CC}	V_{CC} power supply terminal.
GND	GND power supply terminal.

(4) Operation Description

[Omitted.]

(a) Write Cycle (CPU-USART)

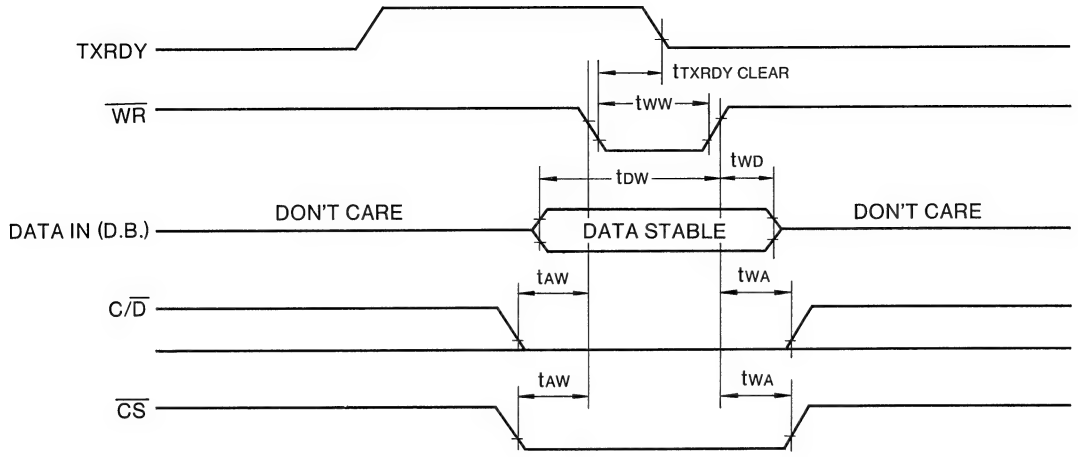


Figure C-23. MSM82C51ARS Write Data Cycle Timing Chart

(b) Read Cycle (CPU-USART)

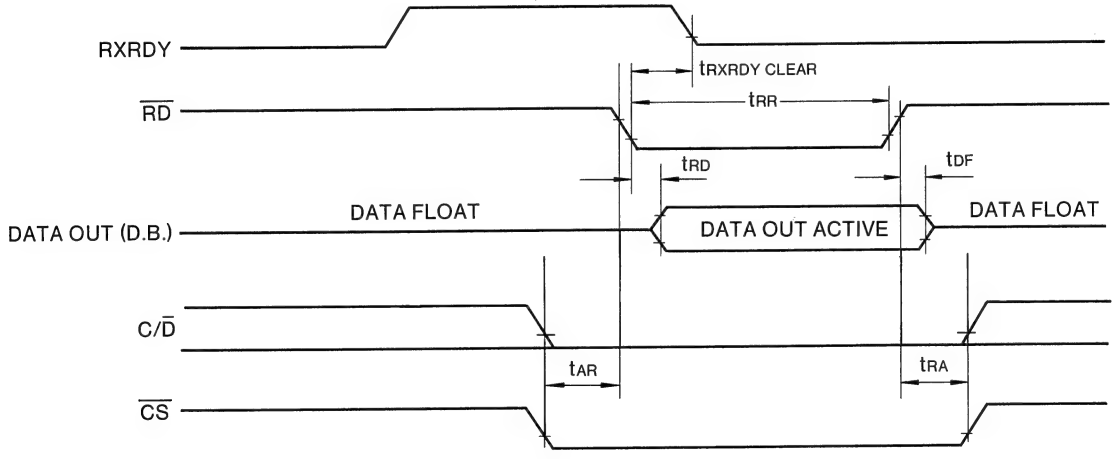
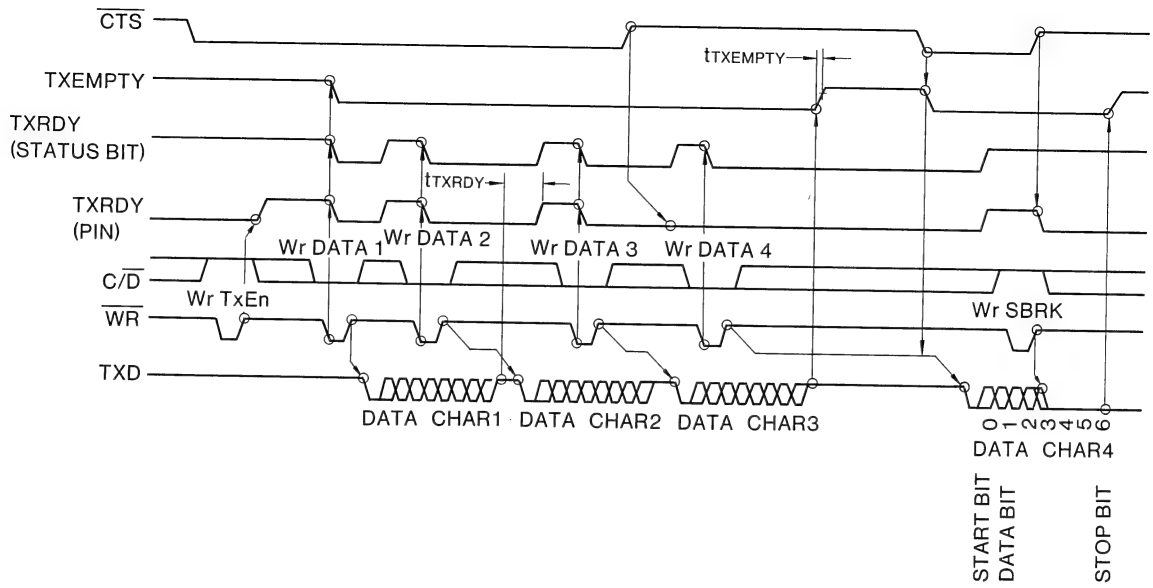


Figure C-24. MSM82C51ARS Read Data Cycle Timing Chart

(c) Transmitter Control and Flag Timing (ASYNC MODE)



Note: The waveform diagram applies to the case of a length of 7 data bits + parity bit + 2 stop bits.

Figure C-25. MSM82C51ARS Transmitter Control and Flag Timing Chart (ASYNC MODE)

(5) Timing Chart

(a) Transmitter Clock and Data

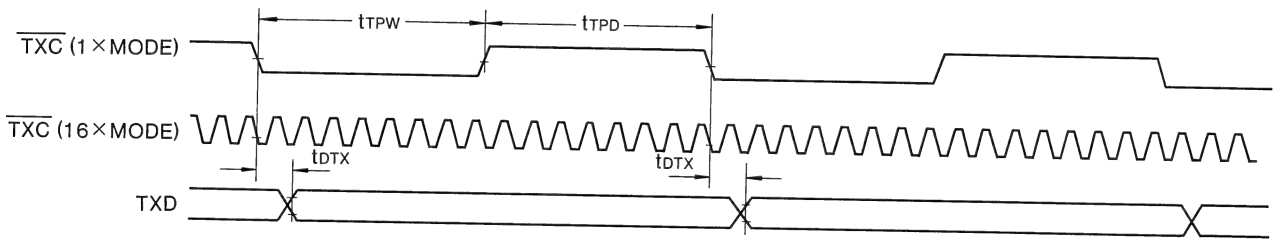


Figure C-26. MSM82C51ARS Transmitter Clock and Data Timing Chart

(b) Receiver Clock and Data

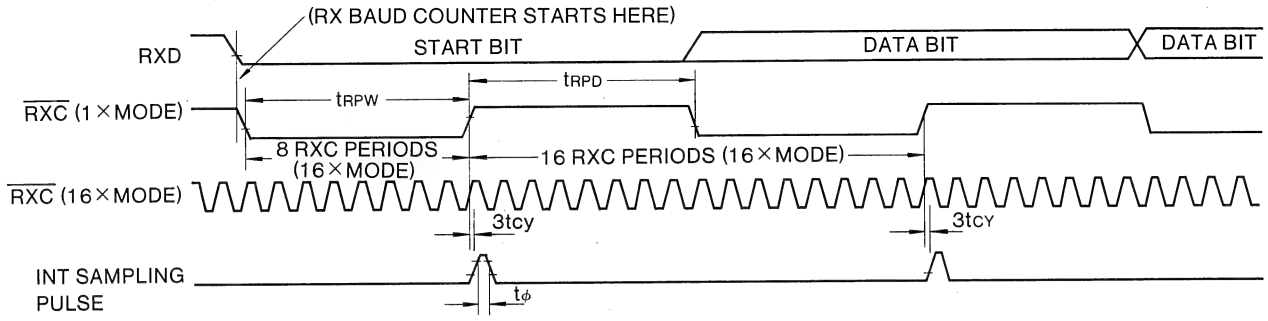
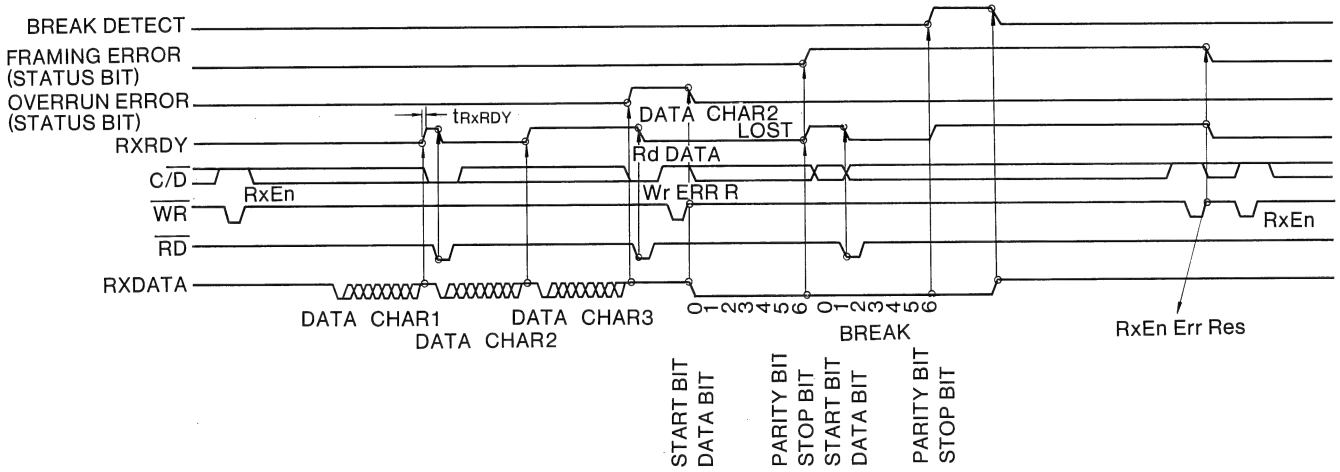


Figure C-27. MSM82C51ARS Receiver Clock and Data Timing Chart

(c) Receiver Control and Flag Timing (ASYNC MODE)



Note: The waveform diagram applies to the case of a length of 7 data bits + parity bit + 2 stop bits.

Figure C-28. MSM82C51ARS Receiver Control and Flag Timing Chart

(d) Write Control or Output Port Cycle (CPU→USART)

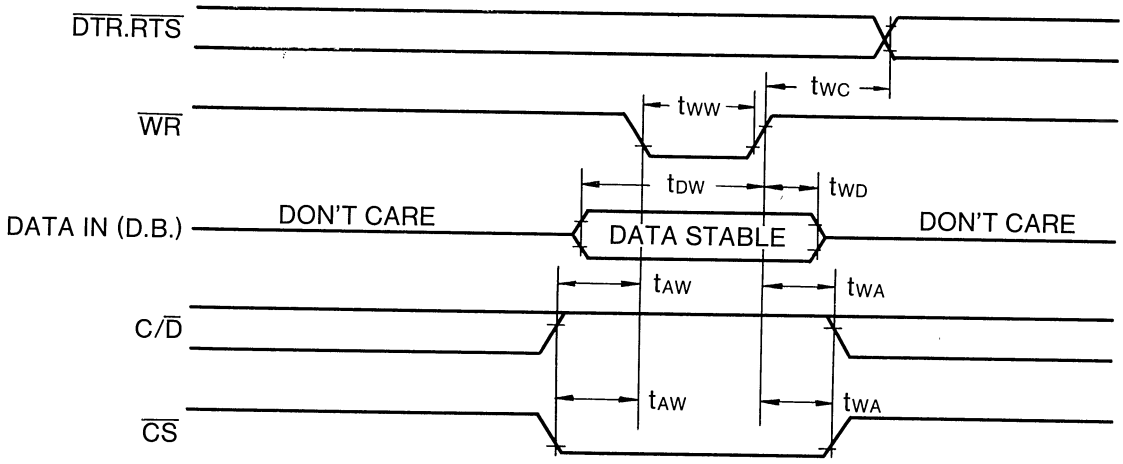


Figure C-29. MSM82C51ARS Write Control or Output Port Timing Chart

(e) Read Control or Input Port (CPU→USART)

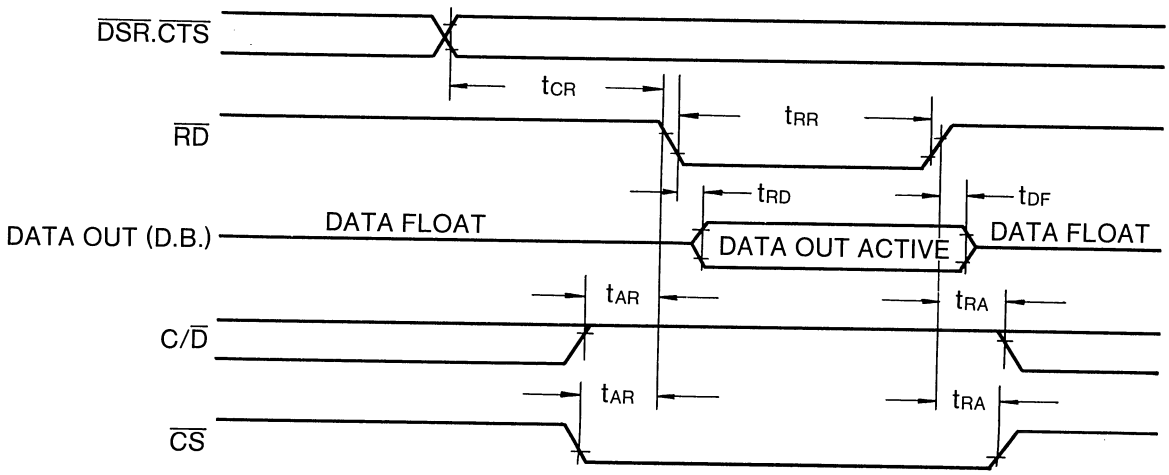


Figure C-30. MSM82C51ARS Read Control or Input Port Timing Chart

C.6 MSM6946RS

(1) Overview

The MSM694RS is a 300-BPS FSK modem.

(2) Terminal Connection and Circuit Configuration

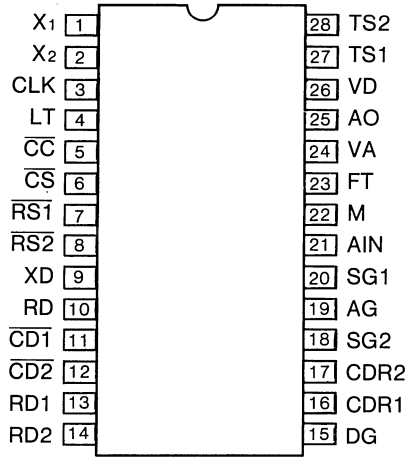


Figure C-31. MSM6946RS Terminal Connection

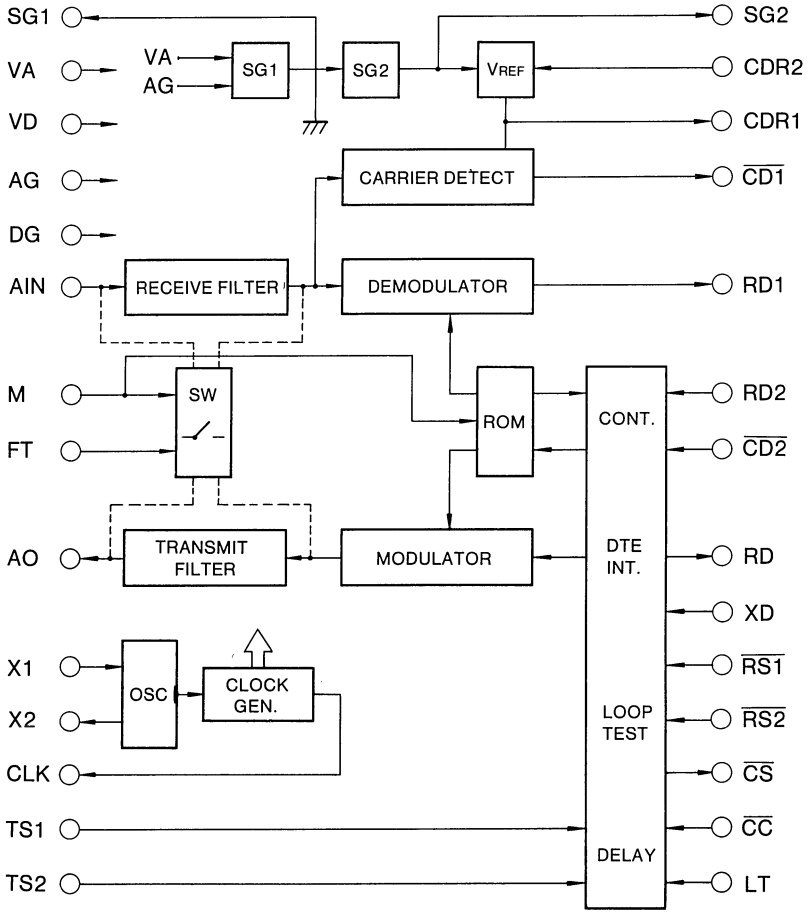


Figure C-32. MSM6946RS Circuit Configuration

(3) Terminal Description

Terminal symbol	Function
X1	X1 and X2 are connected to crystal oscillators with a resonance frequency of 3.57954 MHz. The clock necessary for the IC operation is output from this terminal. X1 is used as an input terminal when an external clock is used.
X2	See the above description for X1. This terminal is opened when an external clock is used.
CLK	Output terminal for an 873.9 Hz clock. This terminal is mainly used when an external timer is used.
LT	A control input terminal used for performing a loop test. When a digital 1 is entered, the data that is entered to XD and $\overline{RS1}$ is output to RD and $\overline{CS}$, respectively. At this time, the demodulated data of the AIN reception carrier signal is not output to RD but is used as the input data for the modulator. A modulation carrier signal is generated in accordance with the operation mode specified for the modulator. Whether or not the modulation carrier signal that is output to AO is controlled by $\overline{CC}$, and not by $\overline{RS1}$. Enter a digital 0 to LT for a normal operation.
$\overline{CC}$	Controls whether or not a modulation carrier signal will be output to AO during loop test (LT = digital 1). A modulation carrier signal is output to AO if a digital 0 is entered, and the signal is not output if a digital 1 is entered. This terminal has no effect on the operation if a digital 0 is entered to LT.
$\overline{CS}$	A clear to send output terminal that indicates whether or not the modulator is in a data transmittable status. A digital output of 1 indicates that the modulator is not in a data transmittable status (OFF). A digital output of 0 indicates that the modulator is in a data transmittable status (ON). A digital 0 is output from this terminal after the elapse of the RS/$\overline{CS}$ delay time subsequent to the input of a digital 0 to the $\overline{RS1}$ terminal. A digital 1 is output from the $\overline{CS}$ terminal when a digital 1 is entered to the $\overline{RS1}$ terminal, without any delay.
$\overline{RS1}$	A request to send input terminal. A digital 0 is entered to set the modulator to data transmission status (ON). A digital 1 is entered to disable (OFF) the modulator from data transmission. A digital 0 must be maintained while data transmission is in progress.
$\overline{RS2}$	The output of an external delay timer, if used, is input to $\overline{RS2}$. Fix the input to a digital 0 or 1 if the built-in delay timer is used.
XD	A transmission data that is FSK modulated and sent to the line via AO. A digital 1 specifies a mark side frequency signal, and a digital 0 specifies a space side frequency signal. Signal reaches AO when digital 0 is entered to $\overline{RS1}$.

Terminal symbol	Function
RD	A reception data. FSK modulated signal that is received by AIN is demodulated and is output as a serial data. A digital 1 indicates mark, and a digital 0 indicates a space. If the carrier detector output (CD2) is a digital 1 (that is, OFF), a mark status (digital 1) is maintained.
$\overline{\text{CD1}}$	The carrier detection circuit is connected to the built-in delay timer with an internal connection. $\overline{\text{CD1}}$ outputs the carrier detection signal prior to it passing through the delay timer. When an external delay timer is used, the input for the timer is connected to $\overline{\text{CD1}}$, and the output from the timer is connected to $\overline{\text{CD2}}$ (I/O terminal). When this is done, $\overline{\text{CD2}}$ functions as an input terminal.
$\overline{\text{CD2}}$	An output data from the carrier detector. CD2 is used as an input terminal for connecting the output of an external delay timer, if one is used. Whether or not an external delay timer is used, the $\overline{\text{CD2}}$ status indicates the status of the carrier detector. A digital 0 indicates the presence of a carrier, while a digital 1 indicates the absence of a carrier.
RD1	RD1 is an output from the modulator. The output is normally entered directly to RD2 in the logical interface circuit where it is controlled and subsequently output to RD. When an output data from the modulator that has been controlled by NCU (network-control unit) is necessary as the RD2 signal, RD1 and RD2 are connected through an external gate circuit.
RD2	See the description for RD1.
DG	A ground for the digital circuit power supply (VD). Shares DG with AG at a point sufficiently close to the system ground.
CDR1	A reference voltage output for the carrier detection circuit. The carrier detection level is set using an external resistance. An approximate +3V with respect to SG2 is used as the reference voltage.
CDR2	An inverse input terminal for the built-in operational amplifier used in setting the carrier detection level. Normally, two external resistances are connected. A suitable carrier detection level is set by adjusting the ratio between the two resistances. The implication is that the reception signal level loss caused by the line transformer can be compensated for. Select the two resistances so that the sum of the resistances is at least 50k ohms.
SG2	A built-in signal ground used only by the carrier detection circuit. To keep the impedance low so that high performance can be obtained, it is better to bypass to AG, at a point close to the device, using a capacitor with a capacitance of at least 0.01 microfarads.
AG	A ground for the analog circuit power supply (VA). Shares the ground with DG at a position close to the system ground.

Terminal symbol	Function
SG1	A built-in signal ground used as a ground for all analog circuits other than the carrier detection circuit. To reduce the impedance so as to assure high performance, it is better to bypass to AG, at a position close to the device, using a capacitor with a capacitance of at least 1 microfarad.
AIN	A reception signal input terminal for the Tandy 600. A modem will fetch only the digital information from the AIN FSK modulated signal, and output the information as a serial data to RD.
M	An input for specifying the selection between originate mode and answer mode. The originate mode (transmission carrier frequency less than the reception carrier frequency) is selected if it is a digital 1, and the answer mode (transmission carrier frequency higher than the reception carrier frequency) is selected if it is a digital 0. When used with FT, this terminal can be used for testing the transmission and reception filters.
FT	An input terminal used for device testing. When a digital 1 is entered, AO is disconnected from the transmission filter output and is connected to the reception filter output. To use this terminal, connect the terminal to a digital 0.
VA	A power supply for the analog circuits. The recommended voltage is +12V. To eliminate noise, bypass to AG using a capacitor with a capacitance of approximately 10 microfarads.
AO	A transmission signal output terminal for the Tandy 600. The transmission binary information entered to XD is FSK modulated by the modem, and is transmitted to the line from AO. The DC potential is approximately one half that of VA. Set the load resistance to at least 50k ohms. Since the transmission signal level will change mainly with VA, it is necessary to adjust the level using two resistances.
VD	A power supply for the digital circuits whose recommended voltage is +5V. To reduce noise, bypass to DG using a capacitor with a capacitance of approximately 10 microfarads.
TS1	TS1 and TS2 are input terminals used for selecting the value for the built-in delay timer. By entering a digital 1 to both terminals, an external delay timer may be connected. If this is done, however, all delay timers must be external. When this mode is selected, $\overline{CD2}$ will function as an input terminal. The built-in delay timer is used for RS/ON→CS/ON, CD/ON and CD/OFF.
TS2	See the description above for TS1.

(4) Operation Description

[Omitted.]

(5) Timing Chart

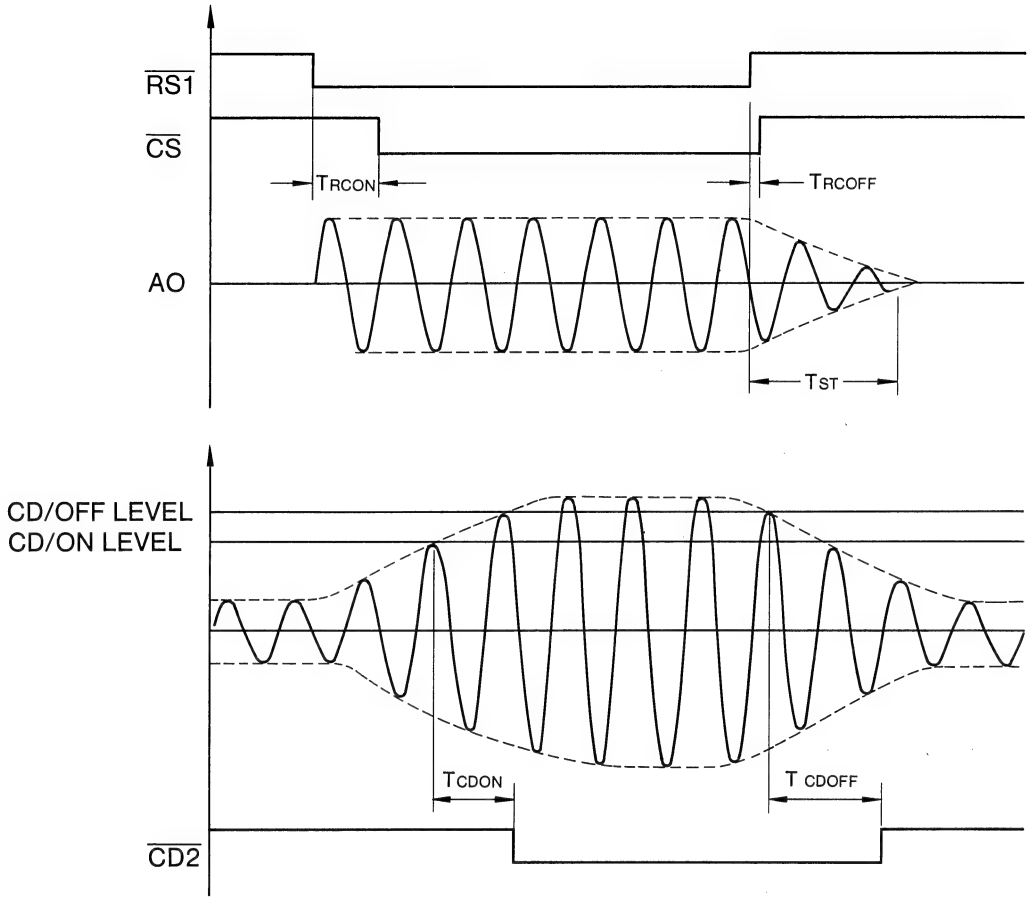


Figure C-33. MSM6946RS Timing Chart

C.7 MSM6234RS

(1) Overview

The MSM624RS is a DTMF (dual-tone multifrequency) signal generation C-MOS LSI for push-button-type telephones.

(2) Terminal Connection and Circuit Configuration

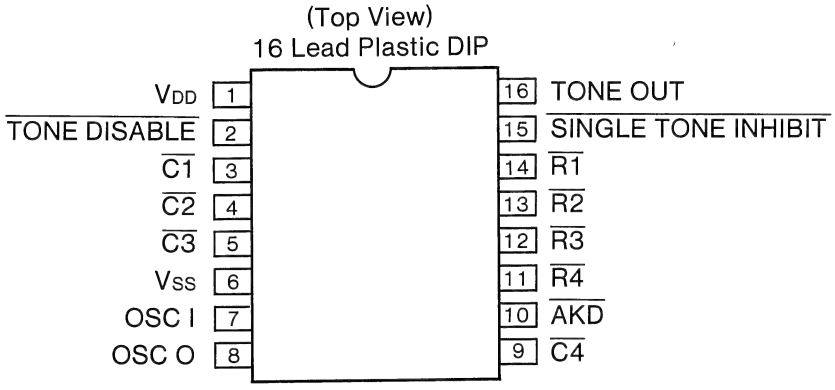


Figure C-34. MSM6234RS Terminal Connection

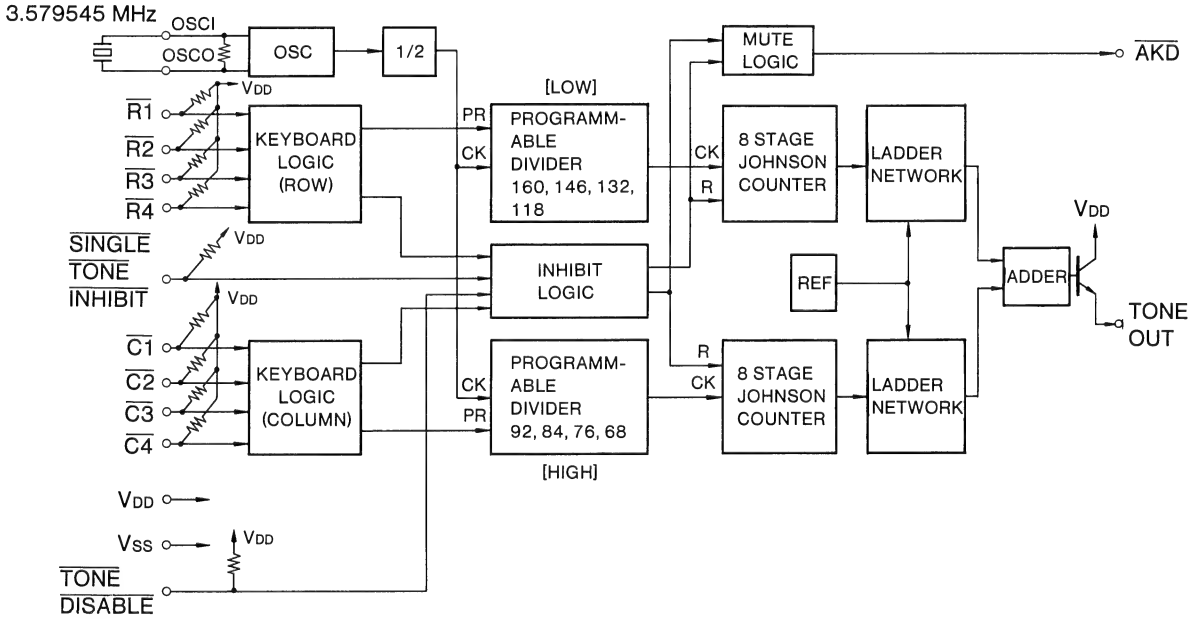


Figure C-35. MSM6234RS Circuit Configuration

(3) Terminal Description

Terminal symbol	Function
OSCI, OSCO	A terminal to which a 3.579545 MHz quartz oscillator is connected.
$\overline{R1}$, $\overline{R2}$, $\overline{R3}$, $\overline{R4}$ $\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$	A DTMF selection input terminal. R1-R4 selects the low frequency, and C1-C4 selects the high frequency. The relationship between the input signal and frequency is shown in Table C-7.
$\overline{AKD}$	This terminal will have a low level while a DTMF selection signal is being input. Otherwise, it will be open.
$\overline{TONE\ DISABLE}$	An input terminal that controls the TONE OUT terminal. With a high level input, the tone is output to the TONE OUT terminal, and with a low level input, tone output is disabled.
$\overline{SINGLE\ TONE}$ $\overline{INHI\ BIT}$	A single tone is output when two or more columns are selected for a single row or when two or more rows are selected for a single column. This is an input terminal for controlling the output of the TONE terminal. High level input: Outputs a single or dual tone; Low level input: Disables output of only the single tone to the TONE OUT terminal; DC level takes effect.
TONE OUT	An input terminal for DTMF selection. The low frequency and high frequency selected by (row,column) are combined and are output from this terminal.

Note: R1-R4: Row input
C1-C4: Column input

Effective input		TONE OUT frequency	Effective input		TONE OUT frequency
Low (row)	R1	699.1 Hz	High (column)	C1	1215.9 Hz
	R2	766.2 Hz		C2	1331.7 Hz
	R3	847.4 Hz		C3	1471.9 Hz
	R4	948.0 Hz		C4	1645.0 Hz

Table C-7. Relationship between TONE OUT Terminal and Output Frequency

(4) Operation Description

[Omitted.]

(5) Timing Chart

(a) TONE OUT Terminal Output Control

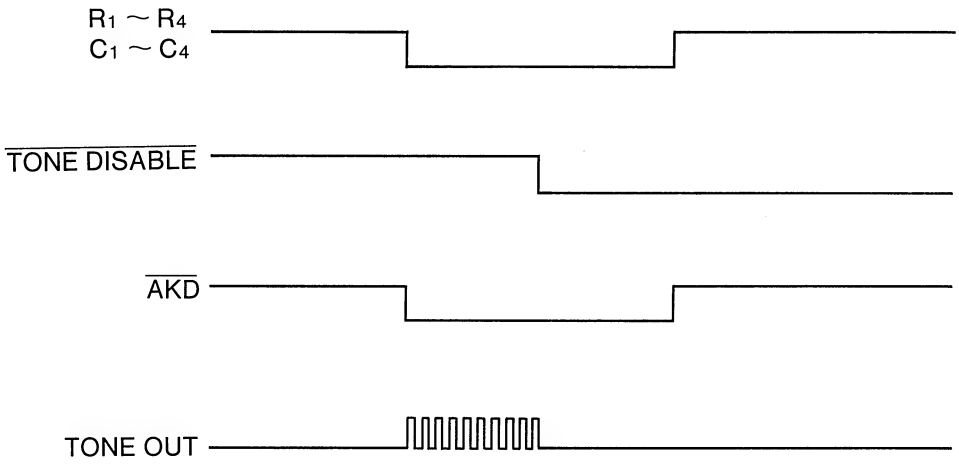


Figure C-36. MSM6234RS TONE OUT Terminal Output Control Timing Chart

(b) Relationship between R1-R4 and TONE OUT

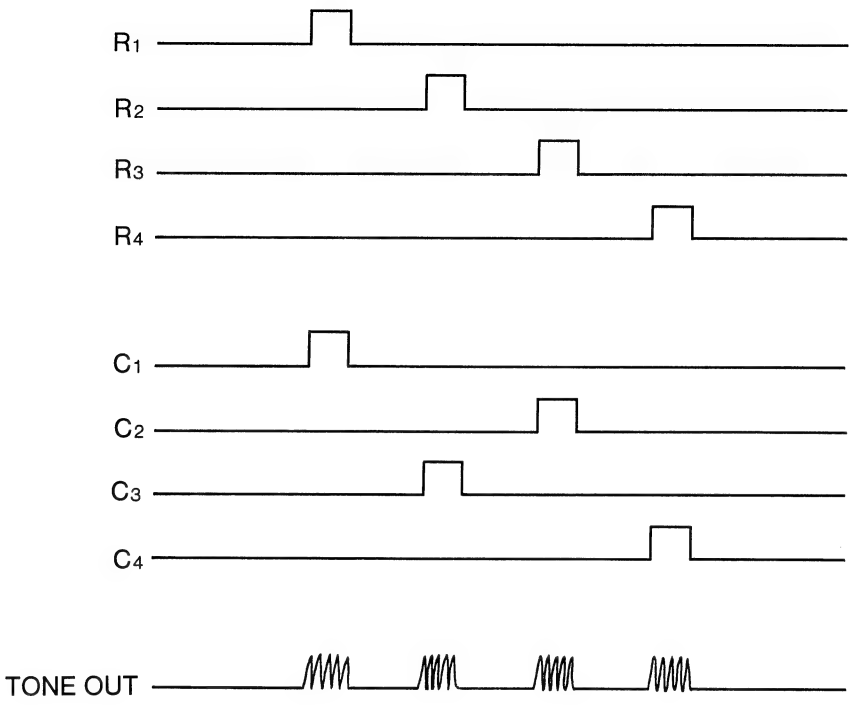


Figure C-37. MSM6234RS Relationship between R_1-R_4, C_1-C_4 and TONE OUT Timing Chart

C.8 HM6264LP-15

(1) Overview

The HM6264LP-15 is an 8192-word by 8-bit, DIP-type CMOS static RAM.

(2) Terminal Connection and Circuit Configuration

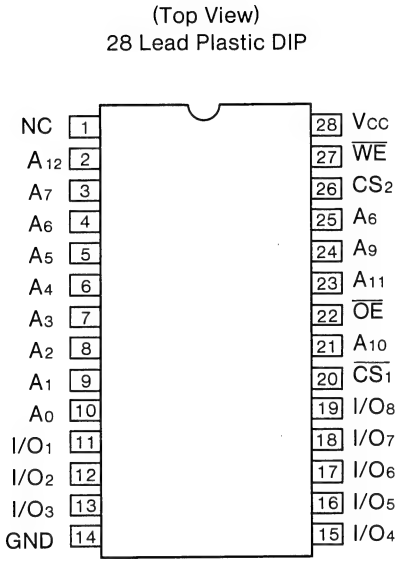


Figure C-38. HM6264LP-15 Terminal Connection

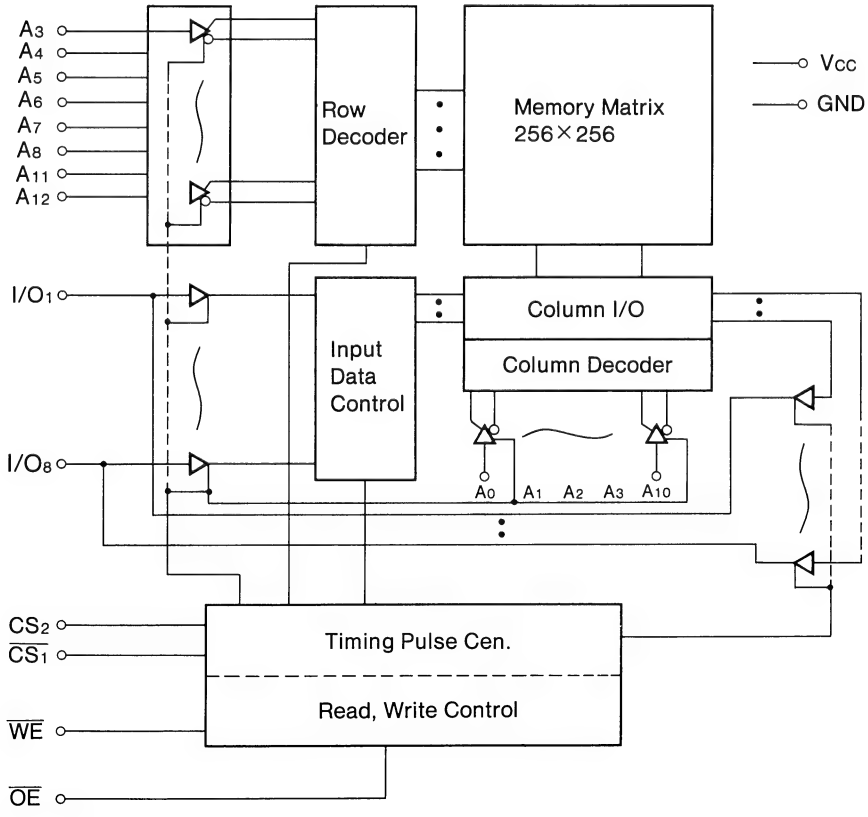


Figure C-39. HM6264LP-15 Circuit Configuration

(3) Terminal Description

Terminal symbol	Function
A0-A12	Address input terminal
I/O1-I/O8	Data I/O terminal
$\overline{CS1}$, CS2	Chip select input terminal
$\overline{OE}$	Out enable input terminal
$\overline{WE}$	Write enable input terminal
Vcc	Power supply
GND	Ground

(4) Operation Description

[Omitted.]

(5) Timing Chart

(a) Read Cycle

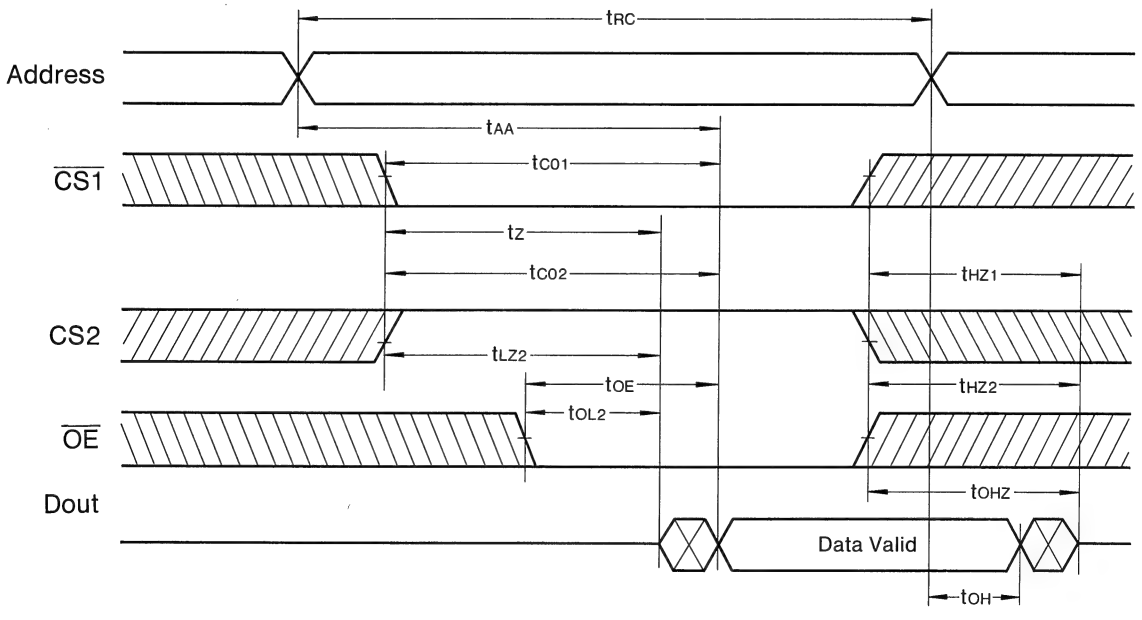


Figure C-40. HM6264LP-15 Read Cycle Timing Chart

(b) Write Cycle ($\overline{OE}$ Clock)

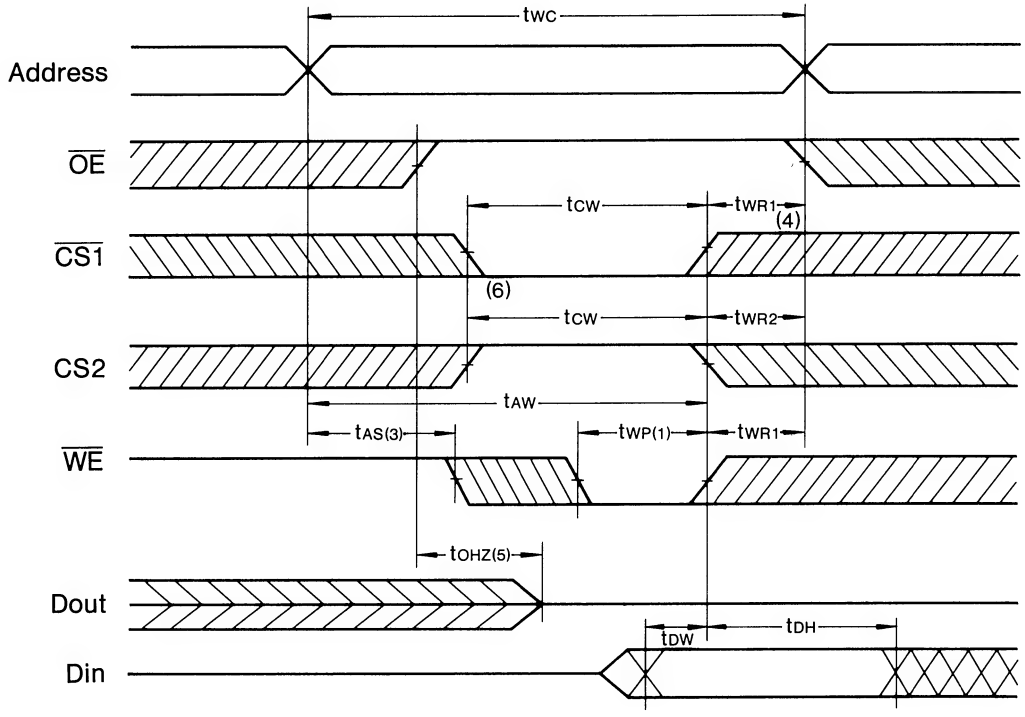


Figure C-41. HM6264LP-15 Write Cycle ($\overline{OE}$) Timing Chart

C.9 HM6264LFP-15

(1) Overview

The HM6264LFP is an 8192-word by 8-bit, FLP-type CMOS static RAM.

(2) Terminal Connection and Circuit Configuration

(Top View)
40 Lead Plastic FLP

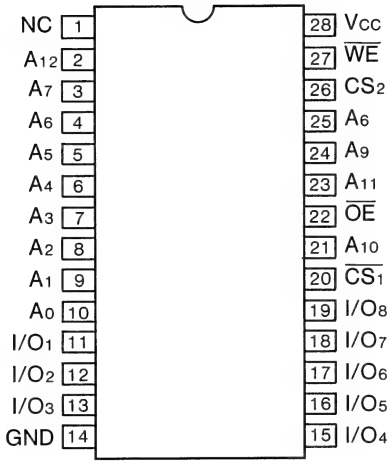


Figure C-42. HM6264LFP-15 Terminal Connection

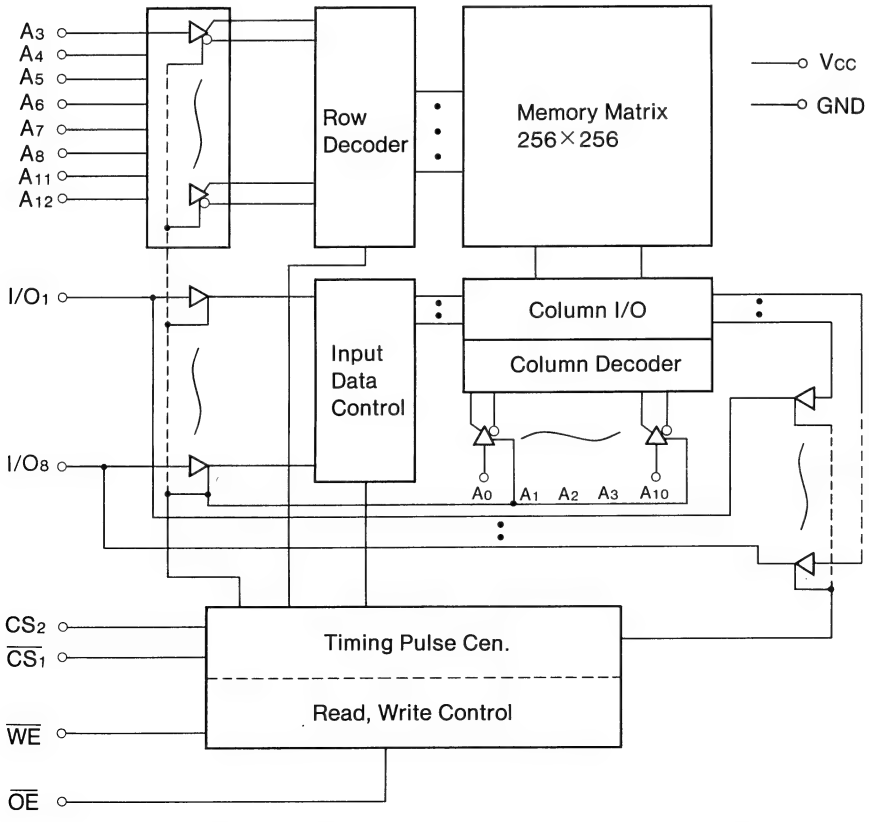


Figure C-43. HM6264LFP-15 Circuit Configuration

(3) Terminal Description

Terminal symbol	Function
A0-A12 **I/O1-I/O8**	Data I/O terminal
$\overline{CS_1}$, CS_2	Chip select input terminal
$\overline{OE}$	Out enable input terminal
$\overline{WE}$	Write enable input terminal
Vcc	Power supply
GND	Ground

(4) Operation Description
[Omitted.]

(5) Timing Chart

(a) Read Cycle

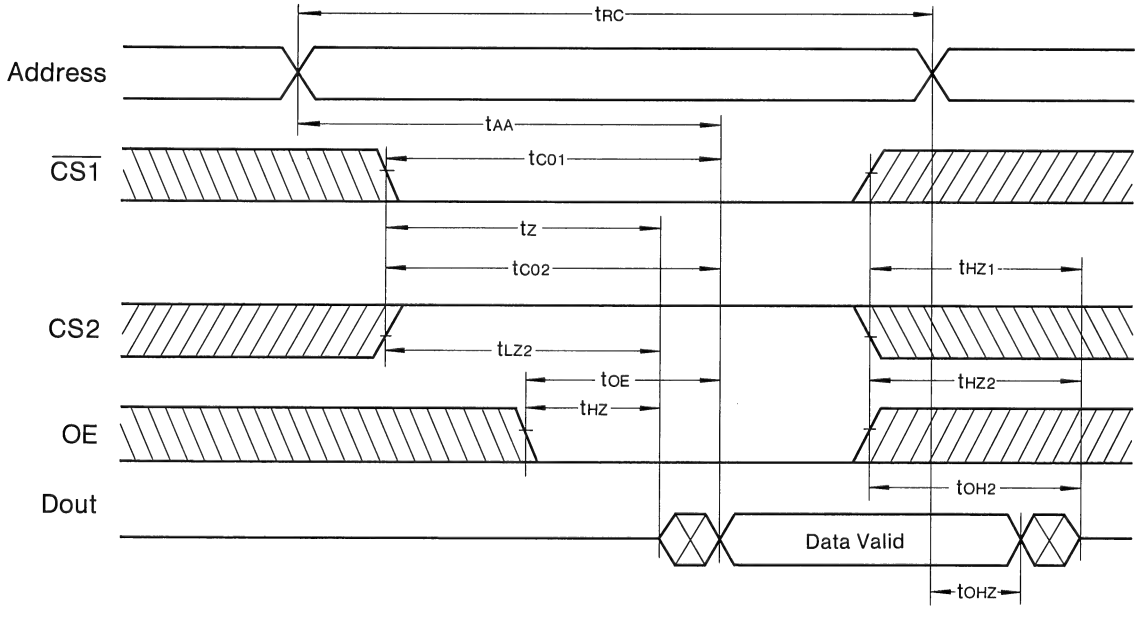


Figure C-44. HM6264LFP-15 Read Cycle Timing Chart

(b) Write Cycle ($\overline{OE}$ Clock)

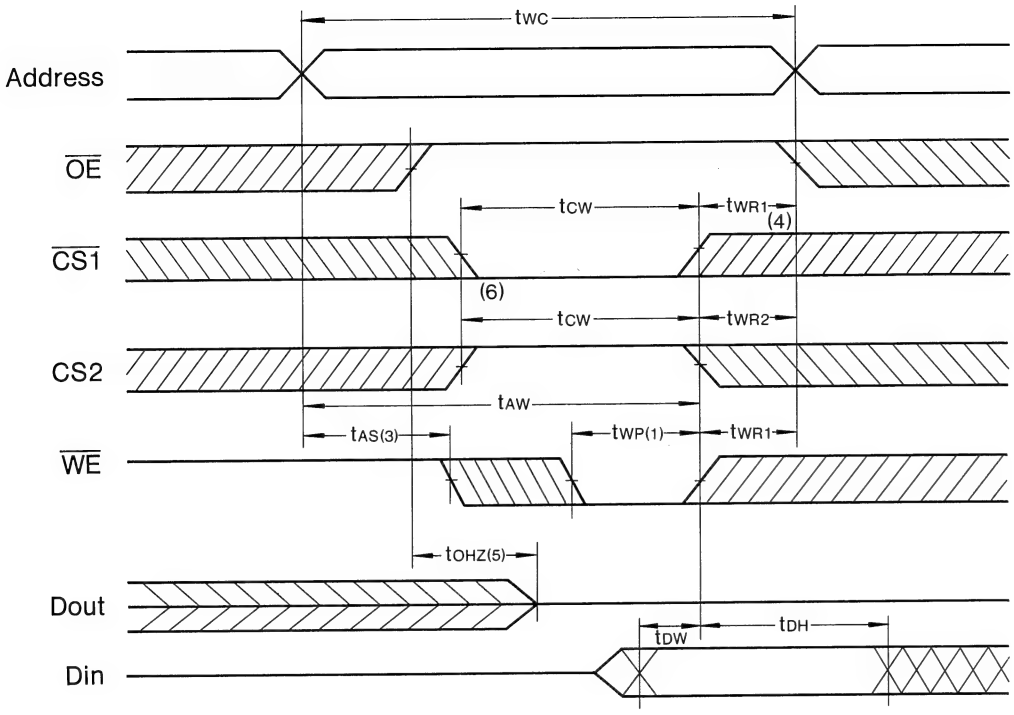


Figure C-45. HM6264LFP-15 Write Cycle ($\overline{OE}$) Timing Chart

C.10 HN613256P

(1) Overview

The HN613256P is a 32768-word by 8-bit, DIP-type mask programmable ROM.

(2) Terminal Connection and Circuit Configuration

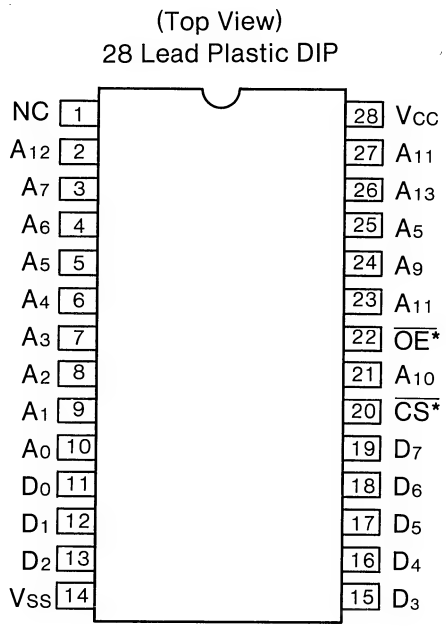


Figure C-46. HN613256P Terminal Connection

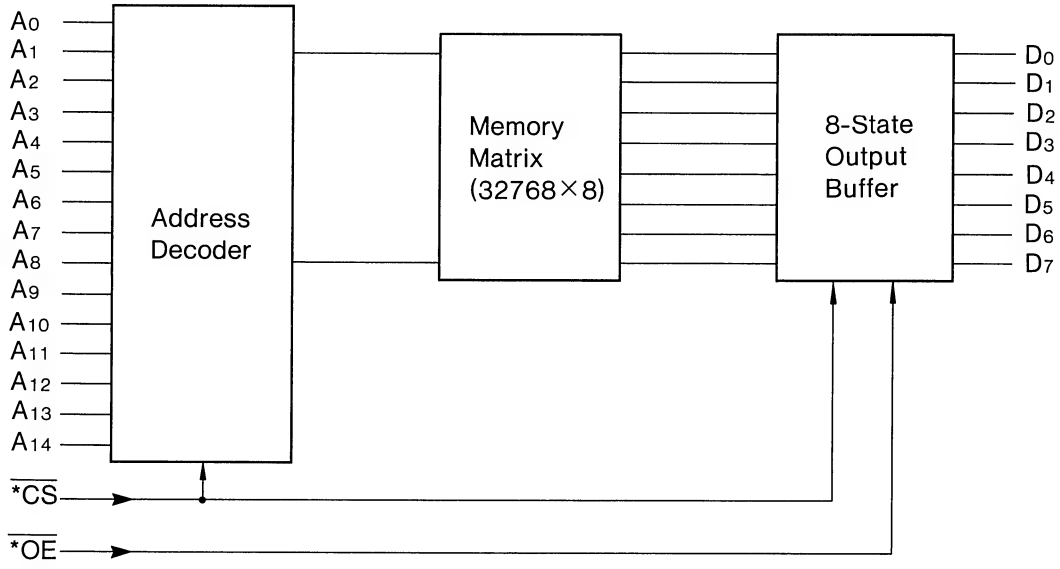


Figure C-47. HN613256P Circuit Configuration

(3) Terminal Description

Terminal symbol	Function
A0-A14	Address input terminal
D0-D7	Data I/O terminal
$\overline{CS}$	Chip select input terminal
$\overline{OE}$	Out enable input terminal
Vcc	Power supply
Vss	Ground

(4) Operation Description

[Omitted.]

(5) Timing Chart

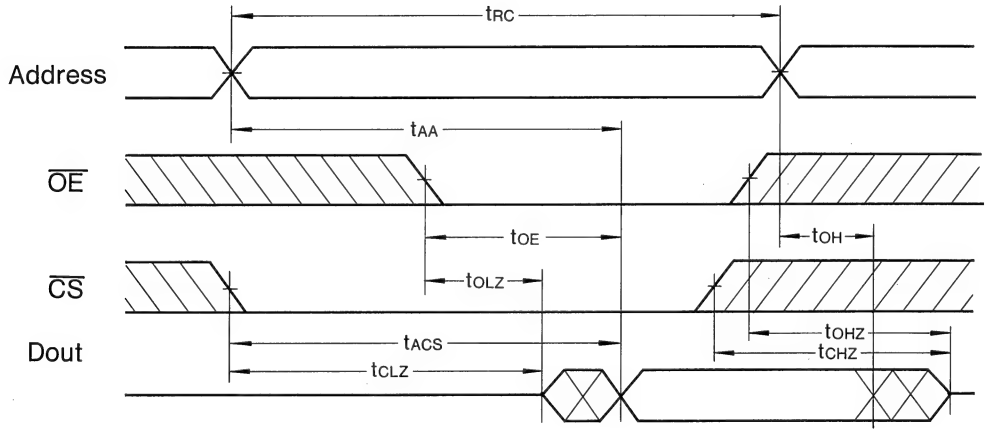


Figure C-48. HN613256P Timing Chart

C.11 WD2797

(1) Overview

The WD2797 is a floppy-disk drive control LSI of the WD279X series. This FDC is software-compatible with the FD179X series, and is equipped with a built-in write precompensation function, VFO, data separator, etc.

(2) Circuit Configuration and Terminal Connection

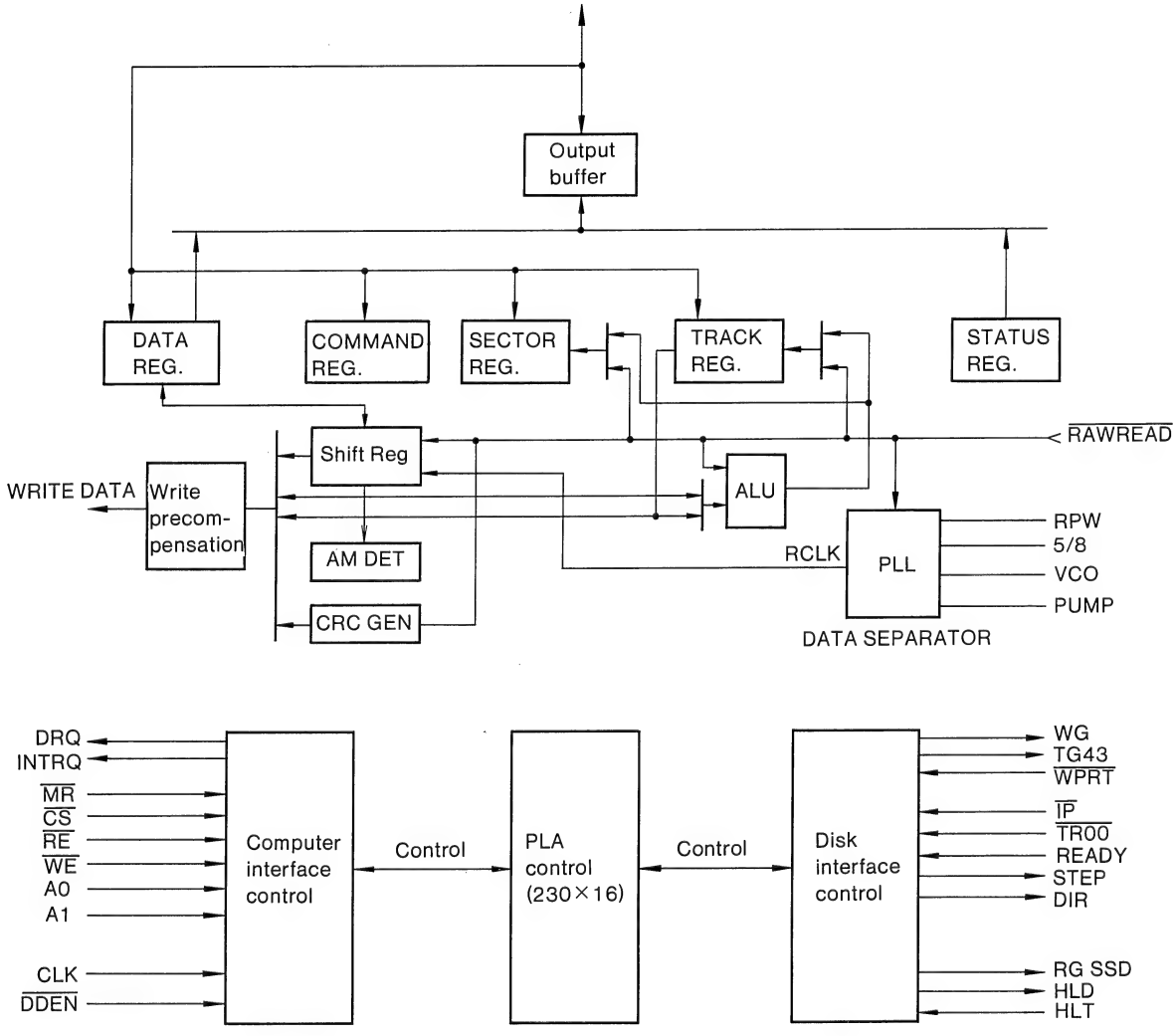


Figure C-49. WD2797PL-02 Circuit Configuration

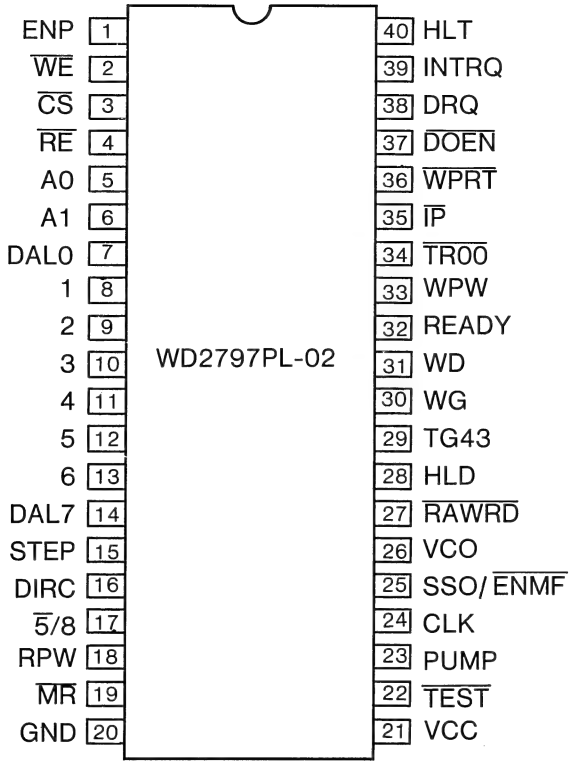


Figure C-50. WD2797PL-02 Terminal Connection

(3) Terminal Description

Terminal symbol	Function
ENP	An abbreviation for enable precompensation. Write precompensation is performed when ENP = 1.
$\overline{MR}$	WD2797 is reset by entering a negative pulse to $\overline{MR}$ for more than 50ms.
GND	Ground terminal.
Vcc	A power supply (+5V) terminal.
$\overline{WE}$	A write pulse signal for writing from the CPU into WD2797.
$\overline{RE}$	A read pulse signal for the CPU to read WD2797.
$\overline{CS}$	A signal used for selecting WD2797.

<table>
<tr><th>Terminal symbol</th><th>Function</th></tr>
<tr><td>A0, A1</td><td>An internal register select signal.
<table>
<tr><th>$\overline{CS}$</th><th>A1</th><th>A0</th><th>$\overline{RE}$</th><th>$\overline{WE}$</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Status REG</td><td>Command REG</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Track REG</td><td>Track REG</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Sector REG</td><td>Sector REG</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Data REG</td><td>Data REG</td></tr>
</table></td></tr>
<tr><td>DAL0-DAL7</td><td>A bidirectional data bus used for data transfer, status read, etc.</td></tr>
<tr><td>CLK</td><td>A 1 MHz clock input terminal.</td></tr>
<tr><td>DRQ</td><td>A data request terminal for read/write operation. This signal is automatically reset if a read or write is not performed.</td></tr>
<tr><td>INTRQ</td><td>This signal level is set to HIGH whenever a command is completed. This signal is reset when the status register is read.</td></tr>
<tr><td>STEP</td><td>A step signal that initiates a seek operation by the floppy-disk drive's head.</td></tr>
<tr><td>DIRC</td><td>A signal that determines the seek operation direction. The head seeks inward when the signal is 1 and seeks outward when the signal is 0.</td></tr>
<tr><td>$\overline{5}$/8</td><td>The VCO frequency differs between a 5-inch floppy-disk drive and an 8-inch floppy-disk drive. The frequency selection is made from this terminal.</td></tr>
<tr><td>$\overline{TEST}$</td><td>The VCO central frequency and write precompensation calibration are performed with this signal set to 0.</td></tr>
<tr><td>PUMP</td><td>A terminal used to set the VCO output charge pump constant. SSO = 0 for head No. 0, and SSO = 1 for head No. 1.</td></tr>
<tr><td>SSO/$\overline{ENMF}$</td><td>The VCO central frequency is determined by the capacitance of the capacitor connected to this pin.</td></tr>
<tr><td>VCO</td><td>An abbreviation for read pulse width. The phase comparator in the data separator is controlled by this terminal.</td></tr>
<tr><td>RPW</td><td>Read data from the floppy-disk drive is entered to this terminal.</td></tr>
<tr><td>HLD</td><td>An output signal to the floppy-disk drive. The head contacts the disk surface when this signal level is HIGH.</td></tr>
<tr><td>TG43</td><td>TG43 level is LOW for track numbers 0 through 43, and is HIGH for track numbers above 43.</td></tr>
<tr><td>$\overline{RAW\ READ}$</td><td>Read data from the FDD is entered to this terminal.</td></tr>
</table>

Terminal symbol	Function
WG	An abbreviation for write gate. WG level is HIGH when writing to a floppy-disk drive.
WD	An abbreviation for write data; a write signal to a floppy-disk drive.
READY	An input terminal for the READY signal from a floppy-disk drive.
WPW	An abbreviation for write precomp width. A terminal used for setting the write compensation value.
$\overline{\text{TRACK 00}}$	An input terminal for the TRACK 00 signal from the floppy-disk drive.
$\overline{\text{IP}}$	An abbreviation for index pulse. An input terminal for the INDEX signal from the floppy-disk drive.
$\overline{\text{WPRT}}$	An abbreviation for write protect. An input terminal for the WRITE PROTECT signal from the floppy-disk drive.
$\overline{\text{DDEN}}$	An abbreviation for double density. Double-density is selected if the $\overline{\text{DDEN}}$ level is LOW; single-density is selected if the $\overline{\text{DDEN}}$ level is HIGH.
HLT	A timing signal for indicating termination of head load. An HLT level of HIGH indicates termination of head load.

(4) Operation Description

[Omitted.]

(5) Timing Chart

(a) CPU Interface Timing

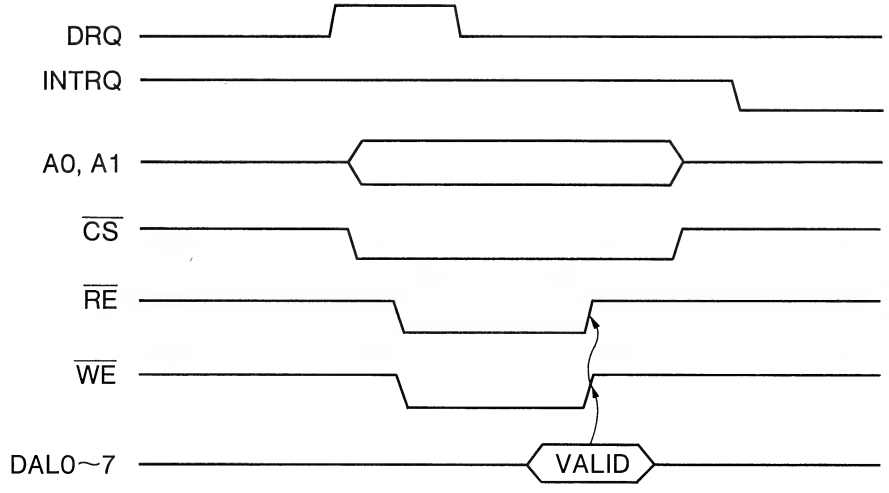


Figure C-51. WD2797LFP-02 CPU Interface Timing Chart

(b) SEEK operation

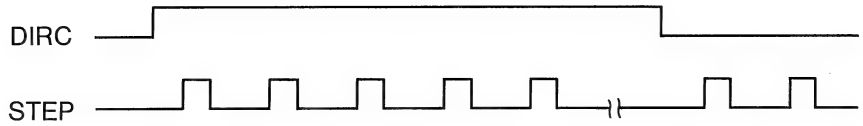


Figure C-52. WD2797 SEEK Timing Chart

(c) WRITE DATA Timing

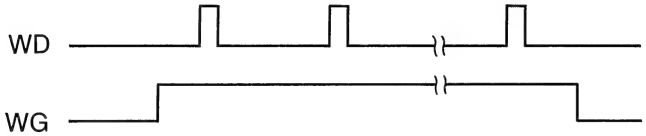


Figure C-53. WD2797 WRITE DATA Timing Chart

(d) READ DATA Timing

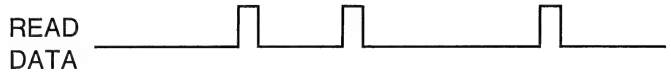


Figure C-54. WD2797 READ DATA Timing Chart

C.12 μPD8257

(1) Overview

μPD8257 is a 4-channel DMA (direct memory access) controller. Its main function is to control data read/write operation between the storage and the peripheral devices without the intervention of the CPU, by generating R/W control signals and continuous memory addresses.

(2) Terminal Connection and Circuit Configuration

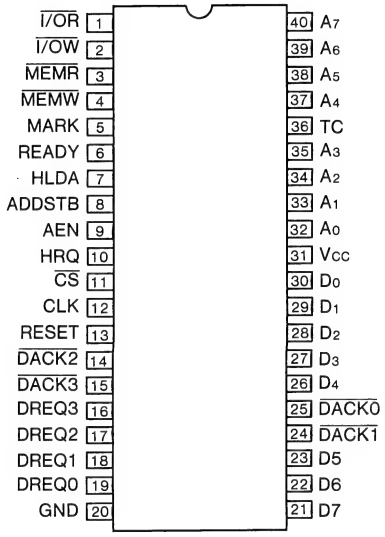


Figure C-55. μPD8257 Terminal Connection

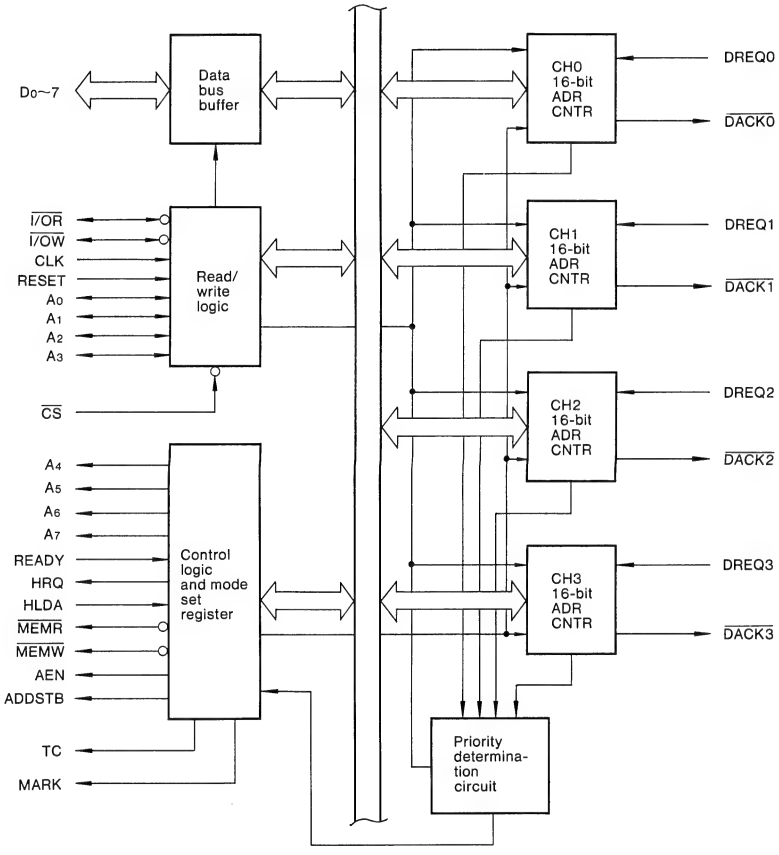


Figure C-56. μPD8257 Circuit Configuration

(3) Terminal Description

Terminal symbol	Function
$\overline{\text{I/OR}}$	A terminal used as an input terminal when in the slave mode. By entering a low level, the 8-bit status register, the 16-bit DMA address register, or the most or least significant byte of the 16-bit TC register is read. A control output signal is output when in the master mode. It is used for receiving data from the peripheral devices during the DMA write cycle.
$\overline{\text{I/OW}}$	A terminal used as an input terminal when in the slave mode. By entering a low level, loading is enabled for the 8-bit mode set register, the 16-bit DMA address register, or the most or least significant byte of the TC register. When in the master mode, it is used for the control output signal that allows data to be written to the peripheral devices.
$\overline{\text{MEMR}}$	When in the DMA read cycle, the terminal is used for reading the data from the storage location that is addressed. The terminal will have a high impedance when in the slave mode.
$\overline{\text{MEMW}}$	When in the DMA write cycle, the terminal is used for writing the data to the storage location that is addressed. The terminal will have a high impedance when in the slave mode.
MARK	A terminal used in notifying the peripheral devices that the DMA cycle that is currently being executed is the 128th cycle from the previous MARK signal. MARK occurs at every 128th cycle from the end of a data block. MARK is issued after the elapse of 128 cycles from the beginning of a data block, if the total number (n) of DMA cycles is divisible by 128, and if n-1 is loaded in the TC register.
READY	If a storage that is used is slow and requires a long cycle, the memory read/write cycle can be extended by asynchronously entering a low-level signal to this input terminal. Doing so will cause the μPD8257 to place a weight on the internal state and extend the memory read/write cycle.
HLDA	An input terminal for receiving the HLDA signal. This HLDA signal is returned from the 8080A when a hold request is accepted and indicates that the μPD8257 has gained control of the system bus. When in this state, the bus output from the 8080A has a high impedance.
ADDSTB	An output terminal for a strobe signal used for sending the most significant memory address byte from a data bus to the μPB8218. The terminal is usually connected to the STB input of the μPB8212.

Terminal symbol	Function
AEN	The output of this terminal is sent to the system controller bus enable ($\overline{\text{BUSEN}}$) input on the μPB8228. The output also sets the data bus and the control bus used for output from the μPB8228 to a high impedance. To disable devices not involved in DMA from responding during a DMA cycle, this terminal signal may also be employed to use the address bus driver enable input in the system to disable the system address bus. The signal is also used to disconnect the μPD8257 data bus from the system data bus so that a special timing restriction need not be imposed on the system bus when transferring the most significant 8 bits of the DMA address from the μPD8257 data bus. When the μPD8257 is being used in an I/O device configuration (for memory mapping), the AEN output is used to prevent an I/O device from being selected when the DMA address enters the address bus. The selection of an I/O device must be made by outputting a DMA acknowledge to 4 channels.
HRQ	An output signal used for requesting control of the system bus. The terminal is connected to the HOLD input on the 8080A when only one μPD8257 chip is used in the system. When two or more chips are used, an additional circuit (priority encoder) must be established so that two or more HRQ signals are summarized by one HOLD request signal.
$\overline{\text{CS}}$	When the μPD8257 is being programmed or read in the slave mode, the I/O read and I/O write inputs are enabled. $\overline{\text{CS}}$ is automatically disabled in the master mode so that $\overline{\text{CS}}$ itself is not selected during DMA operation.
CLK	A clock input. Normally, the ϕ2 (TTL) signal output by the μPB8224 (clock generator) is fed to this terminal.
RESET	Normally, receives the asynchronous reset output from the μPB8224 to clear all the registers and control signal of the μPD8257, and to implement the slave mode. Also, any and all operations are suspended when a reset signal is entered, regardless of the μPD8257 state, and idle state (S_1) is entered.
$\overline{\text{DACK0}}$–$\overline{\text{DACK3}}$	Informs all peripherals connected to each channel that a DMA cycle is allowed.
$\overline{\text{DREQ0}}$–$\overline{\text{DREQ3}}$	An asynchronous channel request input that is used independently by the peripherals to request a DMA cycle from μPD8257. Unless in the rotation priority mode, DRQ3 has the lowest priority and DRQ0 has the highest priority. $\overline{\text{DRQn}}$ input will cause a high level to be maintained until $\overline{\text{DACKn}}$ is received. For a multi DMA cycle (burst mode), $\overline{\text{DRQn}}$ input will cause a high level to be maintained until a DACKn of the last cycle is received.

Terminal symbol	Function
D_0-D_7	When the μPD8257 is being programmed by the 8080A (CPU), data that is output from the 8080A to be coded in the DMA address register, the most and least significant 8 bits of the TC register, or the 8 bits of the mode set register is received from the data bus. When the 8080A is reading the contents of the DMA address register, the TC register, or the status register, the data is sent to the 8080A over the data bus. (This description is for the slave mode.) During the DMA cycle (μPD8257 is the bus master), the most significant 8 bits of a memory address are sent from the μPB8218 from one DMA address register over the data bus. These address bits are transmitted at the start of the DMA cycle. After the transmission, the address bits are used for the memory data transmission which occurs during the remaining portion of the DMA cycle.
A_0-A_3	In the slave mode, this input terminal is used to select the register that is to be read out or programmed. In the master mode, the least significant 4 bits of the 16-bit memory address from the μPD8257 are output from this terminal.
A_4-A_7	In the master mode, bits 4-7 of the 16-bit memory address from the μPD8257 are output from this terminal. In the slave mode, the terminal will have a high impedance.
TC	The TC output informs the currently used peripherals that the DMA cycle that is currently being executed belongs to the last cycle of the data block. If the TC stop bit in the mode set register is set, the channel that is selected is automatically disabled at the end of the DMA cycle. The TC signal is output when the value of bit 14 of the TC register of the selected channel becomes 0. It is necessary for n-1 to be loaded in the least significant 14 bits of the TC register, where n is the number of DMA cycles to be executed.

(4) Operation Description

[Omitted.]

(5) Timing Chart

(a) READ Timing

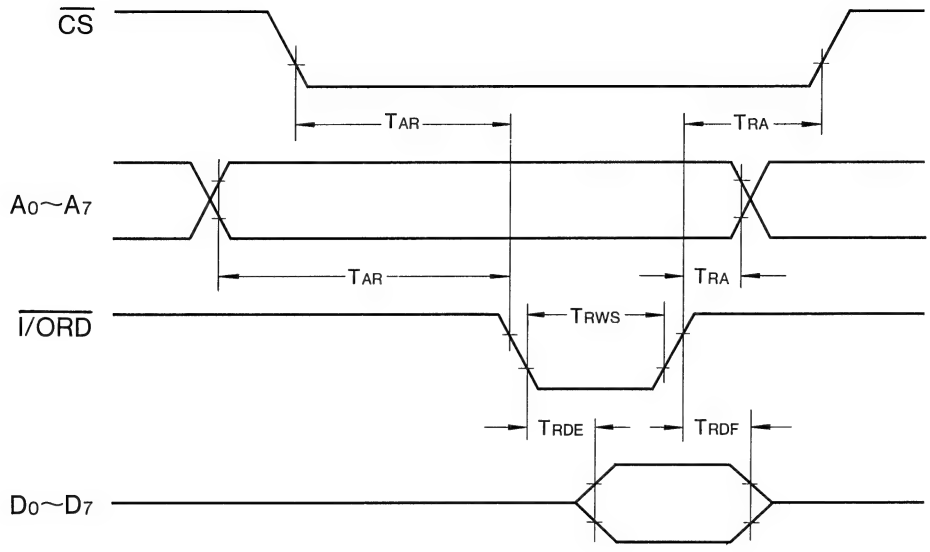


Figure C-57. μPD8257C-5 READ Timing Chart

(b) WRITE Timing

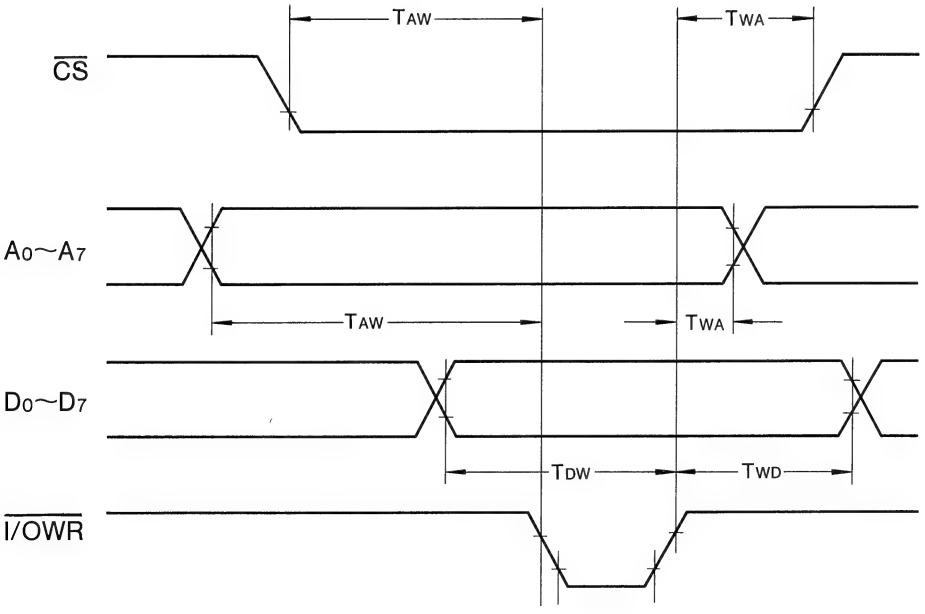


Figure C-58. μPD8257C-5 WRITE Timing Chart

(c) DMA Mode Timing

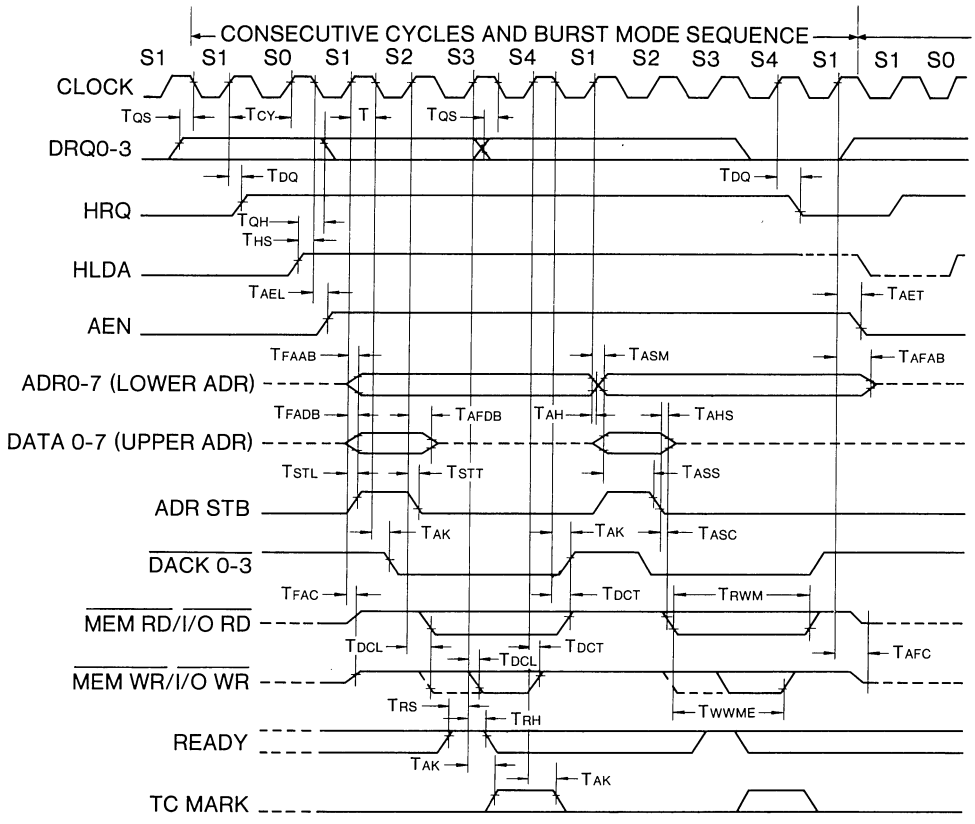


Figure C-59. μPD8257C-5 DMA Mode Timing Chart (a)

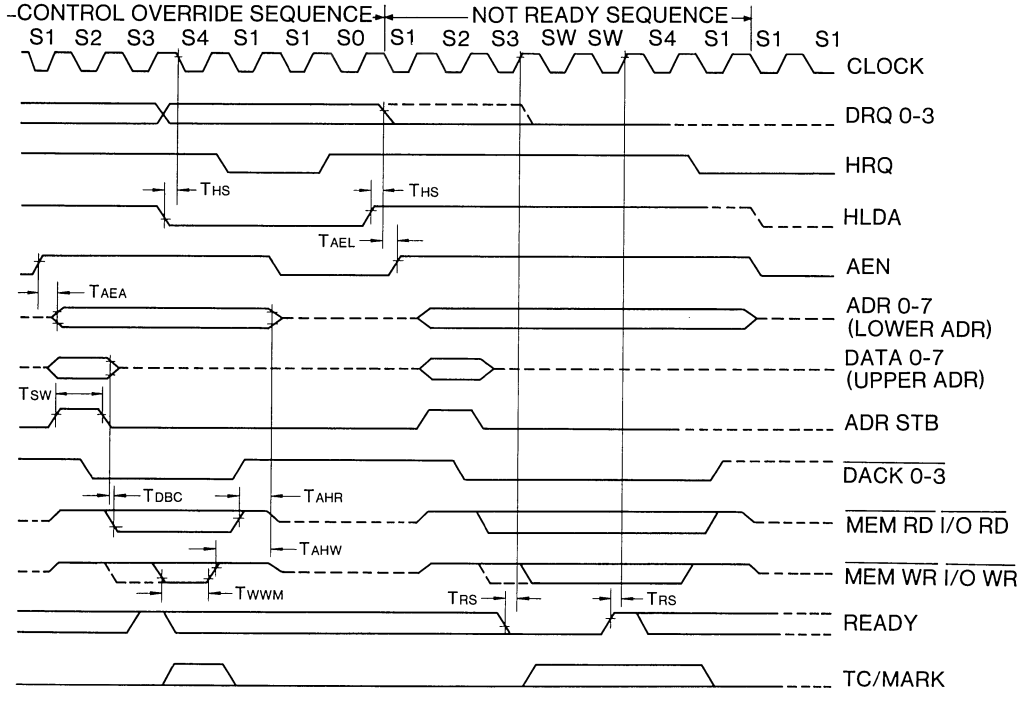


Figure C-60. μPD8257C-5 DMA Mode Timing Chart (b)

C.13 HD61830

(1) Overview

The HD61830 is an LSI for controlling the liquid crystal dot matrix graphics display. A display data sent from an 8-bit microprocessor is stored in an external display RAM. A dot matrix liquid crystal drive signal is then generated.

Either of two modes, the graphics mode or the character mode, may be selected. With the graphics mode, one bit of data in the external RAM corresponds to lighting or not lighting a single dot. With the character mode, a character code is stored in the external RAM. The character code is expanded into a character display by a built-in character generator ROM.

(2) Terminal Connection and Circuit Configuration

(Top View) 60 Lead Plastic DIP

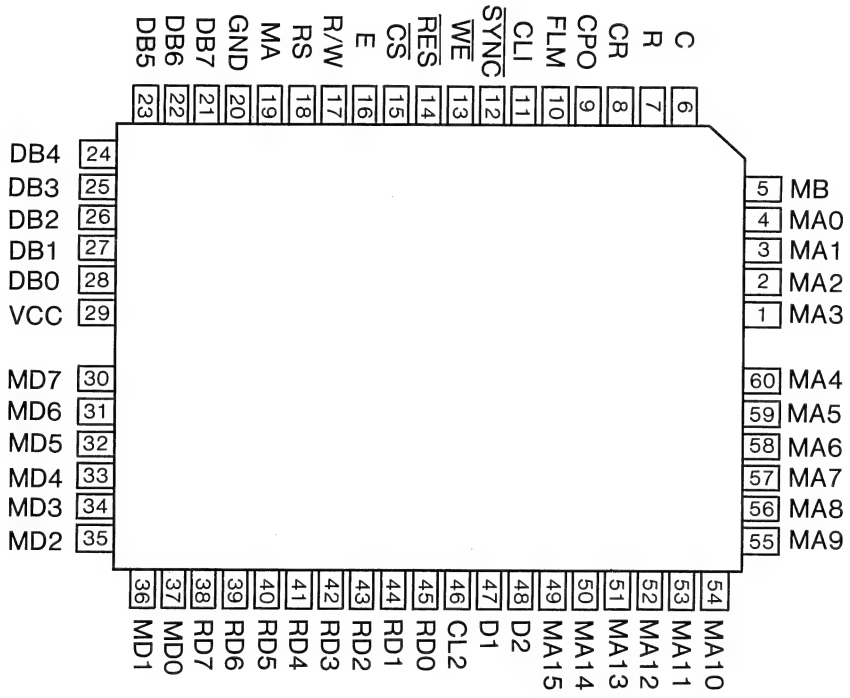
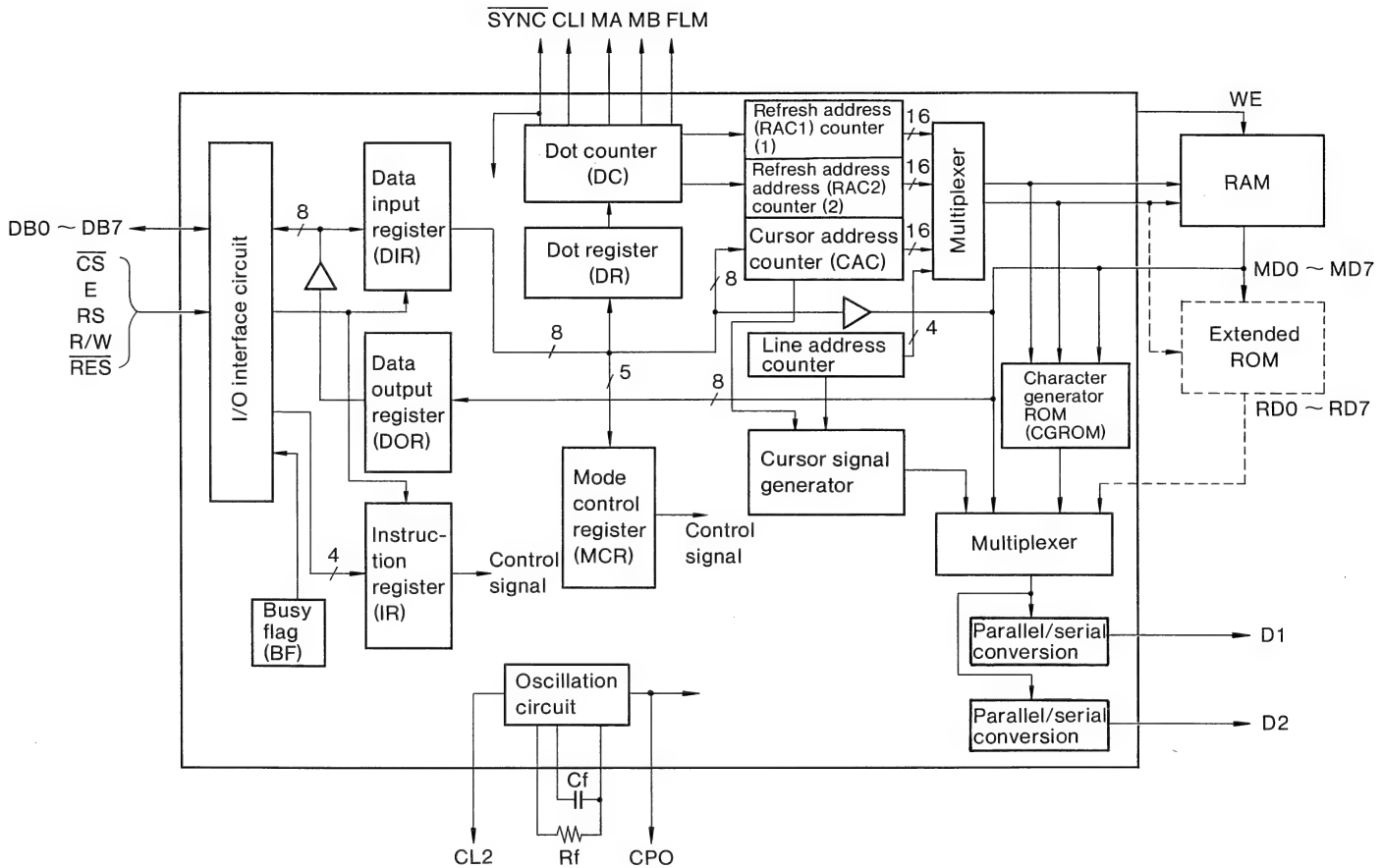


Figure C-61. HD61830 Terminal Connection



* When extended ROM is used, MA0 ~ MA11 are used as the RAM address, and MA12 ~ MA15 are used as the extended ROM.

Figure C-62. HD61830 Circuit Configuration

(3) Terminal Description

Terminal name	Function
DB0-7	Data bus: Three-state I/O common terminal DB0-DB7 are used for transmitting data to and receiving data from MPU.
$\overline{CS}$	Chip select: Select mode when $\overline{CS} = 0$.
R/W	Read/write: R/W = 1: HD61830 to MPU R/W = 0: MPU to HD61830
RS	Register select: RS = 1: Instruction register RS = 0: Data register
E	Enable: Data is written using the rising and falling edge timing of E. Data can be read while E = 1.
CR, R, C	CR oscillator.
RES	Reset: Set the reset to 0 to turn off the display and to enter the slave mode.
MA0-15	Display RAM address output. When using the character display, MA12-MA15 display the line codes for the external CG MA12-MA15 select the character cells and the low address bits select the individual dots of the character. (0: 1st line of character; F: 16th line of character)
MD0-7	Display data bus: Three-state I/O common terminal.
RD0-7	ROM data input: Dot data from the external character generator is entered here.
WE	Write enable: RAM write signal.
CL2	Display data shift clock.
CL1	Display data latch signal.
FLM	Frame signal: Display synchronization.
MA	Liquid crystal drive signal: AC creation signal; method A.
MB	Liquid crystal drive signal: AC creation signal; method B.
D1, D2	Display data serial output: D1: upper screen D2: lower screen
CPO	Slave clock.
SYNC	Parallel operation synchronization signal: Three-state I/O common terminal (with pull-up MOS): Master: Synchronization signal is output Slave: Synchronization signal is input

(4) Operation Description

Description of Block Functions

■ Register

The HD61830 has five different registers: instruction register (IR), data input register (DIR), data output register (DOR), dot register (DR) and mode control register (MCR).

The IR register stores instruction codes such as the start address, the cursor address specification, etc. The register is comprised of four bits, and the least significant four bits of the data bus are written into DB0-DB3.

The DIR register is used for temporary storage of data that is to be written to DR, MCR, etc. The register is comprised of eight bits.

The DOR register is used as temporary storage when reading data from an external RAM. The register is comprised of eight bits. After cursor address information is written to CAC from DIR and a memory read command is set in IR (falling edge of E is the latch timing), an internal operation will cause the data in an external RAM to be read into DOR. Data transmission to MPU is completed when MPU reads DOR in the next instruction (the contents of DOR when E has a high level are output to the data bus).

The DR register stores the dot information, such as the character pitch or the number of vertical dots, etc., necessary for displaying data on the liquid crystal display. All information sent from MPU passes through DIR before it is written.

The MCR register stores the display status of the liquid crystal, such as whether the display is on or off, or whether the cursor is on, off or blinking. The register is comprised of six bits. Information sent from MPU passes through DIR before it is written.

■ Busy Flag (BF)

The HD61830 is engaged in an internal operation if the busy flag is 1. Hence, the next instruction will not be accepted. The busy flag status is output to DB7 only if RS = and R/W = 1. Check that the busy flag is 0 before writing the next instruction.

■ Dot Counter (DC)

The dot counter generates liquid crystal display timing in accordance with the contents of DR.

■ Refresh Address Counters (RAC1, RAC2)

The refresh address counters control the addresses of the external RAM, the character generator ROM (CGROM), and the extended ROM. There are two types: RAC1 and RAC2. RAC1 is for the upper screen, and RAC2 is for the lower screen. When in the graphics mode, a 16-bit data which is used as an address signal for the external RAM is output. When in the character mode, the most significant four bits are ignored, and the four bits from the line address counter are output instead. These four bits are used as the extended ROM address.

■ **Character Generator ROM**
The character generator ROM has a total bit size of 7360 bits and stores data for 192 types of characters. A character code from the external RAM and a line code from the line address counter are added to the address signal to output a 5-bit dot data.

There are 192 character fonts: 160 5×7 fonts and 32 5×10 fonts. By using an external-extended ROM, it is possible to use an 8×16 format (maximum of 256 types).

■ **Cursor Address Counter**
A 16-bit counter that can be preset by instructions and which stores the address for reading or writing either dot data or character code data in an external RAM. The value of the cursor address counter is automatically incremented by one when a display data is read or written, or when a bit set or a bit clear instruction is executed.

■ **Cursor Signal Generator**
When in the character mode, the cursor display can be controlled by an instruction. A cursor is displayed when the cursor address counter and the line address counter reach a prescribed value.

■ **Parallel/Serial Conversion**
Parallel data from an external RAM, the character generator, or the extended ROM is transmitted simultaneously to the liquid crystal drive circuits for the upper screen and the lower screen after being converted to serial data by two parallel/serial converter circuits.

Display Control Instructions:
Display is controlled by writing data into the instruction register and into the 13 data registers. The RS signal is used to distinguish the instruction register from the data registers. An 8-bit data is first written into the instruction register with RS = 1 to specify the data register code. Next, with RS = 0, an 8-bit data is written into the data register to execute the prescribed instruction.

New instructions are not accepted while an instruction is being executed. Since the BUSY flag is set to 1 when an instruction is being executed, read and check that the BUSY flag is 0 before writing in a new instruction.

1. Mode Control

Write code $"00" in the instruction register to specify the mode control register. (Hexadecimal notation is used for $"00".)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	0	1	0	0	0	0	0	0	1	0
Mode control register	0	0	0	0	MODE Data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphics/ character display
1/0	1/0	0	0	0	0	Cursor OFF	Internal CG	Character display
		0	1			Cursor ON		
		1	0			Cursor OFF character blink		
		1	1			Cursor blink		
		0	0		1	Cursor OFF	External CG	
		0	1			Cursor ON		
		1	0			Cursor OFF character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphics mode
Display ON/OFF	Master/ slave	Blink	Cursor	Mode	External/ internal CG			

1: Master mode
0: Slave mode

1: Display ON
0: Display OFF

Figure C-63. Mode Control Register

2. Character Pitch Set

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	0	0	0	1
Character pitch register	0	0	(Vp-1) binary				0	(H_P – 1) binary		

V_p is the number of dots per character in the vertical direction. V_p must be set considering the spacing necessary between the characters above and below. This value is only meaningful when in the character display mode; it is ignored in the graphics mode.

Hp represents the number of dots per character in the horizontal direction when in the character display mode. It also includes the space between the subject character and the character to the right. When in the graphics mode, Hp indicates the number of bits that appear in one byte of display data from the RAM.

The Hp value may be one of the following:

H_p	DB_2	DB_1	DB_0	
6	1	0	1	Horizontal character pitch of 6
7	1	1	0	Horizontal character pitch of 7
8	1	1	1	Horizontal character pitch of 8

3. Character Count Set

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	0	0	1	0
Character count register	0	0	0	(H_N – 1) binary						

H_N represents the number of characters in the horizontal direction when in the character display mode. When in the graphics mode, $H_N$represents the number of bytes in the horizontal direction. Let n be the total number of dots in the horizontal direction on the screen.

$$n = H_P \times H_N$$

Any number from 0 to 127 (decimal) may be set for H_N.

4. Time-Division Count Set (Display Duty)

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	0	0	1	1
Time division count register	0	0	0	$(H_N - 1)$ binary						

N_X represents the time-division count for the display. The display duty will, therefore, be $1/N_X$. Any value from 0 to 127 (decimal) may be set for N_X.

5. Cursor Position Set

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	0	1	0	0
Time division count register	0	0	0	$(N_X - 1)$ binary						

C_P represents the line where the cursor is to be displayed, when in the character display mode. For example, if $C_P = 8$ (decimal) is specified, the cursor will appear at the bottom of the character if a 5×7 dot font is being used. The horizontal length of the cursor is equivalent to H_P, the horizontal-direction character pitch. Any value from 1 to 16 (decimal) may be specified for C_P. However, if the C_P value is less than or equal to V_p, the vertical-direction character pitch, the cursor will be given priority. If the cursor display is ON, or if C_P is larger than Vp, the cursor is not displayed. The horizontal length of the cursor is equivalent to the value of H_P.

6. Display Start Least Significant Address Set

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	1	0	0	0
Display start address register (most significant byte)	0	0	Least significant start address							

7. Display Start Most Significant Address Set

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	1	0	0	1
Display start address register (most significant byte)	0	0	Most significant start address							

This instruction writes the value of the display start address in the display start address register. The display start address represents the storage address in the RAM of the data that is to be displayed at the upper-left corner of the screen.

In the graphics mode, the start address is comprised of 16 bits, divided into the most significant and least significant 8 bits. When in the character display mode, the start address is comprised of 12 bits, divided into the 4 least significant bits (DB_3– DB_0) of the most significant address, and 8 bits of the least significant address. The most significant 4 bits of the most significant address are ignored.

8. Cursor Address (Least Significant) Set (RAM Write Least Significant Address)

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	1	0	1	0
Display start address register (most significant byte)	0	0	(Least significant cursor address) binary							

9. Cursor Address (Most Significant) Set (RAM Write Most Significant Address)

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	1	0	1	1
Display start address register (most significant byte)	0	0	(Most significant cursor address) binary							

This instruction writes a value of the cursor address in the cursor address counter. The cursor address indicates the address to be used when passing display data and character code to and from the RAM. The data in the storage address specified by the cursor address is read or written. In the character display mode, the cursor is displayed at the position specified by the cursor address.

10. Display Data Write

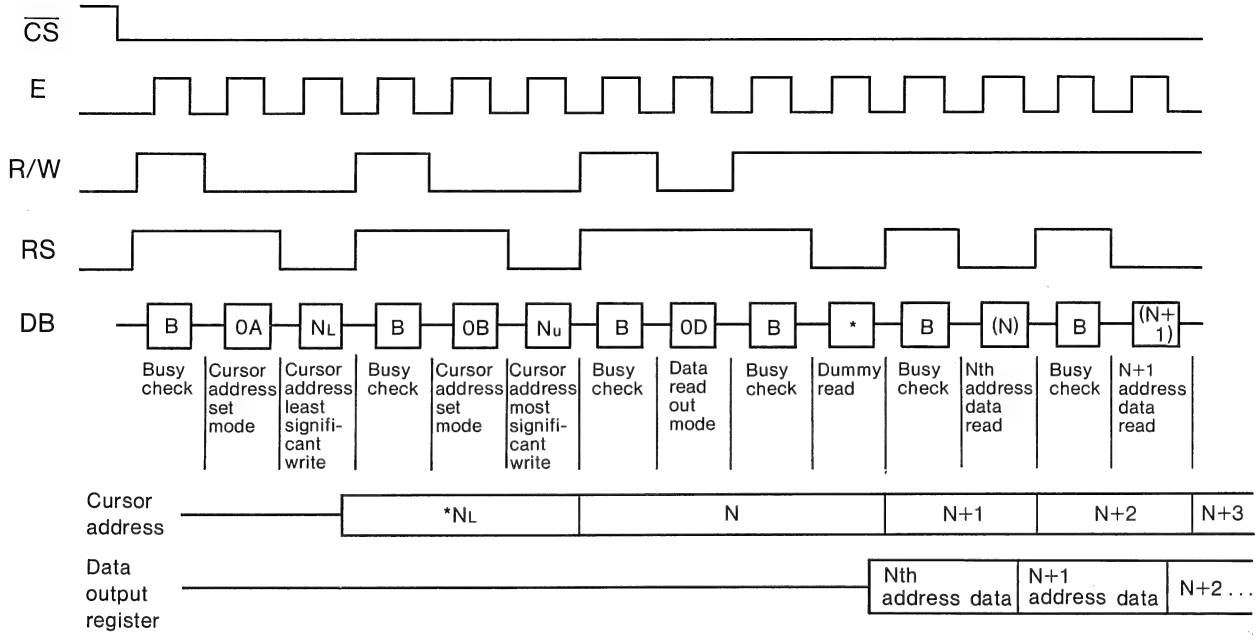
Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data character code)							LSB

By writing in code $'0C' in the instruction register and writing an 8-bit data with RS = 0, the data is written into the RAM address specified by the cursor address counter as a character data or a character code. After the data is written, the cursor address counter is incremented by one.

11. Display Data Read

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data character code)							LSB

By writing $'0D' in the instruction register with RS = 0, data in the RAM may be read by entering the read out mode. The read out procedure is shown below:



With this instruction, the contents of the data output register are output to OB_{0-7}, and the data in the RAM specified by the cursor address is then transferred to the data output register. The cursor address is then incremented by one. Therefore, after setting the cursor address, the correct data is not output for the first read operation. The correct value is output during the second read operation. Therefore, when reading a data after setting a cursor address, a dummy read operation must be performed once.

12. Bit Clear

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	1	1	1	1
Bit clear	0	0	0	0	0	0	0	(N_B-1) binary		

13. Bit Set

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction register	0	1	0	0	0	0	1	1	0	1
Bit set	0	0	0	0	0	0	0	(N_B-1) binary		

The bit clear and bit set instructions set one bit of the display data RAM byte to 0 or 1. The bit clear instruction will set the bit specified by N_B to 0, and the bit set command will set the bit to 1. The RAM address is specified by the cursor address, and the cursor address is automatically incremented by one when the instruction is executed. N_B must be a value from 1 to 8. $N_B = 1$ indicates the least significant bit, and $N_B = 8$ indicates the most significant bit.

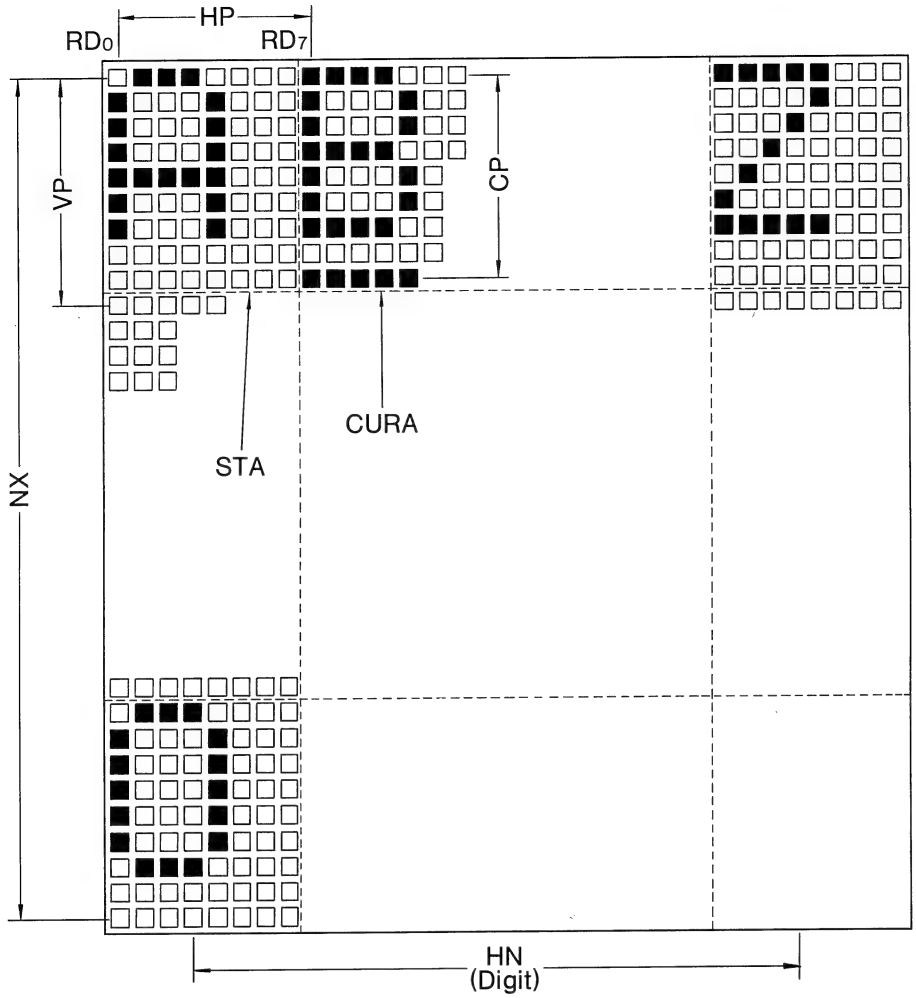
14. BUSY Flag Read

Register	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Busy flag	1	0	1/0	*						

When read-out mode is selected with RS = 0, a busy flag is output to DB_7. The busy flag is set to 1 while any of the instructions a through m are being executed. The flag is set to 0 when the instruction is executed, and the next instruction can then be accepted.

A new instruction is not accepted if the busy flag is 1. The busy flag must be checked to see that it is 0 before writing in a new instruction or data. The busy flag status is not changed by writing (RS = 1) data in the instruction register. Therefore, it is not necessary to check the busy flag immediately after writing to the instruction register.

The instruction register need not be specified for reading the busy flag.



Symbol	Name	Meaning	Value
H_p	Horizontal character pitch	Character pitch in the horizontal direction	6–8 dots
H_N	Horizontal character count	Number of characters (digit count) per horizontal line, or (in the graphics mode) the number of words per line	2–128 digits
V_p	Vertical character pitch	Character pitch in the vertical-direction	1–16 dots
C_p	Cursor position	Line number where the cursor is displayed	Line 1–16
N_x	Vertical-direction line count	Display duty	1–128 lines

Note: Let m be the number of dots in the vertical direction, and n the number of dots in the horizontal direction. Then:

$1/m = 1/N_X$ = Display duty
$n = H_P \times H_N$
m/VP = number of lines displayed
$C_p \leqq V_p$

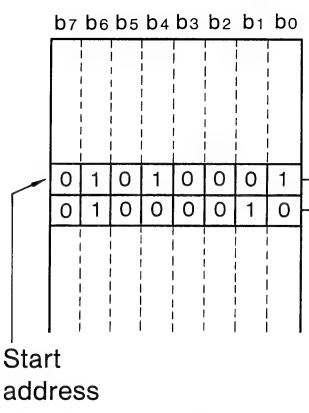
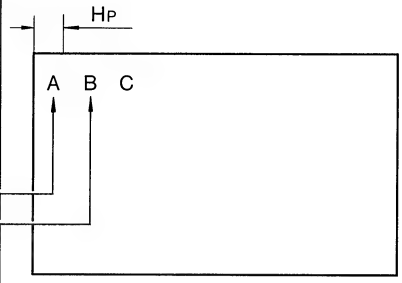
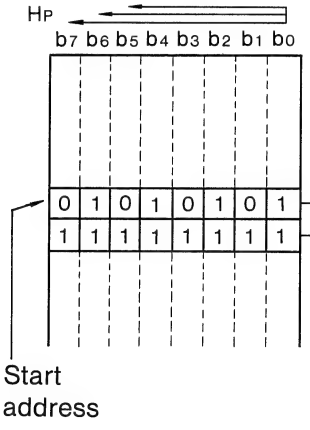
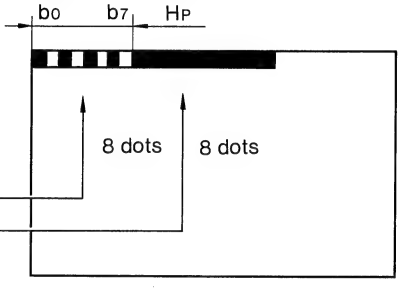
Display mode	Display mode from MPU	RAM	Liquid crystal panel
Character display	Character code (8 bits)		 HP: 6, 7 or 8 dots
Graphics	Display pattern (8 bits)		 HP: 8 dots

Table C-8. Character Display and Graphics Mode

(5) Timing Chart

(a) CPU Interface

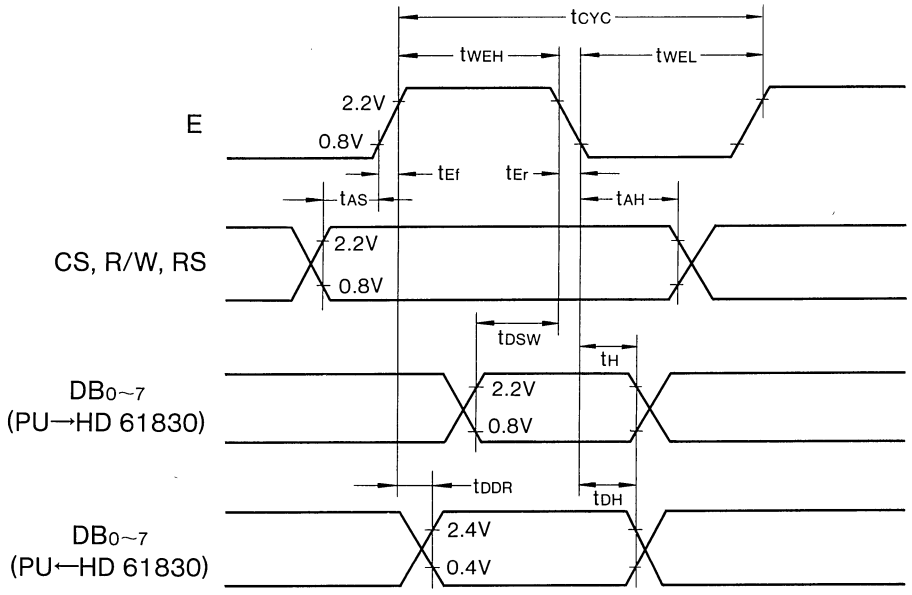


Figure C-64. HD61830 CPU Interface Timing Chart

(b) External RAM and ROM Interface

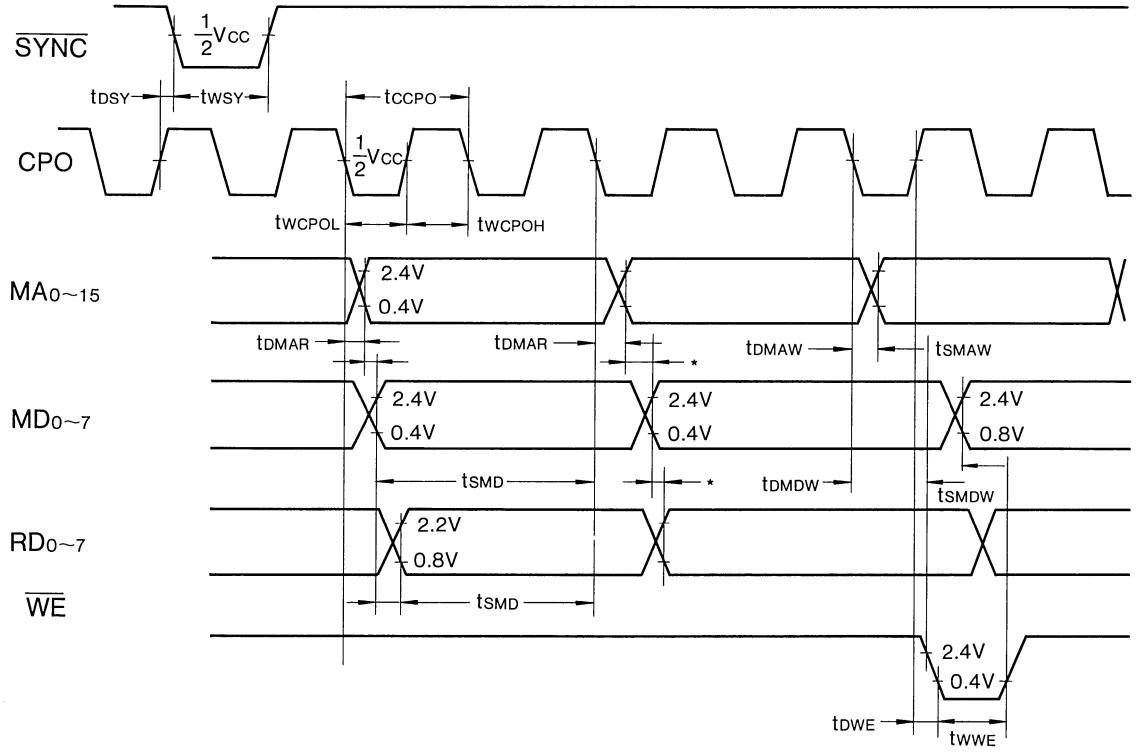


Figure C-65. HD61830 External RAM and ROM Interface Timing Chart

(c) Data Transmission to Driver LSI

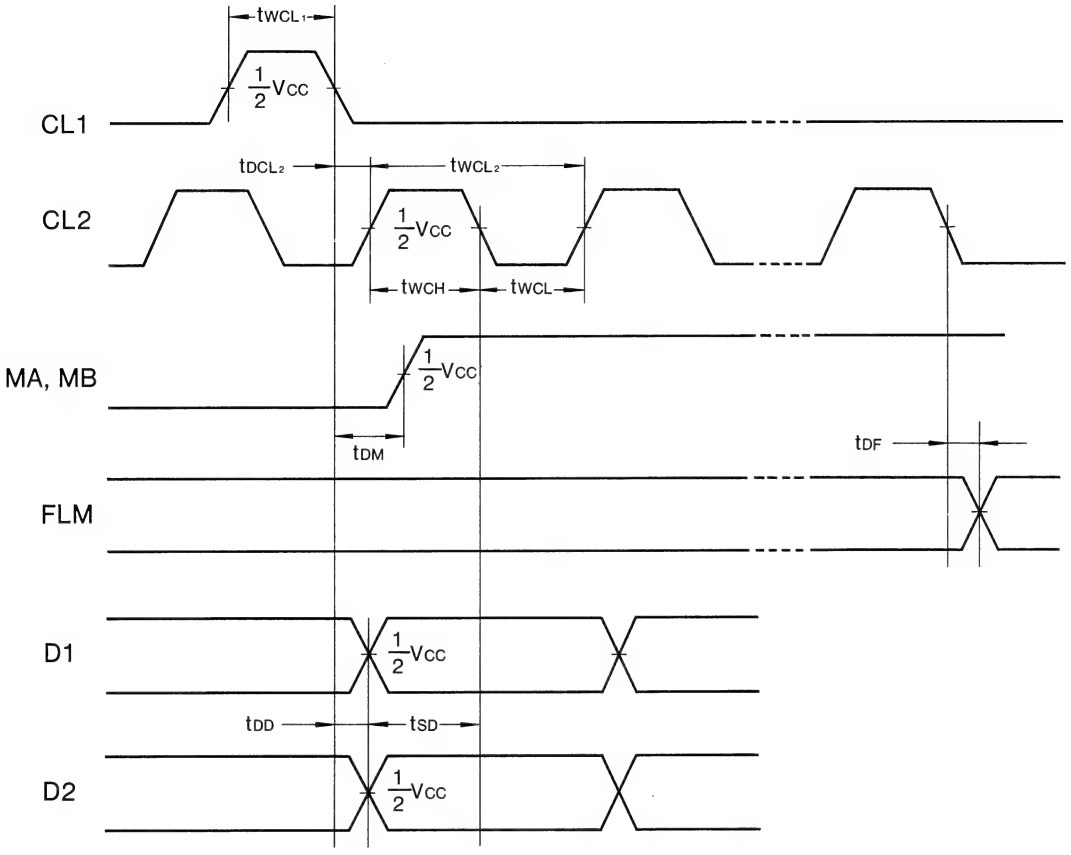


Figure C-66. HD61830 and LCD Unit Interface Timing Chart

APPENDIX D

APPENDIX D – INSTALLATION OF OPTIONAL RAM AND ROM

D.1 Installation of Optional RAM Card

(1) Remove the top cover assembly (see section 3).

(2) Connect the optional RAM card to the white CN1 or CN2 connector.

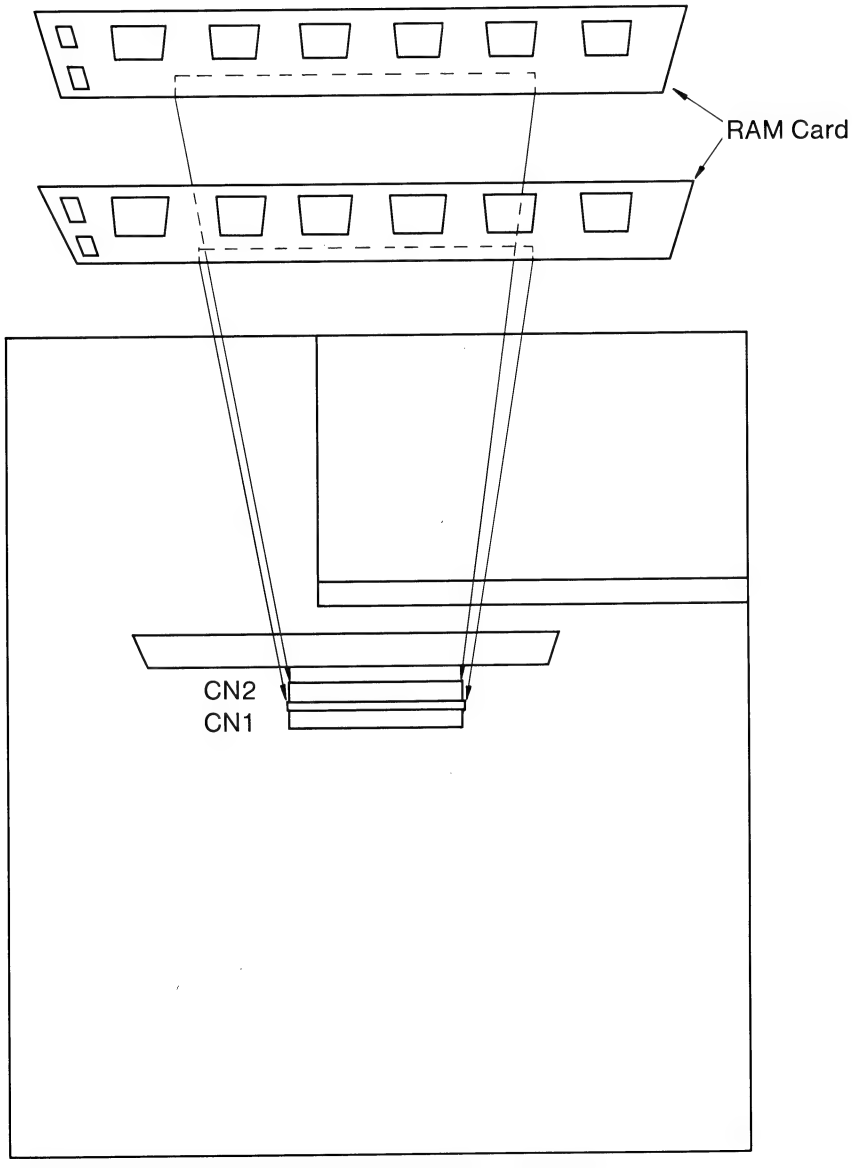


Figure D-1. Optional RAM Installation

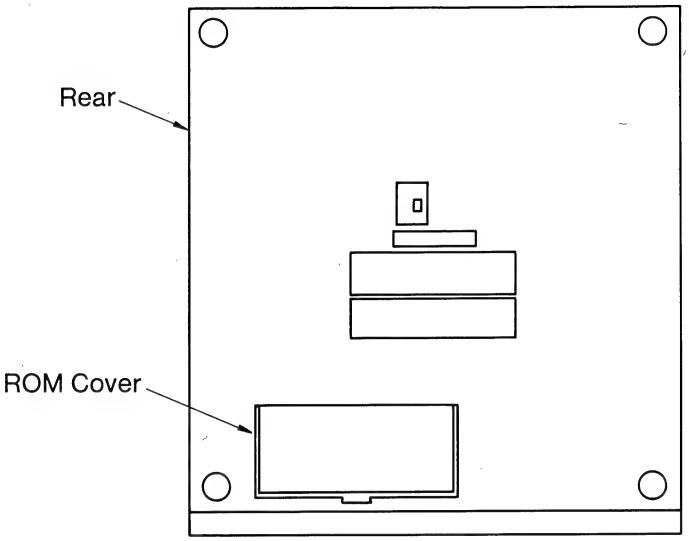
Note: Turn off the Memory Power Switch when you install or remove the RAM Card.

D.2 Installation of Optional ROM Chip

(1) Remove the ROM cover from the rear of the unit using a slot-head screwdriver.

(2) Install the optional ROM chip.

1)



2)

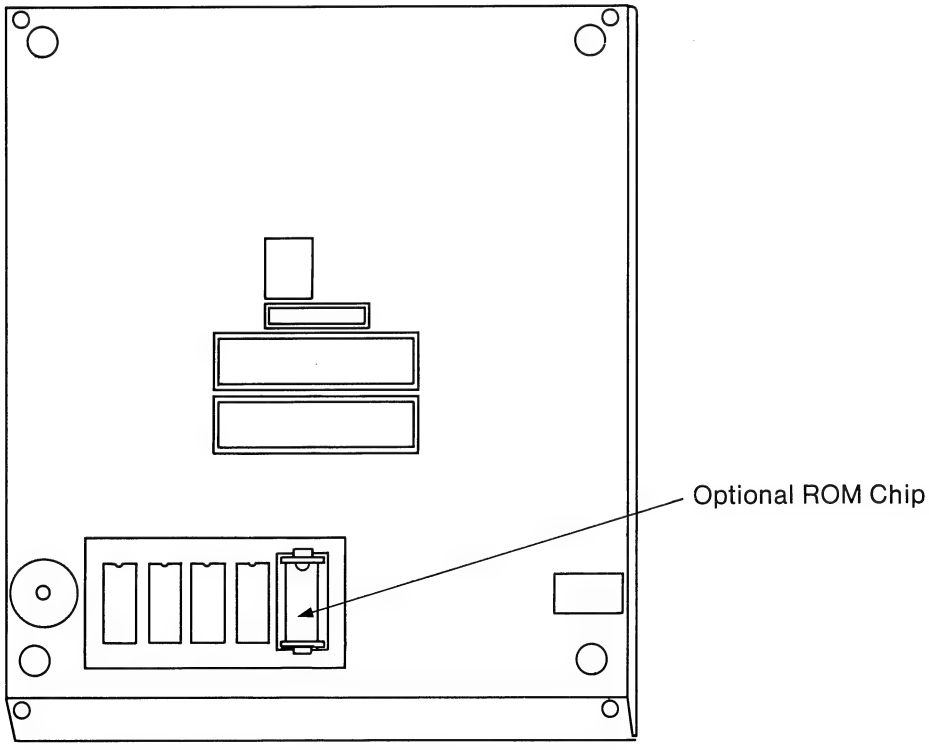


Figure D-2. Optional ROM Installation

Note: Do not touch the other ROM chips.

RADIO SHACK, A DIVISION OF TANDY CORPORATION

U.S.A.: FORT WORTH, TEXAS 76102
CANADA: BARRIE, ONTARIO L4M 4W5

TANDY CORPORATION

AUSTRALIA	BELGIUM	U.K.
91 KURRAJONG AVENUE	RUE DES PIEDS D'ALOUETTE, 39	BILSTON ROAD, WEDNESBURY
MOUNT DRUITT N.S.W. 2770	5140 NANNINE (NAMUR)	WEST MIDLANDS WS10 7JN

8A5

Printed in Japa