

Tandy 3000

Technical Reference Manual

Tandy 3000
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DETAIL DESIGN SPECIFICATION

TANDY MODEL 3000 COMPUTER

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1.0 SCOPE

The purpose of this specification is to serve as the detailed specification guide for the TANDY Model 3000 computer. The system is composed of four buses; 80286 LOCAL BUS, LOCAL MEMORY BUS, SYSTEM I/O (AT) BUS, and the BUFFERED PERIPHERAL BUS.

Each bus has timing associated with the devices being accessed. For instance, the 80286 LOCAL BUS typically operates with one wait state, its bandwidth is 90 % utilized by the CPU, operates asynchronous to the math coprocessor (optional), and operates synchronous to the other buses.

The LOCAL MEMORY BUS consists of two banks of DRAMS. This bus can support to 1MB of memory using 256K x 1 DRAMS. At this time the basic configuration of this bus will consist of one bank of 256K x 1 DRAMS and be upgradable to only 640KB by populating the second bank with 64K x 1 DRAMS. The bandwidth of this bus is 5.3MB/sec, and requires the use of DRAMS with a maximum access time of 150ns.

The SYSTEM I/O (AT) BUS provides system expansion through 10 I/O peripheral card slots (2 PC compatible and 8 AT compatible) internal to the cabinet. The bandwidth of this bus is the same as the 80286 LOCAL BUS or the MEMORY BUS, and incorporates variable wait states to service some option cards.

The BUFFERED PERIPHERAL BUS is an extension of the SYSTEM I/O (AT) BUS, but supports DMA operations, provides counters and timers, interrupt requests, I/O decoding, keyboard logic, speaker logic, and a real time clock with RAM.

1.1 PRODUCT BRIEF

TANDY DESK TOP PC/AT PRODUCT BRIEF

FEATURES:

- o Low Entry Cost Advanced PC
- o 8MHZ 16-Bit 80286 with on Chip Memory Management and Protection
- o Standard 512KB Memory
 - Expandable to 640KB on Board
 - Bus Addressing Supports to 16MB Memory
- o Standard High Capacity 5-1/4" Slim Line Floppy Disk Drive
 - Selectable 1.2MB or 720KB Formats Allows Compatibility with IBM-AT or Tandy 2000
 - Channel for Additional Internal Floppy Disk Drive for either a 360KB, 720KB, or 1.2MB Format
- o Channel for optional Hard Disk Drive
- o Ten IBM-AT Compatible Slots for Standard Peripherals and Additional Memory expansion (8-Slots Open)
- o True Software Compatibility with the IBM-AT in the Single User MS-DOS Mode or Multi-User Protected Mode
- o Standard Real Time Clock with CMOS Ram and Battery Backup
- o Standard Serial/Parallel Adapter (Uses one I/O Slot)
- o Standard PC/AT Compatible Keyboard
- o Support for Optional Math Co-processor

PHYSICAL DIMENSIONS

Height 6.5 inches
Width 19.0 inches
Depth 18.0 inches

HEAT OUTPUT

850 BTU/hr.

NOISE LEVEL

42 decibels

OPERATING TEMPERATURE

55 - 85 degrees Fahrenheit
13 - 29 degrees Celsius

2.0 FUNCTIONAL DESCRIPTION

2.1 80286 Local Bus

This bus consists of the 80286 CPU and the 80287 Co-Processor. There are no buffers between the two. This bus connects memory and I/O resources to the 80286 processor, using 24 address lines, 16 data lines, and a number of status and control signals. All resources other than the 80287 are buffered to this bus.

2.1.1 82284 Clock Generator

This 18-pin dip generates the clock, ready, and reset signals required for the 80286 processors and support components.

2.1.2 82288 Bus Controller

This 20-pin dip is used to provide address latch control, and command outputs based on the 80286 status lines.

2.1.3 80287 Numeric Processor Extension (Optional)

This 40-pin dip works in parallel with the 80286 CPU. This parallel operation decreases operating time by allowing the coprocessor to execute mathematical calculations independent of the CPU. This device performs high-speed arithmetic, logarithmic functions, and trigonometric operations with seven numeric data types divided into the following three classes:

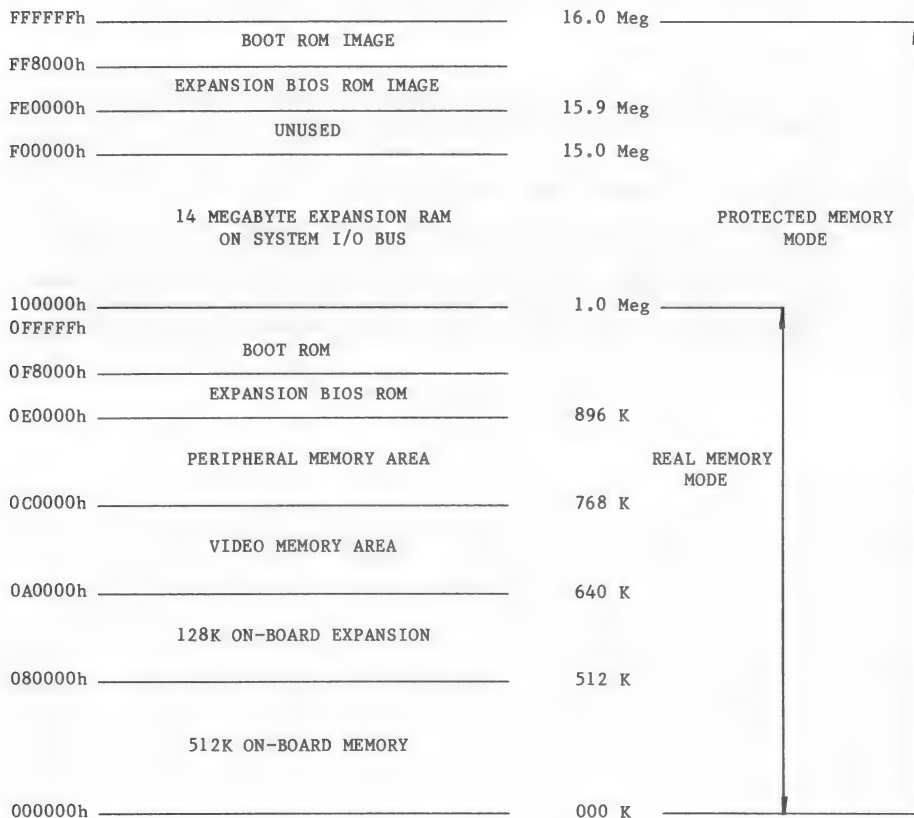
- * Binary integers (three types)
- * Decimal integers (one type)
- * Real numbers (three types)

2.2 System Memory

2.2.1 Memory Configuration

The real address mode is defaulted to at power up, and has a maximum directly addressable range of 1 megabyte.

The protected address mode of the CPU has a maximum directly accessible range of 16 megabytes, and a virtual addressable range of 4 gigabytes. In this mode, memory configuration below the 1 megabyte region remains mapped the same as in real address mode. The on-board ROM locations 0E0000H thru 0FFFFFH are duplicated at addresses FE0000H thru FFFFFFH.



2.2.2 ROM Subsystem

The on-board ROM subsystem consists of four ROM/EPROM modules; the code for odd and even addresses reside in separate modules, and is not parity checked. Each module can support to 32KB of data for a total of 128KB. The BIOS (Basic Input Output System) resides in 64KB allowing a 64KB expansion range. The ROM is assigned at the top of the first and last 1 megabyte address space (0E0000 and FE0000 HEX)

2.2.3 RAM Subsystem

The system RAM consists of two divisions; the on board system memory (Standard 512 kilobytes of DRAM upgradable to 640 kilobytes), and the SYSTEM I/O (AT) BUS memory options.

Memory refresh requests one memory cycle every 15 microseconds through channel 1 of the counter/timer subsystem. The RAM initialization program initializes channel 1 of the counter/timer subsystem to the rate generation mode, with a period of 15 microseconds, and then performs a memory read operation to any memory location. The memory must be accessed or refreshed eight times before it can be used.

2.2.4 Parity Control

All dynamic memory utilizes odd parity. Parity can be disabled by the CPU. There is one parity bit per byte of DRAM - for both upper and lower banks of memory.

2.3 System I/O (AT) Bus

This bus is a 100% compatible IBM-AT bus. It has an open-bus structure which will allow multiple microprocessors to share the systems resources. A total of ten expansion cards are supported. Although all of these slots can support some PC compatible boards, two are dedicated for this use. Some of the functions supported by this bus are:

- * 24-bit memory addressing.
- * 8 or 16 bit data accesses.
- * I/O addressing range of 100 to 3FF hex.
- * Interrupts and DMA support.
- * I/O wait state generation.
- * Refresh of system memory.

2.3.1 Floppy Disk Controller

This controller resides on the I/O (AT) bus and is an integral part of the Fixed Disk controller. It supports two 5-1/4" drives (one standard) through an internal, daisy-chained, flat cable. The controller will support 160K, 320K, and 1.2M byte formats. The interface is buffered on the I/O bus and uses the system board's DMA for block data transfers. An interrupt is used to indicate when an operation is complete or that a status condition requires the CPU's attention.

2.3.2 Fixed Disk Controller

This controller is integrated with the Floppy Disk controller. It is 100% PC AT compatible. The controller is based on Western Digital's WD1010 and on a self-adjusting Data Separator WD10C20. The controller board supports up to 16 read/write heads per drive, 1024 cylinders per drive, and two Winchester disk drives.

2.3.3 Memory Expansion Board

These optional boards may be configured as 512KB, 1MB, 1.5MB or 2MB. All Memory Expansion boards must be configured on contiguous boundaries. These boards have a 16-bit data path, parity checking, and an addressable range of 16MB. Refresh of the DRAMs is accomplished by the main PCB. Memory limitation is determined by the available option slots.

2.3.4 Serial/Parallel I/O

This standard Serial/Parallel card is 100% compatible with the IBM-AT.

SERIAL PORT

The serial portion of this board supports the EIA RS-232C interface standard through a 9-pin D-shell connector (a 9-pin to 25-pin adapter cable is used to complete the EIA RS-232C interface) located on the rear of the board for external chassis access (the serial port is fully programmable, and supports asynchronous communications).

The onboard universal asynchronous receiver transmitter adds and removes start, parity, and stop bits (five, six, seven, and eight bit characters with 1, 1.5, or 2 stop bits are supported). The onboard programmable baud-rate generator supports operation from 50 to 9600 baud. A prioritized interrupt scheme controls transmit, receive, error, line status, and data set interrupts.

Serial Port Controller (NS16450) Specifications

Clear-to-Send (CTS): signal is bit 4 of the modem status register - bit 0 (DCTS) of the modem status register indicates a state change of CTS. If the modem status interrupt is enabled, and the CTS changes state, an interrupt is generated.

Data Set Ready (DSR): signal is bit 5 of the modem status register and indicates the modem or data set is ready to establish communications link and transfer data with the controller - bit 1 (DDSR) of the modem status register indicates a state change of DSR. If the modem status interrupt is enabled, and the DSR changes state, an interrupt is generated.

2.3.5 Monochrome Display Adapter

The controller used for this option is the TANDY Catalog # 25-3040 Monochrome Display Adapter. This adapter uses the TANDY VM-3 Monochrome Monitor catalog # 25-3010. This card is 100% compatible with this or the IBM AT product.

2.3.6 Color/Graphics Monitor Adapter

The controller used for the 320 x 200 resolution option is the TANDY Catalog # 25-3043 Graphics Display Adapter. This adapter uses the TANDY CM-2 Color Monitor catalog # 26-3212 or the TANDY VM-3 Monochrome Monitor catalog # 25-3010. This card is 100% compatible with this or the IBM AT product.

The controller used for the 640 x 200 resolution option is the TANDY Catalog # 25-3044 Graphics Master Adapter. This adapter uses the TANDY CM-2 Color Monitor catalog # 26-3212.

This card is 100% hardware compatible with this or the IBM AT product. It is not software compatible with any IBM high resolution graphics cards.

2.4 Buffered Peripheral Bus

2.4.1 System Interrupts

The 80286 microprocessor NMI (non maskable interrupt) and two 8259A interrupt controller chips together provide the system with a total of 16 levels of interrupts. Note that any or all interrupt levels may be masked, including the CPU's NMI. The following table shows the interrupt level assignments in decreasing order of priority (note that interrupts 8 thru 15 are accessed thru interrupt 2).

<u>INTERRUPT</u>	<u>DEVICE</u>	<u>FUNCTION</u>
NMI	CPU's	Parity of I/O Channel Check
IRQ0	Controller 1	Timer Output 0
IRQ1	Controller 1	Keyboard (Output Buffer Full)
IRQ2	Controller 1	IRQ8 thru IRQ15
IRQ3	Controller 1	Serial Port 2
IRQ4	Controller 1	Serial Port 1
IRQ5	Controller 1	Parallel Port 2
IRQ6	Controller 1	Diskette Controller
IRQ7	Controller 1	Parallel Port 1
IRQ8	Controller 2	Real Time Clock Interrupt
IRQ9	Controller 2	Software Redirected to INT 0AH (IRQ2)
IRQ10	Controller 2	Reserved
IRQ11	Controller 2	Reserved
IRQ12	Controller 2	Reserved
IRQ13	Controller 2	Coprocessor
IRQ14	Controller 2	Fixed Disk Controller
IRQ15	Controller 2	Reserved

2.4.2 Direct Memory Access

The system supports 7 DMA channels, using two 8237A-5 DMA controller chips (each chip has four channels, but channel 4 of controller 2 is used to cascade the two DMA chips).

DMA controller 1 contains channels 0 thru 3, and supports 8 bit data transfers between 8 bit I/O adapters and 8 or 16 bit system memory (each channel can transfer data throughout the 16 megabyte system address space in 64 kilobyte blocks).

DMA controller 2 contains channels 5 thru 7, and supports 16 bit data transfers between 16 bit I/O adapters and 16 bit system memory (each channel can transfer data throughout the 16 megabyte system address space in 128 kilobyte blocks, but not on odd byte boundaries).

HEX ADDRESS	COMMAND CODES	DMA CONTROLLER
000	CH0 base and current address	1
002	CH0 base and current word count	1
004	CH1 base and current address	1
006	CH1 base and current word count	1
008	CH2 base and current address	1
00A	CH2 base and current word count	1
00C	CH3 base and current address	1
00E	CH3 base and current word count	1
010	Read Status Reg/Write Command Reg	1
012	Write Request Register	1
014	Write Single Mask Register Bit	1
016	Write Mode Register	1
018	Clear Byte Pointer Flip-Flop	1
01A	Read Temporary Reg/Write Master Clear	1
01C	Clear Mask Register	1
01E	Write All Mask Register	1
0C0	CH4 base and current address	2
0C2	CH4 base and current word count	2
0C4	CH5 base and current address	2
0C6	CH5 base and current word count	2
0C8	CH6 base and current address	2
0CA	CH6 base and current word count	2
0CC	CH7 base and current address	2
0CE	CH7 base and current word count	2
0D0	Read Status Reg/Write Command Reg	2
0D2	Write Request Register	2
0D4	Write Single Mask Register Bit	2
0D6	Write Mode Register	2
0D8	Clear Byte Pointer Flip-Flop	2
0DA	Read Temporary Reg/Write Master Clear	2
0DC	Clear Mask Register	2
0DE	Write All Mask Register	2

2.4.2 Direct Memory Access -- CONTINUED

Addresses for all DMA channels do not increase or decrease through page boundaries (64 kilobyte for channels 0 thru 3 and 128 kilobyte for channel 5 thru 7). Address generation for DMA channels are as follows in the next table:

<u>PAGE REGISTER</u>	<u>I/O HEX ADDRESS</u>	<u>PAGE ADDRESS</u>	<u>DMA OUTPUT ADDRESS</u>
DMA CHANNEL 0	0087	A23<---->A16	A15<---->A0
DMA CHANNEL 1	0083	A23<---->A16	A15<---->A0
DMA CHANNEL 2	0081	A23<---->A16	A15<---->A0
DMA CHANNEL 3	0082	A23<---->A16	A15<---->A0
DMA CHANNEL 5	008B	A23<---->A17	A16<---->A1
DMA CHANNEL 6	0089	A23<---->A17	A16<---->A1
DMA CHANNEL 7	008A	A23<---->A17	A16<---->A1
REFRESH	008F		

NOTE: For channels 0 thru 3 -- byte high enable (BHE) = A0 inverted
For channels 5 thru 7 -- BHE and A0 are forced to a logic 0.

2.4.3 I/O Decode

The following table is a condensed map of the I/O address map (each address range is expanded within the sections listed under the heading 'SEE SECTION').

<u>HEX RANGE</u>	<u>DEVICE</u>	<u>SEE SECTION</u>
000 - 01F	DMA controller 1 (8237A-5)	2.4.2
020 - 03F	Interrupt controller 1, Master (8259A)	2.4.1
040 - 05F	Timer (8254.2)	2.4.5
060 - 06F	(keyboard) 8042	2.4.7
070 - 07F	Real time clock/NMI mask/(MC146818)	2.4.6
080 - 09F	DMA page register (74LS612)	2.4.4
0A0 - 0BF	Interrupt controller 2 (8259A)	2.4.1
0C0 - 0DF	DMA controller 2 (8237A-5)	2.4.2
0E0 - 0EF	UNDEFINED	
0F0	Clear Math Coprocessor Busy	2.1.3
0F1	Reset Math Coprocessor	2.1.3
0F8 - 0FF	Math Coprocessor	2.1.3
100 - 1EF	UNDEFINED	
1F0 - 1F8	Fixed Disk	2.3.1
1F9 - 1FF	UNDEFINED	
200 - 207	Game I/O	2.3.2
278 - 27F	Parallel printer port 2	2.3.3
280 - 2F7	UNDEFINED	
2F8 - 2FF	Serial Port 2	2.3.3
300 - 31F	Prototype card	2.3.6
320 - 35F	UNDEFINED	
360 - 36F	Reserved	
370 - 377	UNDEFINED	
378 - 37F	Parallel printer port 1	2.3.3
380 - 38F	SDLC, bisynchronous 2	2.3.3
390 - 39F	UNDEFINED	
3A0 - 3AF	Bisynchronous 1	2.3.3
3B0 - 3BF	Monochrome Display/Printer Adapter	2.3.4
3C0 - 3CF	Reserved	
3D0 - 3DF	Color/Graphics Monitor Adapter	2.3.5
3E0 - 3EF	UNDEFINED	
3F0 - 3F7	Diskette controller	2.3.1
3F8 - 3FF	Serial port 1	2.3.3

2.4.4 DMA Paged Memory Mapper

The memory mapper is used to expand the DMA's memory address capability by eight bits. Four bits of the memory address are used to select one of 16 map registers that contain 8 bits each. These 8 bits are presented to the system memory address bus through the map output buffers along with the user memory address bits from the DMA. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus.

The memory mapper has four modes of operation (read, write, map and pass). Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3), under control of R/W* whenever chip select (CS*) is low.

2.4.5 System Timers

The system has an INTEL 8254-2 counter/timer chip (three programmable counter/timers in one chip). This chip is a programmable interval counter/timer that system programs treat as an arrangement of four external I/O ports; three ports are treated as counters, and the fourth is a control register for mode programming. The following table describes each channel control and output as follows (NOTE: channel 1 is programmed as a rate generator to produce a 15 microsecond period signal):

CHANNEL	SIGNAL NAME	DESCRIPTION
0		SYSTEM TIMER
0	GATE 0	TIED ON
0	CLK IN 0	1.190 MHz OSC
0	CLK OUT 0	8259A IRQ0
1		REFRESH REQUEST GENERATOR
1	GATE 1	TIED ON
1	CLK IN 1	1.190 MHz OSC
1	CLK OUT 1	REQUEST REFRESH CYCLE
2		TONE GENERATION FOR SPEAKER
2	GATE 2	CONTROLLED BY BIT 0 OF PORT 61H PPI BIT
2	CLK IN 2	1.190 MHz OSC
2	CLK OUT 2	USED TO DRIVE THE SPEAKER

2.4.6 Real Time Clock

The MC146818 Real Time Clock combines four features on the chip: a complete time of day clock with alarm (not used), a one hundred year calendar, a programmable periodic interrupt and square wave generator, and 64 bytes of general purpose low power static RAM (this RAM is battery backed up, and 50 bytes of this RAM are available for system configuration programmable uses). The setup program initializes registers A,B,C, and D, when the time and date are set. Interrupt 1A is the BIOS interface to read/set the time and date; it initializes the status bytes the same as the Setup program.

<u>HEX ADDRESS</u>	<u>DESCRIPTION</u>
00	* Seconds
01	* Seconds Alarm
02	* Minutes
03	* Minutes Alarm
04	* Hours
05	* Hours Alarm
06	* Day of the Week
07	* Date of the Month
08	* Month
09	* Year
0A	* Register A
0B	* Register B
0C	* Register C
0D	* Register D
0E	* Diagnostic status byte
0F	* Shutdown status byte
10	Diskette drive type byte - drives A and B
11	Reserved
12	Fixed disk type byte - drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2 - byte CMOS checksum
30	* Low expansion memory byte
31	* High expansion memory byte
32	* Date century byte
33	* Information flags (set during power on)
34-3F	Reserved

* These bytes are excluded from the checksum calculation and are not part of the configuration record.

2.4.6 Real Time Clock -- CONTINUED

STATUS REGISTER A

BIT 7 - a 1 indicates the time update cycle is in progress, and a 0 indicates the current date and time is available to read.

BITS 6-4 - these bits are used to select the frequency divider stage based on the time base used; 000 selects 4.194304 megahertz, 001 selects 1.048576 megahertz, default 010 selects 32.768 kilohertz time base, 110 and 111 select any frequency, and other combinations are used for test purposes.

BITS 3-0 - these bits are used to select the frequency divider output as shown in the next table; default 0110 selects 1.024 kilohertz square wave output frequency and a 976.562 microsecond periodic interrupt rate (PIR) for a 32.768 kilohertz time base.

BITS 3-0	TIME BASE CODE 000 OR 001		TIME BASE CODE 010 (DEFAULT)	
	PIR	OUTPUT FREQ	PIR	OUTPUT FREQ
0000	none	none	none	none
0001	30.517 us	32.768 KHz	3,906.250 us	256.000 Hz
0010	61.035 us	16.384 KHz	7,812.500 us	128.000 Hz
0011	122.070 us	8.192 KHz	122.070 us	8.192 KHz
0100	244.141 us	4.096 KHz	244.141 us	4.096 KHz
0101	488.281 us	2.048 KHz	488.281 us	2.048 KHz
0110	976.562 us	1.024 KHz	976.562 us	1.024 KHz
0111	1,953.125 us	512.000 Hz	1,953.125 us	512.000 Hz
1000	3,906.250 us	256.000 Hz	3,906.250 us	256.000 Hz
1001	7,812.500 us	128.000 Hz	7,812.500 us	128.000 Hz
1010	15.625 ms	64.000 Hz	15.625 ms	64.000 Hz
1011	31.250 ms	32.000 Hz	31.250 ms	32.000 Hz
1100	62.500 ms	16.000 Hz	62.500 ms	16.000 Hz
1101	125.000 ms	8.000 Hz	125.000 ms	8.000 Hz
1110	250.000 ms	4.000 Hz	250.000 ms	4.000 Hz
1111	500.000 ms	2.000 Hz	500.000 ms	2.000 Hz

2.4.6 Real Time Clock -- CONTINUED

STATUS REGISTER B

BIT 7 - a 1 aborts any update cycle in progress and the program can initialize the 14 time bytes without any further updates occurring until a 0 is written to this bit (a 0 updates the cycle normally by advancing the counts at one per second).

BIT 6 - is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in REGISTER A; 1 enables the interrupt, and 0 (default) disables the interrupt.

BIT 5 - a 1 enables the alarm interrupt, and a 0 disables it; system default is 0.

BIT 4 - a 1 enables the update ended interrupt, and a 0 disables it; system default is 0.

BIT 3 - a 1 enables the square wave frequency as set by the rate selection bits in REGISTER A, and a 0 disables it; system default is 0.

BIT 2 - indicated whether the time and date calendar updates are to use binary or binary coded decimal formats; 1 indicated binary, and 0 (default) indicates binary coded decimal.

BIT 1 - establishes whether the hours byte is in the 24 hour or 12 hour mode; 1 indicates the 24 hour mode, and 0 indicates the 12 hour mode (default is 0).

BIT 0 - a 1 enables daylight savings, and a 0 disables daylight savings (standard time); system default is 0.

STATUS REGISTER C

BITS 7-4 - are flag bits (IRQF, PF, AF, UF in descending order) which are read only, but are updated when bits 6-4 of REGISTER B are enabled.

BITS 3-0 - are RESERVED.

STATUS REGISTER D

BIT 7 - is a read only bit, which is updated when the real time clock has lost power; 1 indicates power on the real time clock, and 0 indicates that the real time clock has lost power.

BITS 6-0 - are RESERVED.

2.4.6 Real Time Clock -- CONTINUED

DIAGNOSTIC STATUS BYTE

BIT 7 - indicates loss of power on the real time clock when 1, and a 0 indicates that the chip has not lost power.

BIT 6 - is a checksum status indicator; 0 indicates that the checksum is good, and 1 indicates it is bad.

BIT 5 - is a check, at power on time, of the equipment byte of the configuration record; 0 indicates that the configuration information is valid, and 1 indicates it is invalid. Note: power on checks require at least one diskette drive to be installed (bit 0 of the equipment byte set to 1), and the actual display hardware in the system (primary display adapter setting in the configuration record matches the system board's display switch setting).

BIT 4 - a 1 indicates, that the power on check determined the memory size is different from the configuration record, and a 0 indicates a memory size match.

BIT 3 - a 0 indicates that the adapter and drive are functioning properly and the system can attempt a boot up, however, a 1 indicates that the adapter and/or drive C failed initialization, preventing the system from attempting a boot up.

BIT 2 - is a post validity check; 0 indicates that the time is valid, and 1 indicates that the time is invalid.

BITS 1 and 0 - are RESERVED.

SHUTDOWN STATUS BYTE

The bits in this byte are defined by the power on diagnostics in the BIOS Listing.

DISKETTE DRIVE TYPE BYTE

BITS 7-4 - indicate type of first diskette drive installed; 0000 = no drive is present, 0001 = double sided diskette drive (48 TPI), 0010 = high capacity diskette drive (96 TPI), and 0011 thru 1111 are reserved.

BITS 3-0 - indicate type of second diskette drive installed; 0000 = no drive is present, 0001 = double sided diskette drive (48 TPI), 0010 = high capacity diskette drive (96 TPI), and 0011 thru 1111 are reserved.

2.4.6 Real Time Clock -- CONTINUED

FIXED DISK TYPE BYTE

BITS 7-4 - indicate type of first fixed disk drive (drive C) installed; 0000 = no drive is present, 0001 thru 1111 = define type 1 thru type 15 (15 is reserved and set to 0) of fixed disk drive.

BITS 3-0 - indicate type of second fixed disk drive (drive D) installed; 0000 = no drive is present, 0001 thru 1111 = define type 1 thru type 15 (15 is reserved and set to 0) of fixed disk drive.

<u>TYPE</u>	<u>CYLINDERS</u>	<u>HEADS</u>	<u>WRITE PRE-COMP</u>	<u>LANDING ZONE</u>
1	306	4	128	305
2	615	4	300	615
3	615	6	300	615
4	940	8	512	940
5	940	6	512	940
6	615	4	NONE	615
7	462	8	256	511
8	733	5	NONE	733
9	900	15	NONE	901
10	820	3	NONE	820
11	855	5	NONE	855
12	855	7	NONE	855
13	306	8	128	319
14	733	7	NONE	733
15	---	-	---	---

EQUIPMENT BYTE

BITS 7-6 - indicate the number of diskette drives installed; 00 = 1 drive, 01 = 2 drives, and 10 and 11 are reserved.

BITS 5-4 - indicate primary display; 00 = reserved, 01 = primary display is attached to the color/graphics monitor adapter in the 40 column mode, 10 = primary display is attached to the color/graphics monitor adapter in the 80 column mode, and 11 = primary display is attached to the monochrome display and printer adapter.

BITS 3-2 - not used.

BIT 1 - indicates if the math coprocessor is present; 0 = not installed, and 1 = installed.

BIT 0 - indicates if diskette drives are installed if set.

2.4.6 Real Time Clock -- CONTINUED

LOW AND HIGH BASE MEMORY BYTES (15H and 16H)

BITS 7-0 - of 15H indicates low byte base size, and 16H indicates high byte base size; valid sizes 0100H = 256 kilobytes of system RAM, 0200H = 512 kilobytes of system RAM, and 0280H = 640 kilobytes 512 kilobytes if system RAM and the IBM-AT 128 kilobyte memory expansion option.

LOW AND HIGH MEMORY EXPANSION BYTES (17H and 18H)

BITS 7-0 - of 17H indicates low byte base size, and 18H indicates high byte base size; valid sizes 0200H = 512 kilobytes I/O adapter RAM, 0400H = 1024 kilobytes I/O adapter RAM (2 adapter cards), and 0600H to 3C00H = 1536 kilobytes I/O adapter (3 adapters) to 15360 kilobytes I/O adapter (15 megabytes maximum).

CHECKSUM BYTES (2EH and 2FH)

BITS 7-0 - of 2EH indicates low byte of CHECKSUM, and 2FH indicates high byte of CHECKSUM.

LOW AND HIGH EXPANSION MEMORY BYTES (30H and 31H)

BITS 7-0 - of 30H indicates low byte expansion size, and 31H indicates high byte expansion size; valid sizes 0200H = 512 kilobytes I/O adapter RAM, 0400H = 1024 kilobytes I/O adapter RAM (2 adapter cards), and 0600H to 3C00H = 1536 kilobytes I/O adapter (3 adapters) to 15360 kilobytes I/O adapter (15 megabytes maximum).

DATE CENTURY BYTE

BITS 7-0 - indicate BCD value for the century (BIOS interface to read and set).

INFORMATION FLAG BYTE

BIT 7 - if set indicates IBM-AT 128 kilobyte memory expansion option is installed.

BIT 6 - is used by the setup utility to put out a first used message after initial setup.

BITS 5-0 - are RESERVED.

2.4.7 Keyboard Control

The keyboard controller is a single-chip microcomputer (INTEL 8042), which is programmed to be IBM-AT keyboard compatible, with a serial interface. This controller communicates with the keyboard through the status register, an input buffer, and an output buffer; the controller has two byte wide I/O ports and two test inputs (the test inputs are used to read the state of the clock line and the data line).

The keyboard controller receives serial data from the keyboard, checks the parity of the data, translates scan codes, and presents the data to the system as a byte of data in its output buffer; the controller will interrupt the CPU when data is placed in its output buffer.

Data is sent to the keyboard by writing to the keyboard controller's input buffer (the status register contains bits that indicate if an error was detected while receiving the data). Bytes of data are serialized and sent to the keyboard, with odd parity bits automatically inserted; the keyboard is required to acknowledge all data transmissions, and the acknowledgment separates byte transmissions.

The keyboard sends serial format data to the controller, using an 11 bit frame (data sent is synchronized by a clock supplied by the keyboard); the first bit is a start bit, and is followed by eight data bits, an odd parity bit, and a stop bit. At the end of a transmission, the keyboard controller disables the interface until the system accepts the byte. For a received byte of data with a parity error, a resend command is automatically sent to the keyboard. Whenever the keyboard controller is unable to receive the data correctly, FEH is placed in its output buffer, and the parity bit in the status register is set to 1, indicating a receive parity error. The keyboard controller will also time a byte of data from the keyboard, and if the byte transmission does not end within 2 milliseconds, FEH is placed in the keyboard controller's output buffer, and the receive time out bit in the status register is set (no retries will be attempted on a receive time out error).

For scan codes, which are received from the keyboard, the keyboard controller converts these codes to system scan codes before they are put into the controller's output buffer.

Data is sent to the keyboard in the same serial format used to receive data from the keyboard; a parity bit is automatically inserted by the keyboard controller. If the keyboard does not start clocking the data out of the keyboard controller within 15 milliseconds, or completes that clocking within 2 milliseconds, FEH is placed in the keyboard controller's output buffer, and the transmit time out error bit is set in the status register. If the response contains a parity error, FEH is placed in the keyboard controller's output buffer, and the transmit time out and parity error bits are set in the status register. The keyboard controller is programmed to a set time limit for the keyboard to respond; if 25 milliseconds are exceeded, the keyboard controller places FEH in its output buffer and sets the transmit an receive time out error bits in the status register (no retries are made by the keyboard controller for any transmission error).

2.4.7 Keyboard Control -- CONTINUED

The following figure shows the conversion between scan codes, and the key relation on the keyboard.

<u>KB SCAN CODE</u>	<u>SYSTEM SCAN CODE</u>	<u>KEY</u>	<u>KEY DESCRIPTION</u>
00	FF		
76	01	90	ESC
16	02	2	! or 1
1E	03	3	@ or 2
26	04	4	# or 3
25	05	5	\$ or 4
2E	06	6	% or 5
36	07	7	^ or 6
3D	08	8	& or 7
3E	09	9	* or 8
46	0A	10	(or 9
45	0B	11	) or 0
4E	0C	12	_ or -
55	0D	13	+ or =
66	0E	15	backspace
0D	0F	16	tab function
15	10	17	Q or q
1D	11	18	W or w
24	12	19	E or e
2D	13	20	R or r
2C	14	21	T or t
35	15	22	Y or y
3C	16	23	U or u
43	17	24	I or i
44	18	25	O or o
4D	19	26	P or p
54	1A	27	{ or [
5B	1B	28	} or]
5A	1C	43	carriage return
14	1D	30	Cntl
1C	1E	31	A or a
1B	1F	32	S or s
23	20	33	D or d
2B	21	34	F or f
34	22	35	G or g
33	23	36	H or h
3B	24	37	J or j
42	25	38	K or k
4B	26	39	L or l
4C	27	40	: or ;
52	28	41	" or '
0E	29	1	~ or `
12	2A	44	shift
5D	2B	14	or \
1A	2C	46	Z or z
22	2D	47	X or x

2.4.7 Keyboard Control -- CONTINUED

<u>KB SCAN CODE</u>	<u>SYSTEM SCAN CODE</u>	<u>KEY</u>	<u>KEY DESCRIPTION</u>
21	2E	48	C or c
2A	2F	49	V or v
32	30	50	B or b
31	31	51	N or n
3A	32	52	M or m
41	33	53	< or ,
49	34	54	> or .
4A	35	55	? or /
59	36	57	shift
7C	37	106	PrtSc or *
11	38	58	Alt
29	39	61	space
58	3A	64	Caps Lock
05	3B	70	F1
06	3C	65	F2
04	3D	71	F3
0C	3E	66	F4
03	3F	72	F5
0B	40	67	F6
02 or 83	41	73	F7
0A	42	68	F8
01	43	74	F9
09	44	69	F1
77	45	95	Num Lock
7E	46	100	Scroll Lock or Break
6C	47	91	7 or Home
75	48	96	8 or up cursor
7D	49	101	9 or Pg Up
7B	4A	107	-
6B	4B	92	4 or left cursor
73	4C	97	5
74	4D	102	6 or right cursor
79	4E	108	+
69	4F	93	1 or End
72	50	98	2 or down cursor
7A	51	103	3 or Pg Dn
70	52	99	0 or INS
71	53	104	. or DEL
7F or 84	54	105	SYS REQ
60	55	R	reserved
61	56	R	reserved
78	57	R	reserved
07	58	R	reserved
0F	59	R	reserved
17	5A	R	reserved
1F	5B	R	reserved
27	5C	R	reserved
2F	5D	R	reserved

2.4.7 Keyboard Control -- CONTINUED

<u>KB SCAN CODE</u>	<u>SYSTEM SCAN CODE</u>	<u>KEY</u>	<u>KEY DESCRIPTION</u>
37	5E	R	reserved
3F	5F	R	reserved
47	60	R	reserved
4F	61	R	reserved
56	62	R	reserved
5E	63	R	reserved
08	64	R	reserved
10	65	R	reserved
18	66	R	reserved
20	67	R	reserved
28	68	R	reserved
30	69	R	reserved
38	6A	R	reserved
40	6B	R	reserved
48	6C	R	reserved
50	6D	R	reserved
57	6E	R	reserved
6F	6F	R	reserved
13	70	R	reserved
19	71	R	reserved
39	72	R	reserved
51	73	R	reserved
53	74	R	reserved
5C	75	R	reserved
5F	76	R	reserved
62	77	R	reserved
63	78	R	reserved
64	79	R	reserved
65	7A	R	reserved
67	7B	R	reserved
68	7C	R	reserved
6A	7D	R	reserved
6D	7E	R	reserved
6E	7F	R	reserved

2.4.8 Speaker

The system unit has a 2.25 inch permanent magnet speaker which can be driven from: the I/O port output bit, the counter/timer clock out, or both.

3.0 INTERFACE REQUIREMENTS

3.1 System I/O (AT) Bus

This section identifies the I/O interface requirements for both the PC compatible option cards and the AT compatible option cards. Out of the 8 expansion slots available, only 2 are reserved for PC compatibility; all 8 slots have a 62 pin connector socket, and 6 have an additional 36 pin connector socket (used on AT compatible cards only).

3.1.1 PC Interface Compatibility

The following connector pin assignment is used on both the PC and AT option slots; this connector socket has 62 pins.

PIN	SIGNAL NAME	I/O	PIN	SIGNAL NAME	I/O
A1	-I/O CH CK	I	B1	GND	GROUND
A2	SD7	I/O	B2	RESET DRV	O
A3	SD6	I/O	B3	+5 VDC	POWER
A4	SD5	I/O	B4	IRQ9	I
A5	SD4	I/O	B5	-5 VDC	POWER
A6	SD3	I/O	B6	DRQ2	I
A7	SD2	I/O	B7	-12 VDC	POWER
A8	SD1	I/O	B8	OWS	I
A9	SD0	I/O	B9	+12 VDC	POWER
A10	-I/O CH RDY	I	B10	GND	GROUND
A11	AEN	O	B11	-SMEMW	O
A12	SA19	I/O	B12	-SMEMR	O
A13	SA18	I/O	B13	-IOW	I/O
A14	SA17	I/O	B14	-IOR	I/O
A15	SA16	I/O	B15	-DACK3	O
A16	SA15	I/O	B16	DRQ3	I
A17	SA14	I/O	B17	-DACK1	O
A18	SA13	I/O	B18	DRQ1	I
A19	SA12	I/O	B19	-REFRESH	I/O
A20	SA11	I/O	B20	CLK	I
A21	SA10	I/O	B21	IRQ7	I
A22	SA9	I/O	B22	IRQ6	I
A23	SA8	I/O	B23	IRQ5	I
A24	SA7	I/O	B24	IRQ4	I
A25	SA6	I/O	B25	IRQ3	I
A26	SA5	I/O	B26	-DACK2	O
A27	SA4	I/O	B27	T/C	O
A28	SA3	I/O	B28	BALE	O
A29	SA2	I/O	B29	+5 VDC	POWER
A30	SA1	I/O	B30	OSC	O
A31	SA0	I/O	B31	GND	GROUND

3.1.2 AT Interface Compatibility

The following connector pin assignment is used on the AT compatible option slots only; this connector socket has 36 pins.

<u>PIN</u>	<u>SIGNAL NAME</u>	<u>I/O</u>	<u>PIN</u>	<u>SIGNAL NAME</u>	<u>I/O</u>
C1	SBHE	I/O	D1	-MEM CS16	I
C2	LA23	I/O	D2	-I/O CS16	I
C3	LA22	I/O	D3	IRQ10	I
C4	LA21	I/O	D4	IRQ11	I
C5	LA20	I/O	D5	IRQ12	I
C6	LA19	I/O	D6	IRQ15	I
C7	LA18	I/O	D7	IRQ14	I
C8	LA17	I/O	D8	-DACK0	O
C9	-MEMR	I/O	D9	DRQ0	I
C10	-MEMW	I/O	D10	-DACK5	O
C11	SD08	I/O	D11	DRQ5	I
C12	SD09	I/O	D12	-DACK6	O
C13	SD10	I/O	D13	DRQ6	I
C14	SD11	I/O	D14	-DACK7	O
C15	SD12	I/O	D15	DRQ7	I
C16	SD13	I/O	D16	+5 VDC	POWER
C17	SD14	I/O	D17	-MASTER	I
C18	SD15	I/O	D18	GND	GROUND

3.1.3 System I/O (AT) Bus Signal Description

The following signal descriptions for the System I/O Bus, are for both PC and AT compatible option cards (differentiation is presented in the compatibility sections above). Note, that all signal lines are TTL compatible levels, and that I/O adapters should be designed with a maximum of two low power Shottky (LS) loads per line.

* **CLK** -- (clock) signal (8 megahertz, 50 % duty cycle signal) is used only for synchronization, and is not intended for uses requiring a fixed frequency.

* **SA0 thru SA19** -- are 20 address lines used to address memory and I/O devices within the system. They are gated on the system bus when the signal 'BALE' is high and are latched on the falling edge of 'BALE'. Generation of these signals are by the CPU or a DMA controller, but other microprocessors or DMA controller that reside on the bus may drive the address lines.

* **LA17 thru LA23** -- signals (unlatched) are used in conjunction with SA0 thru SA19 to address memory and I/O devices within the system; they give the system up to 16 megabytes of addressability (Validity of these signals are when 'BALE' is high; they are not latched during CPU cycles, and therefore do not stay valid for the whole cycle). Their main purpose is to generate memory decodes for 1 wait-state memory cycles; the decodes should be latched by I/O adapter on the falling edge of 'BALE'. These signals may be driven by other microprocessors or DMA controllers that reside on the bus.

* **BALE** (buffered) -- is an address latch enable generated by the 82288 bus controller; it is used to latch valid addresses and memory decodes from the CPU, and is used as a valid CPU or DMA (forced high during DMA cycles) address indicator, in conjunction with AEN.

* **AEN** -- (address enable) is used to remove the CPU and other devices from the bus to allow DMA transfers to take place. During AEN active, the DMA controller has control of the address bus, the data bus READ command lines, and the WRITE command lines.

* **SD0 thru SD15** -- signals provide bus bits 0 thru 15 for the CPU, memory and I/O devices (D0 is the least significant bit and D15 is the most significant bit). All 8-bit devices on the bus should use D0 thru D7 for communications to the CPU (D8 thru D15 will be gated to D0 thru D7 during transfers to these devices, to provide 2 byte wide transfers per 16-bit transfer), while 16-bit devices will use D0 thru D15.

* **RESET DRV** -- signal (active high) is used to reset or initialize the system logic during power-up time, or during a low line voltage outage.

3.1.3 System I/O (AT) Bus Signal Description -- CONTINUED

* **-I/O CH CK** -- signal indicates an uncorrectable system error when active. The -I/O channel check provides the system board with parity information about memory or devices on the bus.

* **I/O CH RDY** -- signal is used to lengthen I/O or memory cycles when driven low by the active device (this signal should not be held low for more than 2.5 microseconds). Any slow device using this line should drive it low immediately upon detecting its valid address and a READ or WRITE command.

* **IRQ3 THRU IRQ15** -- signals (active high, and must remain high until the CPU acknowledges it) are used to signal the CPU that an I/O device needs attention (these interrupt requests are prioritized in descending order 9 thru 15, and 3 thru 7). Interrupt 13 is used on the system board and is not available on the bus, and interrupt 8 is used for the real time clock.

* **-IOR** -- is a read signal (active low) that instructs an I/O device to drive its data onto the data bus. This line may be driven by the CPU or the DMA controller resident on the bus.

* **-IOW** -- is a write signal (active low) that instructs an I/O device to read the data bus. This line may be driven by the CPU or the DMA controller resident on the bus.

* **-MEMR** -- memory read signal (active low) is active on all memory read cycles (may be driven by any microprocessor or DMA in the system), and instructs the memory devices to drive data onto the data bus. The address lines must be valid on the bus for one system clock period before driving this signal active.

* **-SMEMR** -- is an active signal (active low) only when the memory decode is within the low 1 megabyte range. This signal is derived from the '-MEMR' signal active and the decode of the low 1 megabyte of memory.

* **-MEMW** -- memory write signal (active low) is active on all memory read cycles (may be driven by any microprocessor or DMA in the system), and instructs the memory devices to store present data onto the data bus. The address lines must be valid on the bus for one system clock period before driving this signal active.

* **-SMEMW** -- is an active signal (active low) only when the memory decode is within the low 1 megabyte range. This signal is derived from the '-MEMR' signal active and the decode of the low 1 megabyte of memory.

3.1.3 System I/O (AT) Bus Signal Description -- CONTINUED

* **DRQ0 THRU DRQ7** -- DMA requests are asynchronous, and are used by peripheral devices to gain DMA service or control of the system; they are prioritized in descending order from DRQ0 thru DRQ7. A request is generated by driving a DRQ line active high, and holding it until the corresponding DACK (acknowledge line) signal goes active. DRQ0 thru DRQ3 will perform 8 bit transfers, and DRQ5 thru DRQ7 will perform 16 bit transfers; DRQ4 is used on the system board and is not available on the bus.

* **DACK0 THRU DACK7** -- DMA acknowledge signals (active low) are used to acknowledge DMA requests (DRQ0 thru DRQ7); DACK4 is used on the system board and is not available on the bus.

* **REFRESH** -- signal is used to indicate a refresh cycle, and can be driven by a microprocessor on the bus.

* **T/C** -- terminal count signal provides a pulse when the terminal count for any DMA channel is reached.

* **SBHE** -- system bus high enable indicates data transfer on the upper byte of the data bus (SD8 thru SD15); 16 bit devices use this signal to condition data bus buffers tied to SD8 thru SD15.

* **-MASTER** -- signal is used in conjunction with a DRQ line to gain control of the system; if this signal is held low for more than 15 microseconds, system memory may be lost because of a lack of refresh. A processor or DMA controller on the bus may issue a DRQ to a DMA channel in cascade mode and receive a '-DACK'; reception of the '-DACK' will allow the microprocessor to pull the '-MASTER' line low, which will allow it to control the system address, data, and control lines (condition known as tri-state). After '-MASTER' is low, the processor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a READ or WRITE command.

* **-MEM CS16** -- (not) memory 16 bit chip select (derived from the decode of LA17 thru LA23), signals the system board if the present data transfer is a 1 wait-state, 16 bit, memory cycle. Note, this signal is active low, and should be driven with an open collector or tri-state driver capable of sinking 20 milliamperes of current.

* **-I/O CS16** -- (not) I/O 16 bit chip select (derived from an address decode), signals the system board that the present data transfer is a 16 bit, 1 wait-state, I/O cycle. Note, this signal is active low, and should be driven with an open collector or tri-state driver capable of sinking 20 milliamperes of current.

* **OSC** -- oscillator signal is a high speed clock with a 70 nanosecond period (14.31818 megahertz), asynchronous with the system clock, and has a 50 % duty cycle.

3.1.3 System I/O (AT) Bus Signal Description -- CONTINUED

* OWS -- signal indicates to the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16 bit device without wait cycles, the 'OWS' signal is derived from an address decode gated with a READ or WRITE command. In order to run a memory cycle to an 8 bit device with a minimum of two wait states, the 'OWS' signal is driven active one system clock after the READ or WRITE command is active gated with the address decode for the device (memory read and write commands to an 8 bit device are active on the falling edge of the system clock). Note, this signal is active low, and should be driven with an open collector or tri-state driver capable of sinking 20 milliamperes of current.

THEORY OF OPERATION

TANDY MODEL 3000 COMPUTER
MAIN LOGIC BOARD ASSEMBLY

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1.0 DETAILED DESIGNS

1.1 Clock Circuits

The system clock logics are derived from the INTEL 82284 chip (U42, sheet 4 of the schematics). This device uses an external 16MHZ parallel resonant, fundamental mode crystal, Y2, which is the source of all system timing. This clock, called PRCLK, is synchronized with processor status signal S1 by U36/A (sheet 3), and is then divided by two to 8MHZ by U29/A which provides the system and peripheral clocks called SCLK(H) and SCLK(L). PCLK(H) and PCLK(L) are also derived by dividing the PRCLK by two but they are not synchronized with S1. PCLK(H) and PCLK(L) are the 8042 CPU (U6, sheet 12) clocks which require a clocked setup time prior to reset going away. The processor status signal S1 is valid after reset and so cannot be used to synchronize the 8042 clock. The DMA clock, signal DMACK, is derived by dividing the SCLK by two to 4MHZ.

An 8284 INTEL clock device (U47, sheet 3) provides two clocks which are not synchronous to any of the above clocks. One of the clocks is the OSC clock used by the I/O channel only which has a period of 70ns (14.31818 MHZ). The other clock is derived by dividing the 8284 osc output by two to 1.19MHZ and is used for the system timer chip (8253, U4, sheet 11). The CMOS real time clock controller uses a 32.768KHZ crystal (Y1, sheet 11) configured with a CMOS driver.

1.2 Wait State and Conversion Control

These logics allow compatibility with 8-bit PC type option boards using 8 or 16-bit data CPU instructions.

All 8-bit data references to 8-bit devices have four wait states inserted, resulting in a 1000-nanoscond microprocessor cycle (assuming 8MHZ CPU). CPU odd memory byte location references (BHE active low and A0 inactive high) to 8-bit devices are transferred onto the upper eight bit data bus D8-D16 for a read command and the lower eight bit data bus D0-D8 for a write command cycle.

All 16-bit CPU references to 8-bit devices have 10 wait states inserted, resulting in a 2000-nanoscond microprocessor cycle time. During a CPU read operation the hardware allows transfers of the first 8 data bits through a normal CPU cycle with four wait states inserted; these first 8-bits are latched and held in the 74ALS646 bus transceiver (U82, sheet 4) until the second eight data bits are transferred. The second eight bit transfer continues to wait the CPU by inserting four more wait states. The 82288 bus controller (U49, sheet 9) is temporarily tri-stated to end the first transfer and then released to allow regeneration of the control signals for the second transfer. The second transfer gates the next lower eight bits onto the upper data bus bits D8 - D16, and then releases the CPU to complete the cycle. A similar process takes place for a CPU write operation except data is transferred from the CPU's upper eight bit data bus onto the lower eight bit data bus during the second write cycle.

1.2 Wait State and Conversion Control (continued)

Following are the equations for the 16L8A PAL which senses and controls the transfer logics:

```

/*****
/* Allowable Target Device Types: 16L8 */
*****/

/** Inputs **/

PIN 1 = RAS ; /* MEMORY READ OR WRITE */
PIN 2 = !MWT ; /* MEMORY WRITE */
PIN 3 = !IOR ; /* I/O READ */
PIN 4 = AIOW ; /* I/O WRITE */
PIN 5 = Q1 ; /* ONE WAIT STATE */
PIN 6 = !IOS16 ; /* 16-BIT DATA PATH (I/O) */
PIN 7 = !AEN1 ; /* DMA CNTRL 1 ENABLED */
PIN 8 = !AEN2 ; /* DMA CNTRL 2 ENABLED */
PIN 9 = Q4 ; /* FOUR WAIT STATES */
PIN 11 = SYS16 ; /* 16-BIT DATA PATH (MEMORY) */
PIN 13 = !RESOWS ; /* RESET OR NO WAIT STATES */

/** Outputs **/

PIN 12 = !END ; /* RESET READY LOGICS */
PIN 14 = !DMAEN ; /* AEN1 OR AEN2 */
PIN 15 = !XAO ; /* BUFFERED ADDRESS */
PIN 16 = !XBHE ; /* BUFFERED ADDRESS SELECT */
PIN 17 = !GATE ; /* D0-D7 TO D8-D15 OR VICE VERSA */
PIN 18 = !DIR ; /* DIR OF DATA DURING GATE */
PIN 19 = !CONV ; /* 16-BIT DATA TO/FROM 8-BIT DATA*/

/** Declarations and Intermediate Variable Definitions **/

/** Logic Equations **/

CONV = RAS & Q1 & XBHE & XAO & !AEN1 & !AEN2 & !SYS16 #
      IOR & Q1 & XBHE & XAO & !AEN1 & !AEN2 & !IOS16 #
      AIOW & Q1 & XBHE & XAO & !AEN1 & !AEN2 & !IOS16;

DIR = !MWT & RAS & AEN1 #
     MWT & XBHE & !AEN1 & !AEN2 #
     AIOW & XBHE & !AEN1 & !AEN2;

GATE = MWT & XBHE & !XAO & !AEN1 & !AEN2 & !SYS16 #
      RAS & XBHE & AEN1 & SYS16 #
      RAS & XBHE & !XAO & !AEN1 & !AEN2 & !SYS16 #
      IOR & !IOS16 & !AEN1 & !AEN2 & !XAO & XBHE #
      AIOW & !IOS16 & !AEN1 & !AEN2 & !XAO & XBHE #
      IOR & AEN1 & !IOS16 & XBHE;

```

1.2 Wait State and Conversion Control (continued)

```
XBHE  = !XAO & AEN1 # AEN2;
XBHE.OE= DMAEN;

XAO    = AEN2;
XAO.OE = AEN2;

DMAEN  = AEN1 #
        AEN2;

END    = RAS & RESOWS #
        AIOW & RESOWS #
        Q4 #
        IOR & Q1 & IOS16 #
        AIOW & Q1 & IOS16 #
        RAS & Q1 & SYS16;
```

1.3 Shut Down Control

Shutdown occurs when a severe error is detected that prevents further instruction processing by the CPU. The shutdown logics (U57/A, U45/A/B, U46/B, U23/A, U35/D, sheet 3) decode a shutdown condition only (See INTEL 80286 Hardware Reference Manual for halt conditions). A shutdown bus operation is detected when S1, S0, A1 and COD/INTA are low and M/IO is high. Upon detecting this condition the hardware resets the CPU only using signal RESCPU, thereby allowing all other hardware (including memory) to retain their previous values.

2.0 80286 Local Bus

2.1 82288 Bus Controller

This 20-pin dip (U42, sheet 4) is used to provide address latch control, and command outputs based on the 80286 status lines. The INTEL Hardware Reference manual contains the functional description. The use of this device in the TANDY Model 3000 project differs from the INTEL spec in that CEN/AEN is used in conjunction with the conversion logics to tri-state the 82288 outputs during the second half cycle of a eight-bit to 16-bit transfer. The outputs are also tri-stated during a DMA transfer by asserting the MB pin high.

2.2 80287 Numeric Processor Extension

The 80287 (U78, sheet 4) operates at 1/3 the frequency of the microprocessor clock. It is configured as an I/O device having ports 00F8h, 00FAh, and 00FCh. A 16L8A PAL device (U70, sheet 4) is used to interface the 80287 to the CPU. This PAL provides the I/O decode [NPCS(L)], the 80287 Reset, the 286BUSY signal, and Interrupt Request 13.

```

/*****
/* Allowable Target Device Types:16L8
*****/

/** Inputs **/

PIN 1  =RESET           ; /* */
PIN 2  =!ERROR          ; /* */
PIN 3  =!BUSY           ; /* */
PIN 4  =XA0             ; /* */
PIN 5  =XA3             ; /* */
PIN 6  =!XIOW           ; /* */
PIN 7  =SMIO            ; /* */
PIN 8  =!CS287          ; /* */
PIN 9  =!INTA           ; /* */

```

2.2 80287 Numeric Processor Extension (continued)

```
/** Outputs **/
```

```

PIN    12  =!NPCS           ; /* */
PIN    13  =L               ; /* */
PIN    14  =M               ; /* */
PIN    15  =N               ; /* */
PIN    16  =O               ; /* */
PIN    17  =287RESET        ; /* */
PIN    18  =IRQ13           ; /* */
PIN    19  =!287BUSY        ; /* */

```

```
/** Declarations and Intermediate Variable Definitions **/
```

```
/** Logic Equations **/
```

```

NPCS      =                XA3 & CS287 & !SMIO & !INTA;

!IRQ13     =                !ERROR #
                        !BUSY & !IRQ13;

!287RESET  =                !RESET & SMIO #
                        !RESET & XA3 #
                        !RESET & !XA0 #
                        !RESET & !XIOW #
                        !RESET & !CS287 #
                        !RESET & INTA;

287BUSY    =                BUSY #
                        !N;

!N          =                O & !N & !M #
                        L;

!M          =                O & !M #
                        L #
                        !IRQ13;

!L          =                !O #
                        M & !L #
                        !IRQ13;

!O          =                287RESET #
                        !XA0 & !XA3 & XIOW & !SMIO & CS287 & !INTA;

```

3.0 Local Memory Bus

3.1 Memory Decode Prom

Memory is decoded with the use of a 512 x 8 byte 28S42 PROM. (U63, sheet 7). The data outputs are latched through a 74LS573 (U64, sheet 7) by either ALE or HLDA(H). The inputs to the PROM include A17 thru A23, RFRSH(H), and RAMSEL(L). Address bits A17 thru A23 allow a decode resolution to 128KB to allow a memory configuration of 0-640KB. The RAMSEL(L) signal allows an upgrade option of 128KB from 512K-640KB when asserted low. Asserted high allows only 512KB. The RFRSH(H) signal asserts RAS0, RAS1, Fl6, and MEGCS(L) in order to refresh all memory in the system in parallel. Fl6 is used to signify a 16-bit data width and that no command delays are needed. MEGCS(L) drives the SMWT and SMRD control signals onto the peripheral bus during the low one megabyte range only.

The following table includes the CPU address translated to the PROM address, the data values of the PROM at those address's and the function of the data values:

CPU ADDR	PROM ADDR	DATA	FUNCTION
000000-07FFFF	000-003	91H	0-512K MEMORY
080000-09FFFF	004	61H	512K-640K MEMORY
0A0000-0DFFFF	005-006	37H	PERIPHERAL MEMORY
0E0000-0FFFFF	007	30H	PROM
FE0000-FFFFFF	07F	30H	PROM
000000-07FFFF	100-103	91H	0-512K MEMORY
080000-0DFFFF	104-106	37H	LOW MEG CS ONLY
0E0000-0FFFFF	107	30H	PROM
FE0000-FFFFFF	17F	30H	PROM
000000-000100	180	FlH	REFRESH & LOW MEG CS
000000-000100	080	FlH	REFRESH & LOW MEG CS

All remaining PROM address space must be programmed with a data value of 3FH.

The following table is a bit definition of the 28S42 ROM outputs. The active output polarities are indicated with (H) for active high state or (L) for active low.

D7	RAS0(H)
D6	RAS1(H)
D5	CAS0(L)
D4	CAS1(L)
D3	LOW MB MEMORY(L)
D2	MEMORY SELECT(L)
D1	16-BIT DATA(L)
D0	ROM SELECT(L)

3.2 ROM Subsystem

There are four ROM modules on the main PCB. Two are used for the BIOS and two are left for optional expansion. The basic configuration is jumper selected for 27128K-bit (16K by 8 bits) ROM's occupying U59 and U61 (sheet 6). In this configuration the jumpers are placed between E5 & E9 and E7 & E11 (sheet 6) and use address A15 to select between the BIOS ROM's or the optional ROM. The BIOS ROM starting address location is 0E8000H or FE8000H while the optional starting address location is 0E0000H or FE0000H.

To expand to 27256k-bit (32K by 8 bit) ROM's requires the jumpers to be placed between E6 & E10, and E8 & E12. This places the starting locations of the ROM's to 0F0000H or FF0000H for the BIOS and 0E0000H or FE0000H for the optional ROM.

NOTE: All four ROM modules must be of the same type i.e., four 27128's or four 27256's.

The maximum Rom access time is calculated as follows:

375ns	cycle time
- 0ns	CPU address delay
- 78ns	ALE
- 20ns	ALS573 output from ALE (sheet 7)
- 11ns	ALS04
- 8ns	ALS00 to chip select on the ROM's
- 10ns	data thru ALS245 (sheet 6)
- 10ns	data thru ALS245 (sheet 4)
- 10ns	CPU data setup time
- 27ns	bus capacitance
201ns	ROM access (NOTE: address decode determines access time separate from mem read. Memory read controls output enable)

3.3 RAM Subsystem

The decoding for the RAM is explained in section 3.1. The control logics uses a 200ns, 40ns/tap, 5-tap delay line (U67, sheet 7) along with the decode, XA0 and XBHE. The two RAS's (one per bank) are the "OR" condition of the memory read or memory write control lines "AND'd" with a valid decode. CAS is asserted 80ns after RAS and steered to a row of DRAM with a valid range decode, XBHE and XA0. There are four CAS's, each controlling a 9-bit memory array. The total RAS time is 200ns, and CAS time is 120ns. RAS precharge time is 175ns. Refresh occurs every 15us under a CPU hold cycle (sheet 12) by driving the memory read control line (sheet 9) qualified with a valid RFRSH request. CAS is not asserted during refresh.

3.4 Parity Control

The parity control logics is located on sheet 7 of the schematics. These logics consist of four DRAM chips (U99, U108, U117, U126) and two 74F280 parity generator/checker devices (U62, U71) which outputs are selected by XA0 or XBHE. A valid memory cycle is selected by OR'ing the CAS decode output lines allowing parity to be latched in a 74F74 flip-flop (U26/A) with XMRD. The parity DRAM control is accomplished with the same timing as explained in section 3.3.

4.0 Buffered Peripheral Bus

4.1 System Interrupts

Two cascaded 8259 interrupt controller chips (U2 and U3, sheet 11) along with the CPU NMI provide 16 levels of interrupts. The 8259's prioritize all incoming interrupts, interrupt the CPU and respond to a CPU interrupt acknowledge by placing a vectored address on the data bus. The CPU interrupt acknowledge cycle is comprised of two back to back hardware interrupt-acknowledge cycles. The first cycle allows the 8259's to resolve the source of the interrupt by driving the cascade address lines to the slave and the second cycle allows the CPU to read the pre-programmed vector off the data bus from the interrupt controller. The basic timing of these devices can be found in the INTEL 8259A specifications. These controllers reside on the XDATA bus.

4.2 Direct Memory Access

Section 2.4.2 contains the functional description of the DMA controllers (U21 and U22, sheet 10). There are two 16-bit 4-channel LSI DMA devices and one memory page mapper (U20, sheet 10) used to obtain the upper eight address lines. DMA controller U22 is cascaded to DMA controller U21 by means of DREQ0. This allows four DMA channels on U21 and three DMA channels on U22. Refer to the INTEL 8237 reference manual for the basic timing.

4.3 I/O Decode

I/O decode is comprised of an 74ALS138 three to eight decoder (U55, sheet 5 and a 74S288 32 x 8 ROM (U1, sheet 11). The 74ALS138 is strictly an address decode of address lines XA5 thru XA9 with no CPU control lines. System control lines MASTR and HLDA are used to disable decode output during a CPU hold acknowledge cycle when there is no I/O bus master, and to enable the decode output when there is an I/O bus master controlling the system bus. All I/O control lines are decoded by the peripheral device with the exception of the 74S288 ROM decodes. The 74S288 ROM decodes the PPICS signal from the ALS138 along with XA0, XA4, XIOR, and XIOW to obtain the NMI CS, KEYBD I/O, Real Time CMOS clock, and peripheral register select.

4.4 Real Time Clock

The Real Time Clock consist of a Motorola CMOS MC146818 device (U5, sheet 11), a lithium battery back-up and a battery interface circuit (sheet 11). Power is supplied by VCC through a two stage transistor circuit when power is on and above approximately 3.0v. When the voltage drops below this level power is supplied through CR1 & CR2 by the lithium battery. These two diodes isolate the battery from any voltage spikes or high DC levels on VCC. During power down, the total drain on the battery equals 50ua (146818 max) plus 14.5ua (MC14069) for a total of 64.5ua.

5.0 MAIN LOGIC TIMING DIAGRAMS

5.1 SCOPE

Three important timing diagrams relevant to the TANDY model 3000 computer are included in this section.

5.2 CLOCK TIMING

The TANDY Model 3000 computer clock generation timing is indicated on Page 11. Clock generation and timing is discussed in Section 1.1.

of important note is signal ENAS(L) which is S1(L) synchronized to PROC CLK(1), called PRCLK(L) on the schematic. ENAS is used to allow generation of SYSCLK(H), called SCLK(H) on the schematic, which is one-half the rate of PROC CLK(1), or 8 MHZ, and also synchronized to PROC CLK(1).

DMA CLK(H), called DMACK on the schematic, is SYS CLK(H) divided by two.

5.3 REFRESH TIMING

The diagram on Page 12 illustrates the REFRESH CYCLE timing.

Dynamic RAM refresh is required once every 15uS. The refresh request is generated by a timer IC (U4, sheet 11) OUT1. The refresh request is synchronized to the rising edge of DMACK(L) to generate a CPU HRQ (CPU Hold REQuest).

One the HOLD is acknowledged a "dummy" memory READ cycle is initiated. However, while RAS is allowed to pass to the RAM chips, CAS is inhibited. This produces a RAS-only memory access, or a REFRESH cycle.

During the time the refresh is taking place the processor is generating Ti cycles (indicating that it is working internally), Th cycles (indicating that the processor is holding), or both, depending on the actual instruction currently being executed by the processor.

One the "dummy" cycle is complete the CPU HRQ line is brought inactive. This is recognized by the CPU, the hold acknowledge is dropped, and the processor continues processing normally.

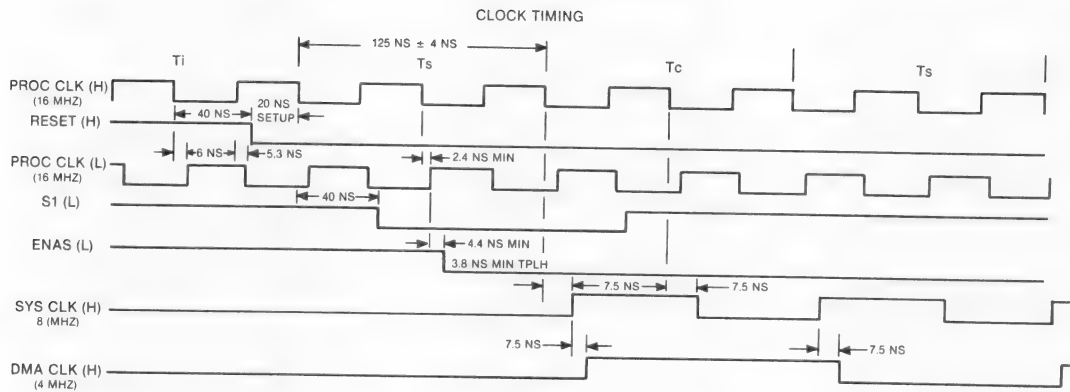
5.4 INTERRUPT ACKNOWLEDGE CYCLE

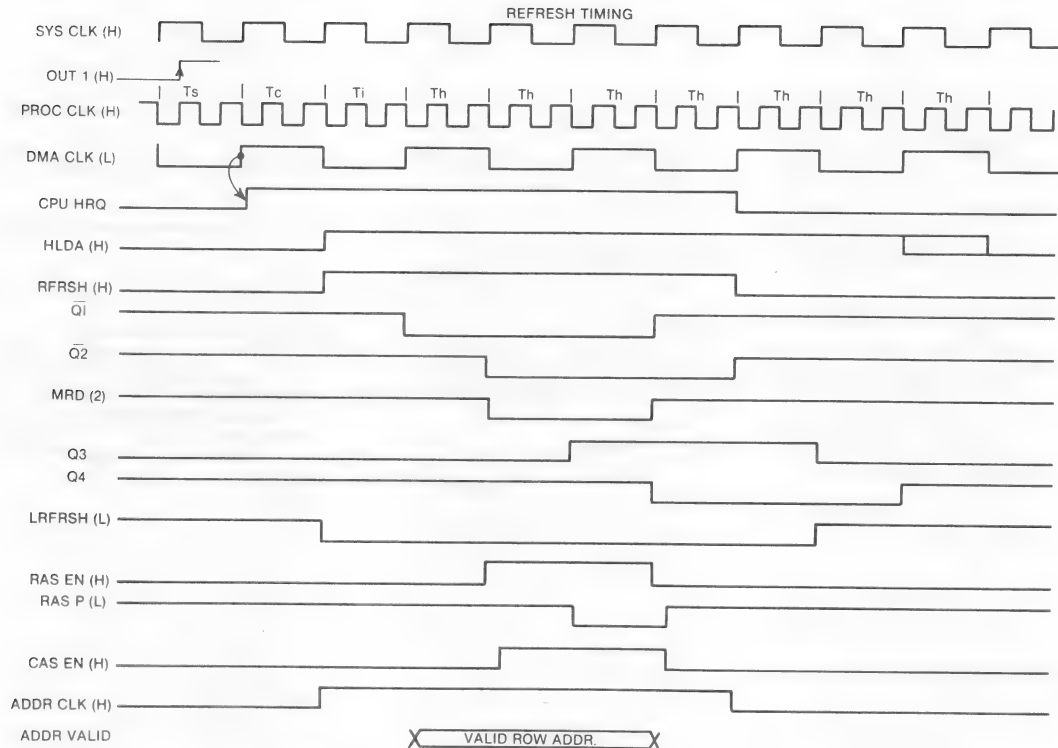
The diagram on Page 13 indicates the INTERRUPT ACKNOWLEDGE (INTA) cycle.

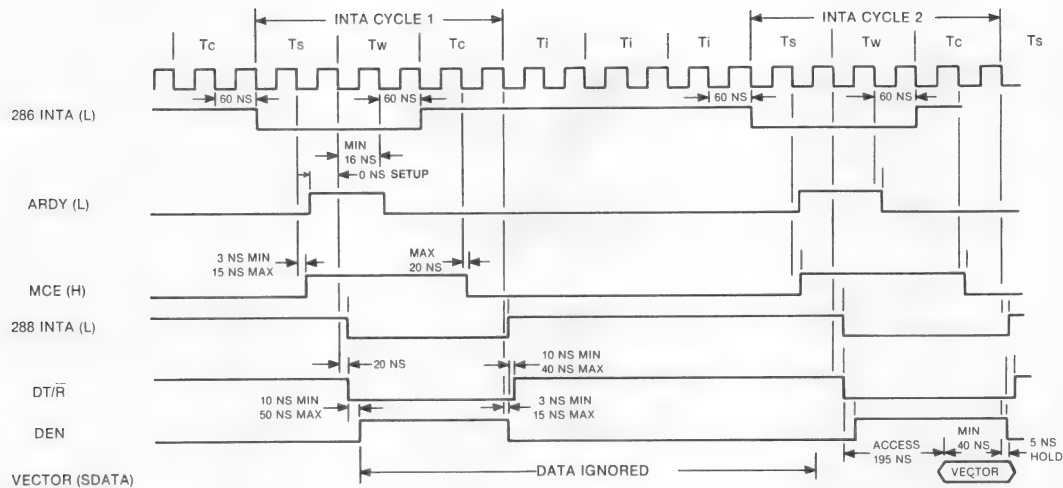
Of primary importance in this diagram is the fact that there are TWO Interrupt Acknowledge cycles for every interrupt generated by the 8259 Interrupt controllers (U2 and U3, sheet 11).

The first INTA cycle is used to indicate to the 8259s that the processor has recognized the attempt to interrupt. This first cycle is used by the 8259 to arbitrate their internal priority settings. Notice that any data appearing on the data lines at this time is ignored by the processor.

The second INTA cycle signals the interrupting 8259 to place an interrupt VECTOR on the data bus during this time. The processor reads this vector and uses it as an offset into a pre-programmed table of interrupts to determine where in memory the necessary interrupt handler routine is located. This routine is then executed by the processor.







TIMING SHOWN IS NOT ACTUAL TIMING.
IT REFLECTS WORST CASE REQUIREMENTS ONLY.

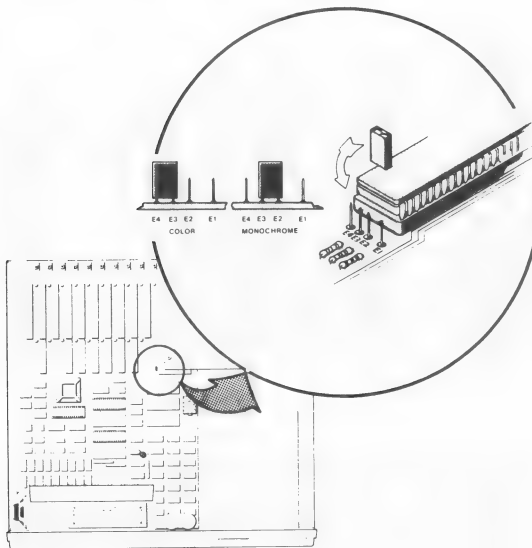
6.0 UPGRADES, JUMPER SETTINGS AND ALIGNMENTS

The following text describes the available jumper setting options and adjustments available on the TANDY Model 3000 computer.

6.1 COLOR / MONOCHROME SETTING

The TANDY Model 3000 is set at the factory for a monochrome video display card and monitor. Before installing a **COLOR** video display card, you must reposition a wire jumper on the computer's main logic board.

The color / monochrome jumper is located between the Serial / Parallel Adapter card (in Slot 10) and the front corner of the power supply chassis. (See the following illustration.)



To reach the jumper, you must remove the serial / Parallel Adapter Card in Slot 10.

The video display jumpers consists of three (3) pins.

JUMPER E2 - E3 MONOCHROME MONITOR [factory default setting]

JUMPER E3 - E4 COLOR MONITOR [user selectable option]

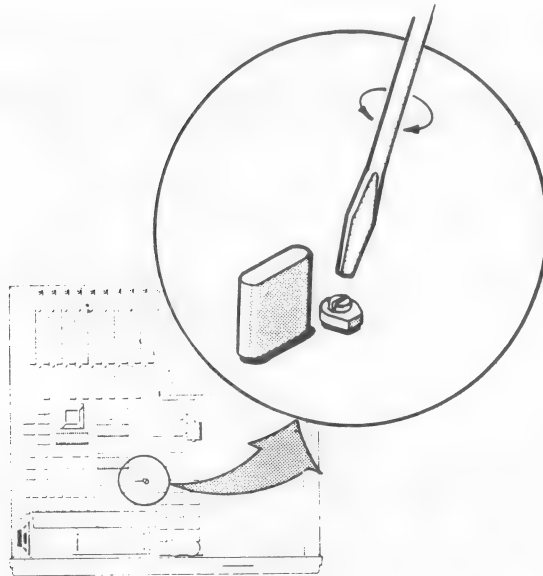
6.2 COLOR BURST CLOCK ADJUSTMENT

If a color video board is installed and a composite video monitor or color television is attached but no color is visible on the monitor it may be necessary to adjust the tunable capacitor on the Main Logic board.

Remove the TANDY Model 3000 computer's cover, then connect the color monitor or color television to the computer. Turn on both the computer and the monitor.

Adjust the Color Burst Clock adjustment until color is displayed on the monitor. (See the following illustration.)

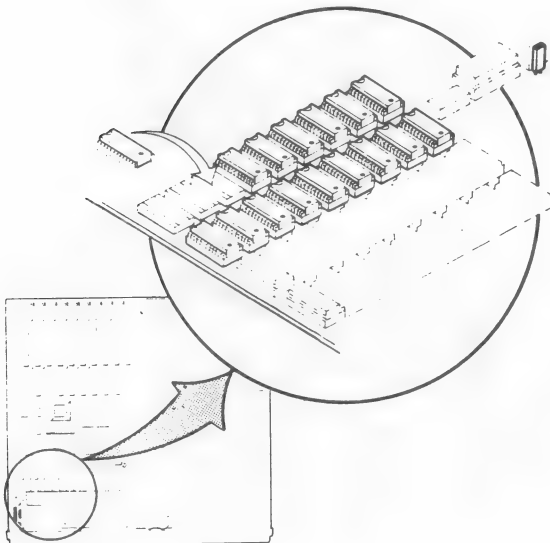
NOTE: You **MUST** use a plastic tuning tool for this adjustment.



6.3 RAM UPGRADE OPTION

The TANDY Model 3000 computer can support an optional 128K Memory Upgrade to bring the total RAM on the Main Logic board to 640K.

1. Remove the computer's cover.
2. The 18 empty RAM sockets are located behind the fan on the left front section of the Main Logic board. (See illustration below.) To gain access to these sockets you must first remove all cards present in Expansion lots 1 through 5. Take care not to damage or apply strain to any interconnecting cables.
3. Note the notch or dot at one end of the RAM chips. Install each chip into its socket **with the notch or dot on the chip facing toward the slots at the rear of the system unit.** (See illustration below.)
4. Install the supplied jumper across pins E13 and E14 on the Main Logic board. (See illustration below.)
5. Reinstall all cards removed from Slots 1 through 5. Verify proper operation using available diagnostics.



6.4 ROM UPGRADE OPTION

The TANDY Model 3000 computer can support two different ROM configurations.

The first is two (2) 27128-type (16K by 8 bit) ROMs. Four (4) ROM locations are available; two are used. The remaining two are for expansion. Using this option there is 64K of ROM space available with 32K used.

The second option is for 27256-type (32K by 8 bit) ROMs. In this case there would be a total ROM address space of 128K available.

To support the 27128-type ROMs requires the following jumpers:

JUMPER E5 - E9 JUMPER E7 - E11 [factory default setting]

If 27256-type ROMs are to be installed then the following jumpers are required:

JUMPER E6 - E10 JUMPER E8 - E12

In either case all four ROMs must be of the same type.

Tandy 3000 Main Logic Sub Assembly

Symbol	Description	Part No.
	Tandy 3000 M/L	AX-0204
	T3000 PCB Rev. A (10.9" x 16" 4 Layer)	8709635A
C1,2,1A,2A,35	Capacitor 47 PF +10% 50V RAD	CF-1366
C3-8,10-13, 15-22,25,26, 28-34,39-43, 45,46-51,57-67, 70-73,77-80, 86-88,107-113, 127-132	Capacitor 0.1 UF Mono Ax.	CC-104JJLA
C9,24,36-38,52, 53,68,69,74-76, 81-83,93,94,96, 105,106,114, 123,124-126, 141,142,151,152	Capacitor 10 UF +20% 16V Rad.	CC-106MDAP
C14	Capacitor 27 PF +15% 50V	CC-270KJCP
C23	Capacitor .01 UF 20% 50V C. Disc	CC-103JJCP
C27	Capacitor 4700 PF 80% 50V RAD	CC-472QJCP
C35	Capacitor .01 UF 10% 50V Ax.	CC-103KJLA
C44	Capacitor Variable, 6-70 PF	ACF-7364
C54,89-92,97- 104,115-122, 133-140,143-149	Capacitor .33 UF +80-50% 50V	CC-334ZJLA
C55	Capacitor 33 PF +10% 50V RAD	CC-330KJCP
C56	Capacitor 15 PF +5% 50V RAD	CC-150DJCP
C84,85,95	Capacitor .047 UF 10% 50V Mono	CC-473KJLA
C150	Capacitor .001 UF 50V 10%	CC-102JJCP
CRL-4	Diode IN4148	DX-0022
E1-14	Staking Pin	AHB-9682
FB1,2	Ferrite Bead	ACA-8242

Symbol	Description	Part No.
J1-10	Connector, 62PB	AJ-5954
J12-17,19	Connector, 36PB	8519258
J21,25	Connector, 4-Pin Header	AJ-7521
J22	Connector, 8-Pin DIN	AJ-7550
J23	Connector, 12-Pin Mate-N-Lock	AJ-1079
J24	Connector, 5-Pin Header	AJ-1078
R1,2	Resistor 470 Ohm 1/4 Watt 5%	N-0169EEC
R3,4,18	Resistor Car F 1K Ohm 1/4 Watt 5%	N-0196EEC
R6	Resistor 150 Ohm 1/4 Watt 5%	N-0142EEC
R7,14-17,21, 25,27-30,100	Resistor Car F 10K Ohm 1/4 Watt 5%	N-0281EEC
R8	Resistor 47 Ohm 1/4 Watt 5%	N-0099EEC
R9,11-13,19	Resistor 300 Ohm 1/4 Watt 5%	N-0158EEC
R10,24,101	Resistor 4.7K Ohm 1/4 Watt 5%	N-0247EEC
R20	Resistor 910 Ohm 1/4 Watt 5%	N-0192EEC
R22,23	Resistor 510 Ohm 1/4 Watt 5%	N-0173EEC
R26	Resistor Car F 51K Ohm 1/4 Watt 5%	N-0344EEC
R93	Resistor 2.2 Meg Ohm 1/4 Watt 5%	N-0454EEC
R102	Resistor 18 Ohm 1/4 Watt 5%	8207027
R103,R104	Resistor 27 Ohm 1/4 Watt 5%	N-0082EEC
RP1,3-7	Resistor Pak 10K Ohm 10-Pin SIP	ARX-0239
RP2,8	Resistor PAK 33 Ohm 10-Pin SIP	ARX-0048
RP9,10	Resistor PAK 33 Ohm 16-Pin DIP	ARX-0390
U1,99-134	Socket 16-Pin DIP	AJ-6581
U2,3,58-61	Socket 28-Pin DIP	AJ-6758
U4	Socket 24-Pin DIP	AJ-5044
U5	IC 146818	MX-5697
U6,21,22,78	Socket 40-Pin DIP	AJ-6580
U7	IC 14069	MX-5425
U8,9,12,17,36 45,46	IC 74ALS74	MX-5689
U10	IC 74LS51	MX-5572
U11	IC 74F11	MX-4979
U13	IC 74F04	MX-5953
U14,26,44,54	IC 74F74	MX-5936
U15	IC 74ALS175	MX-5692
U16,66,94	IC 74ALS244	MX-5853
U18,35,73	IC 74ALS04	MX-5522
U19,41,65,72	IC 74F08	MX-5954
U20	IC 74LS612	MX-5698
U23,69	IC 74ALS00	MX-5445
U24	IC 74ALS10	MX-5527
	14-Pin	

Symbol	Description	Part No.
U25,39	IC 74ALS02	MX-5498
U27,30	IC 74F175	MX-2118
U28,50	IC 74F174	MX-4983
U29	IC 74ALS112	8015112
U31	IC 75477	MX-6111
U32,33,64,85-87	IC 74ALS573	MX-5694
U34	IC 7407	AMX-4628
U37,84	IC 74LS245	AMX-4470
U38,49,63,70	Socket 20-Pin DIP	AJ-6760
U40	IC 74LS125	AMX-4640
U42,47	Socket 18-Pin DIP	AJ-6701
U43,96	IC 74ALS08	MX-5523
U48,53	IC 74ALS32	MX-5688
U51	IC 74F00	MX-6085
U52,68,75,76	IC 74F10	MX-3023
U55	IC 74ALS138	MX-5691
U56	IC 74F257	MX-6083
U57	IC 74ALS27	MX-5542
U62,71	IC 74F280	MX-5435
U67	IC PE21213 Delay Line 200 NS	AMX-5706
U74,98	IC 74S51 Dual AOI Gate	MX-5727
U77	Socket 68-Pin, JADEC "A"	AJ-7539
U79-81,83,88, 89,93	IC 74ALS245	MX-5693
U82	IC 74AS646	MX-5696
U90,91	IC 74F158	MX-2132
U95	IC 74LS590	MX-5695
U97	IC 74S04	AMX-4945
Q1	Transistor 2N3904	AMX-3583
Q2	Transistor 2N3906	AMX-3584
Y1	Crystal 32.768 KHz	MX-1113
Y2	Crystal 16 MHz	MX-0094
Y3	Crystal 14.318 MHz	MX-0095

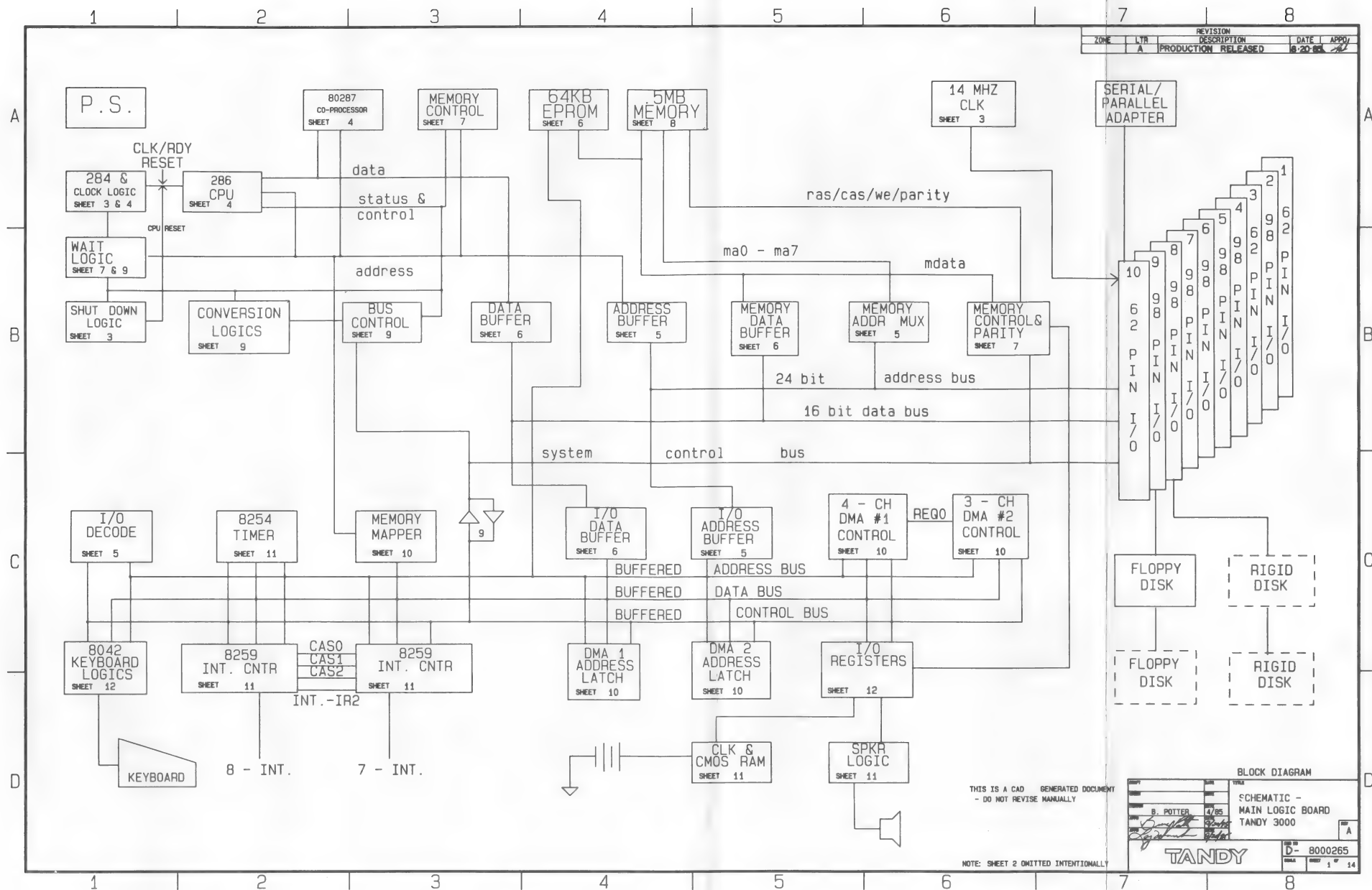
Tandy 3000 Main Logic Main Assembly

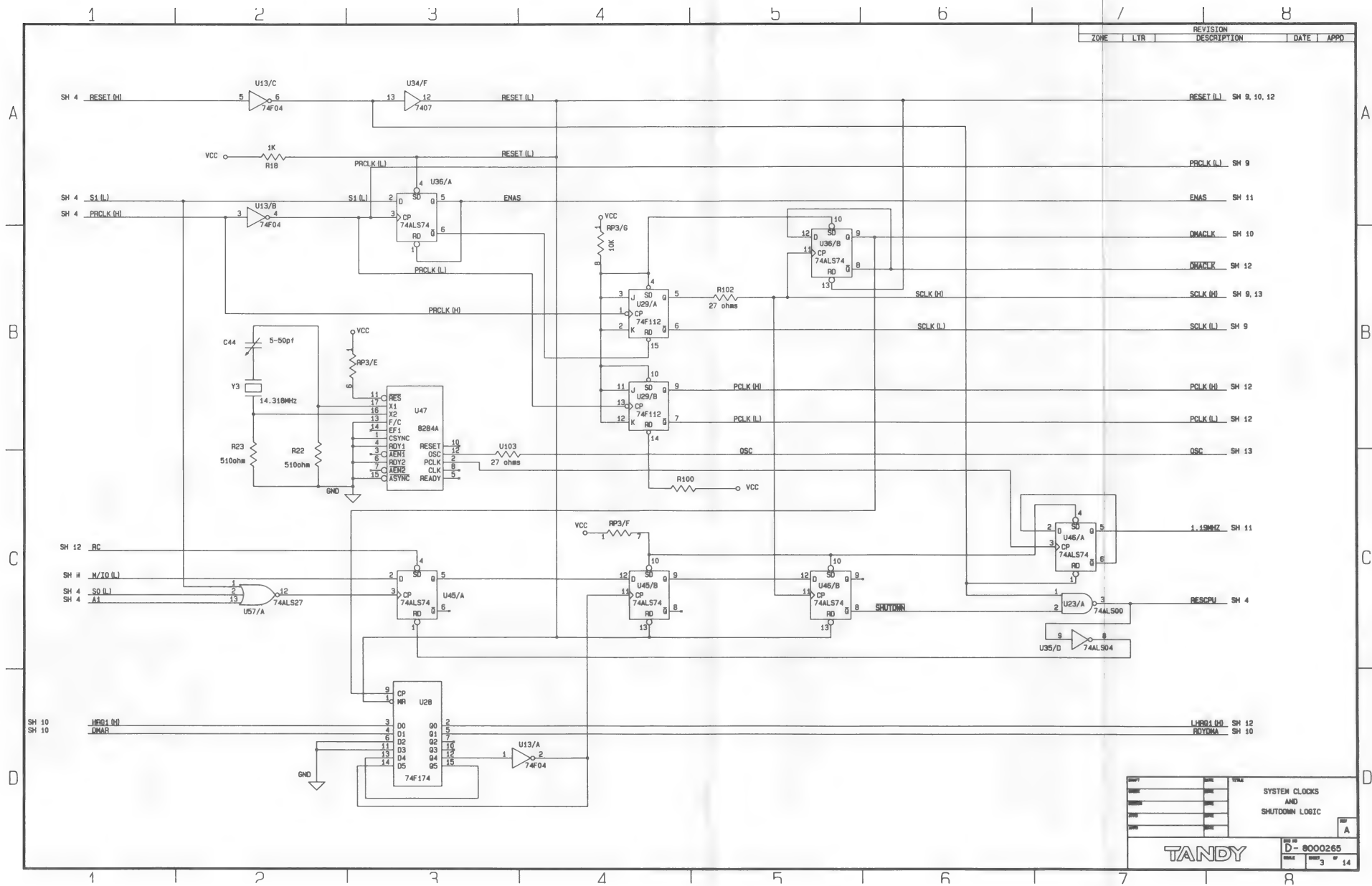
Symbol	Description	Part No.
	Tandy 3000 Main Assembly	889AZ01
	Tandy 3000 Subassembly	AX-0204
	Jumper Plug	AJ-6908
U1	IC 74S288	MX-5701
U2,3	IC 8259A	MX-6001
U4	IC 8254-2	8048284
U6	IC 8042	8040041
U21,22	IC 8237A-5	MX-6778
U38	IC 16L8A PAL	MX-5737
U42	IC 82284-8	MX-5909
U47	IC 8284A	MX-5911
U49	IC 82288-8	MX-5910
U59	IC 27128 EPROM 200 NS	MX-4975
U61	IC 27128 EPROM 200 NS	MX-4976
U63	IC 28S42 512 X 8 PROM	MX-5265
U70	IC 16L8A PAL	MX-5787
U77	IC 80286-8	MX-5908
U117-134	TMS4256-15NL 256K X 1 DRAM 150NS	MX-6796

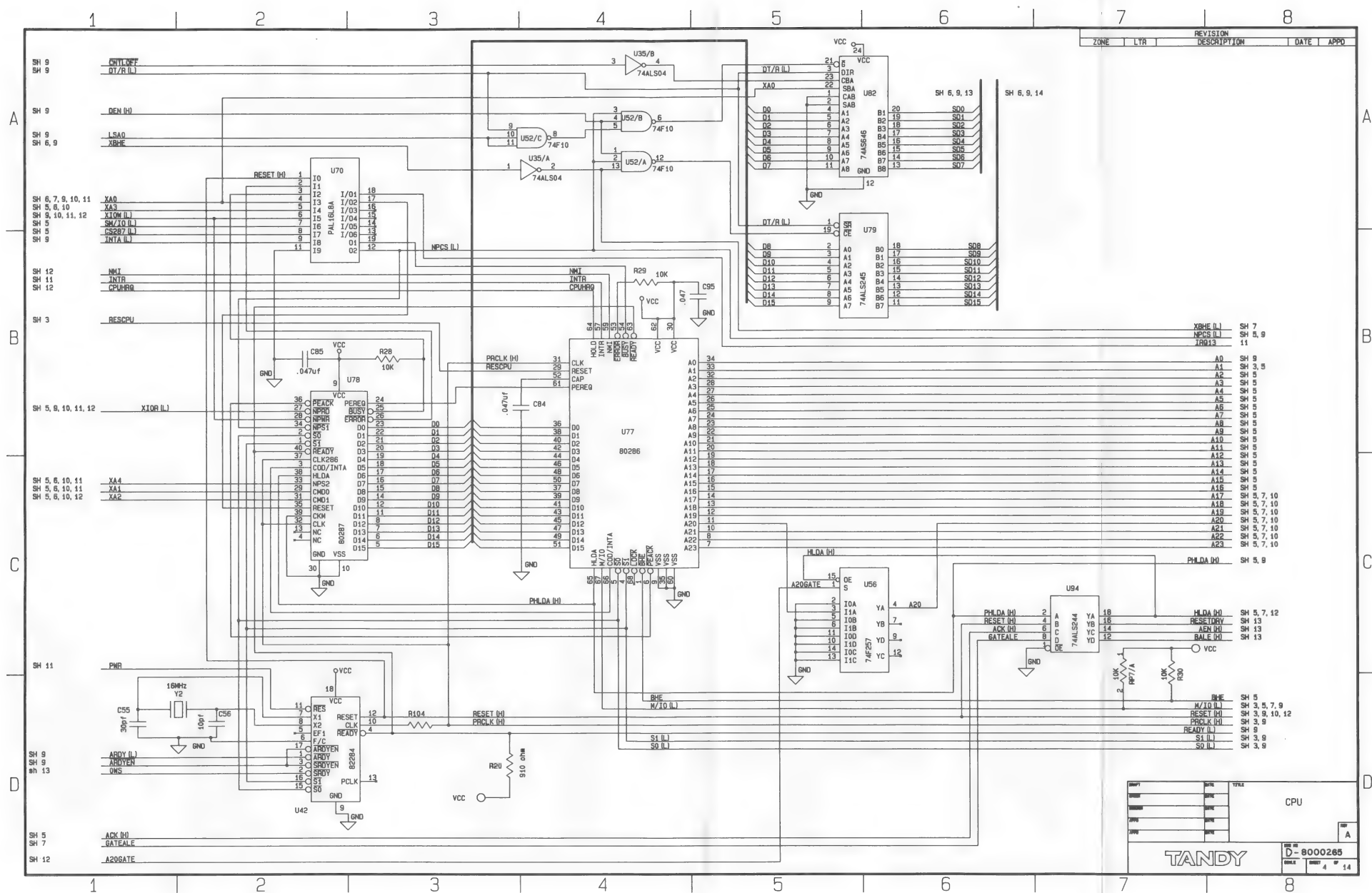
Tandy 3000

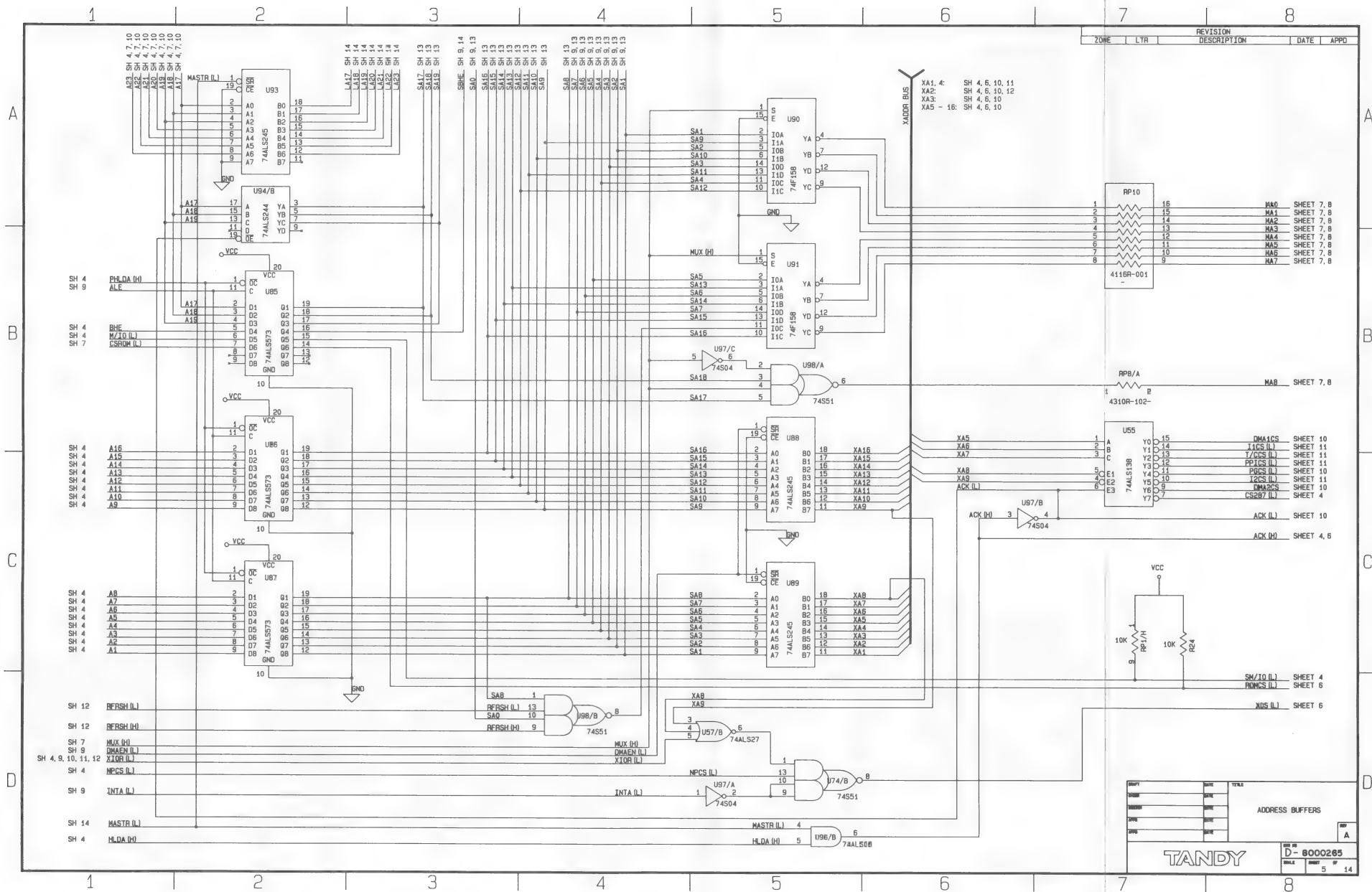
Chassis Subassembly

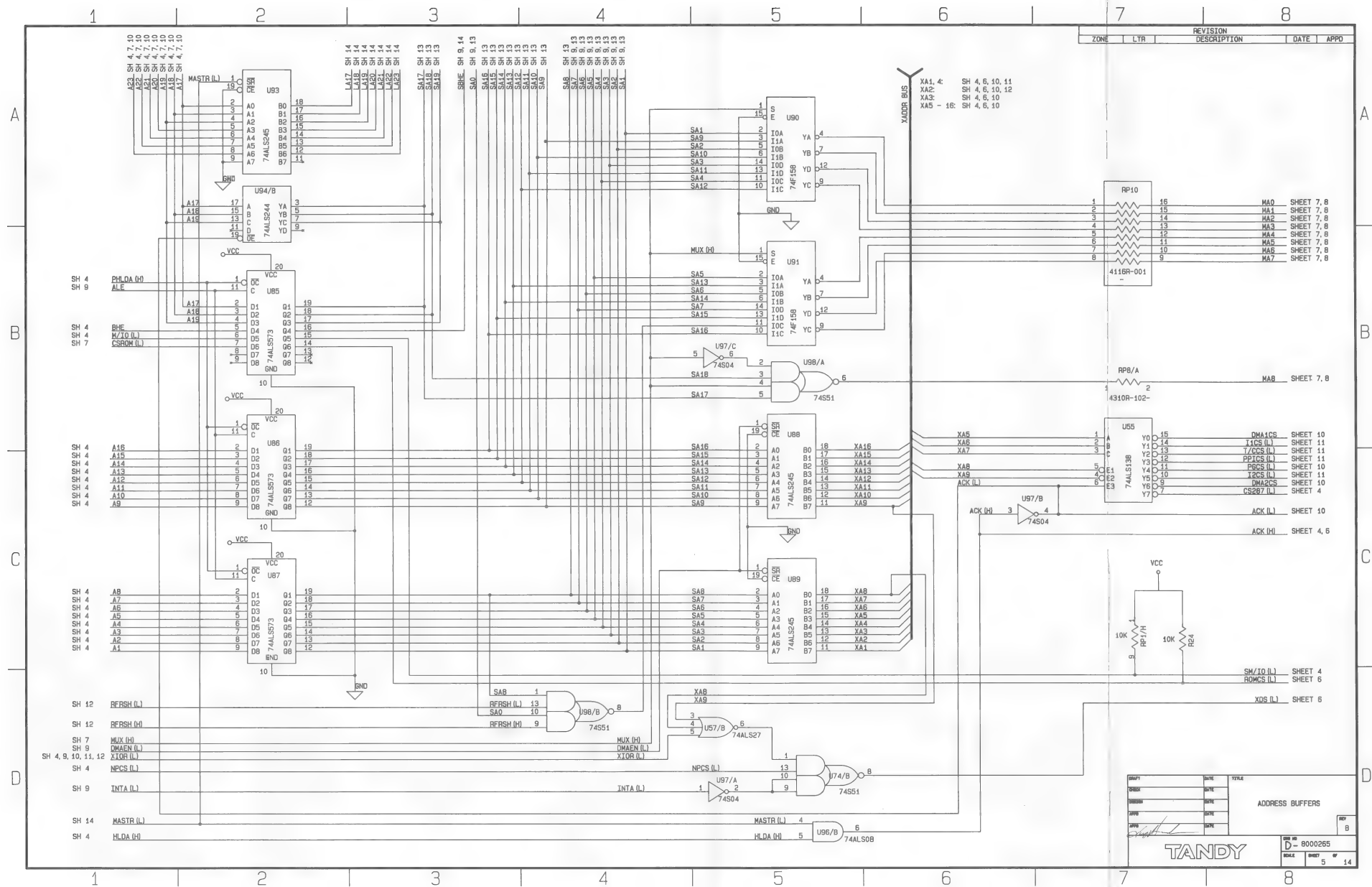
Item	Quan	Description	Part No.
1	1	Weldment, Chassis, Main	AZ-1002
2	1	Chassis, Main	
3	1	Support, Rear, Option Card	
4	1	Panel, Connector, Keyboard	
5	1	Bracket, Card Support	
6	1	Support, Front, Option Card	AHC-0191
7	4	Clip	8559073
8	7	Panel, Option Slot Cover	AZ-1010
9	1	Panel, Serial/Parallel	AZ-1004
10	1	Panel, Memory	AZ-1008
11	5	Feet	AF-0010
12	1	Fan Assembly, DC 12V	AM-4026
13	1	Connector	AJ-1080
14	2	Pins	AJ-1081
15	1	Filter, Fan	AHC-0190
16	4	Screw, #6-32 x 1/2	AHD-1815
17	4	Nut, Keps #6	AHD-7159
18	1	Loop, 5/8" x 3", White	
19	1	Hook, 5/8" x 1", White	
20	1	Speaker	AS-4001
21	1	Cable, Speaker	
22	15	Screw, #6-32 x 5/16 High Performance Thread Forming W/Torque Setting Serrations	AHD-2746
24	7	Screw, #6-32 x 1/4 H.P. Thread Form.	AHD-2618
25	3	Rivet	
26	1	Cable, Floppy Signal	AW-1066
27	1	Guide, Card, Option	ART-0204
28	1	Guide, Air Flow	
29	1	Battery Assembly, 6V	ACS-0020
30	1	Panel, Option Bd. Multiuser	
31	1	Clamp, Multiuser	

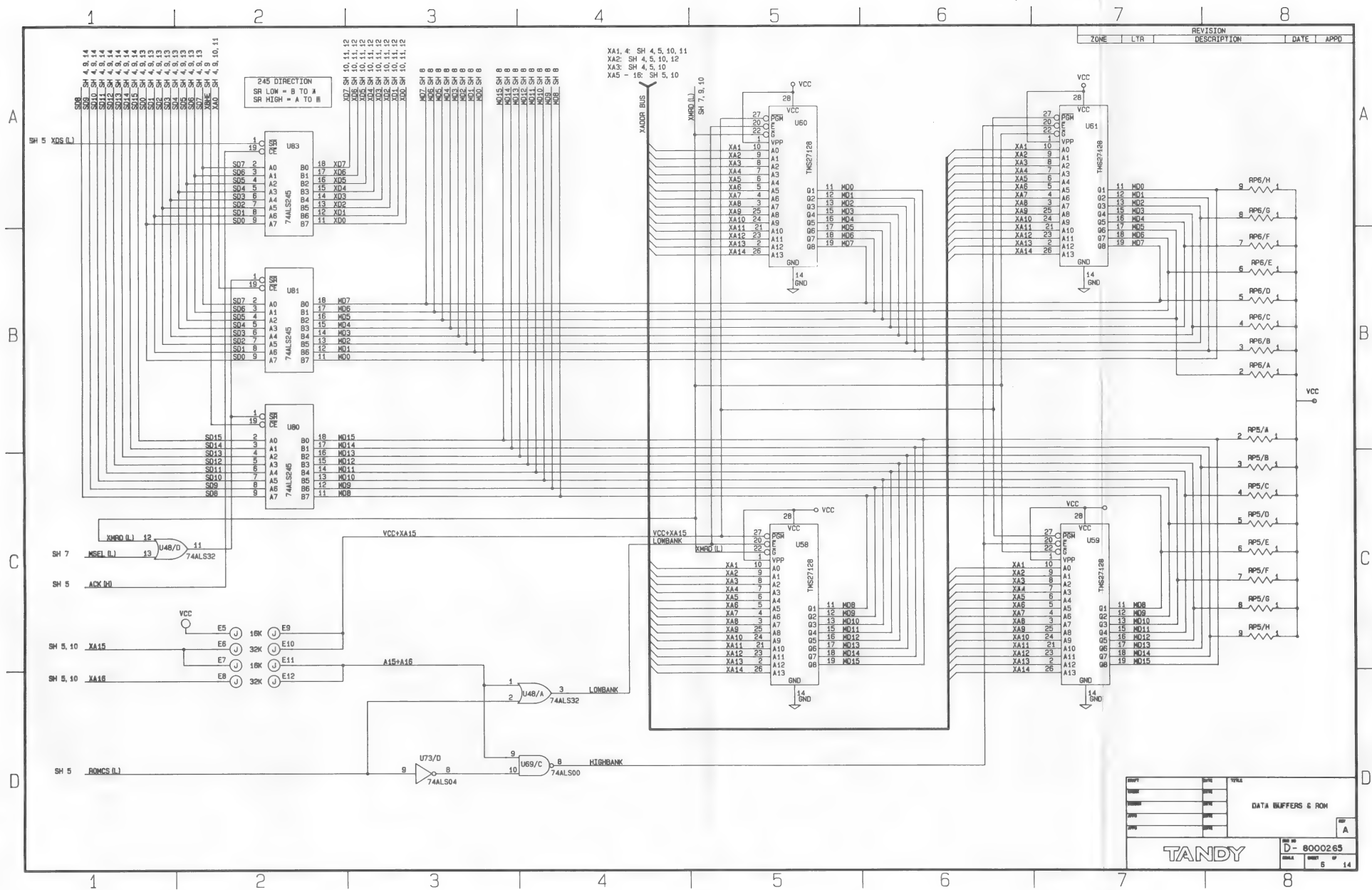


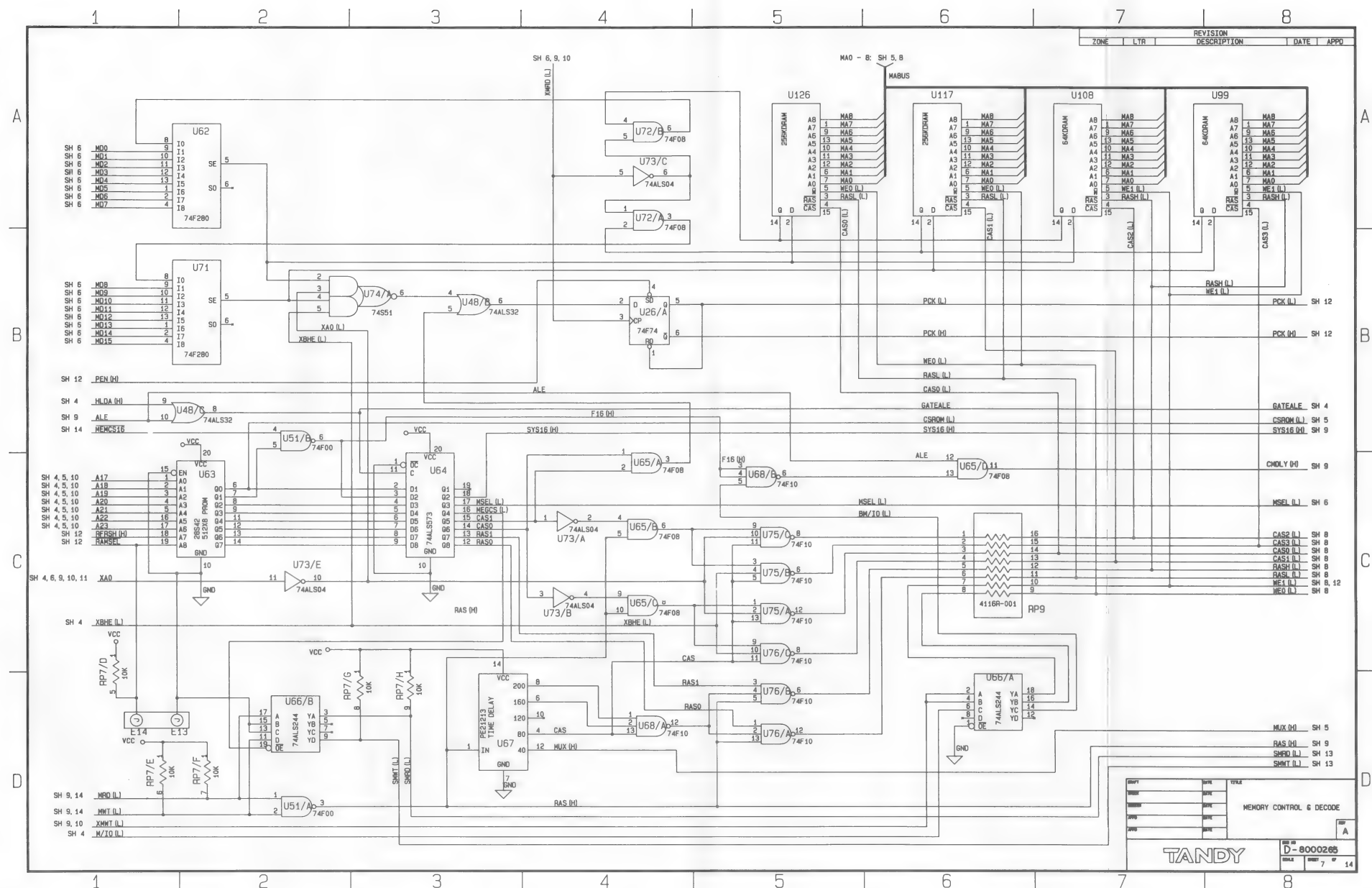


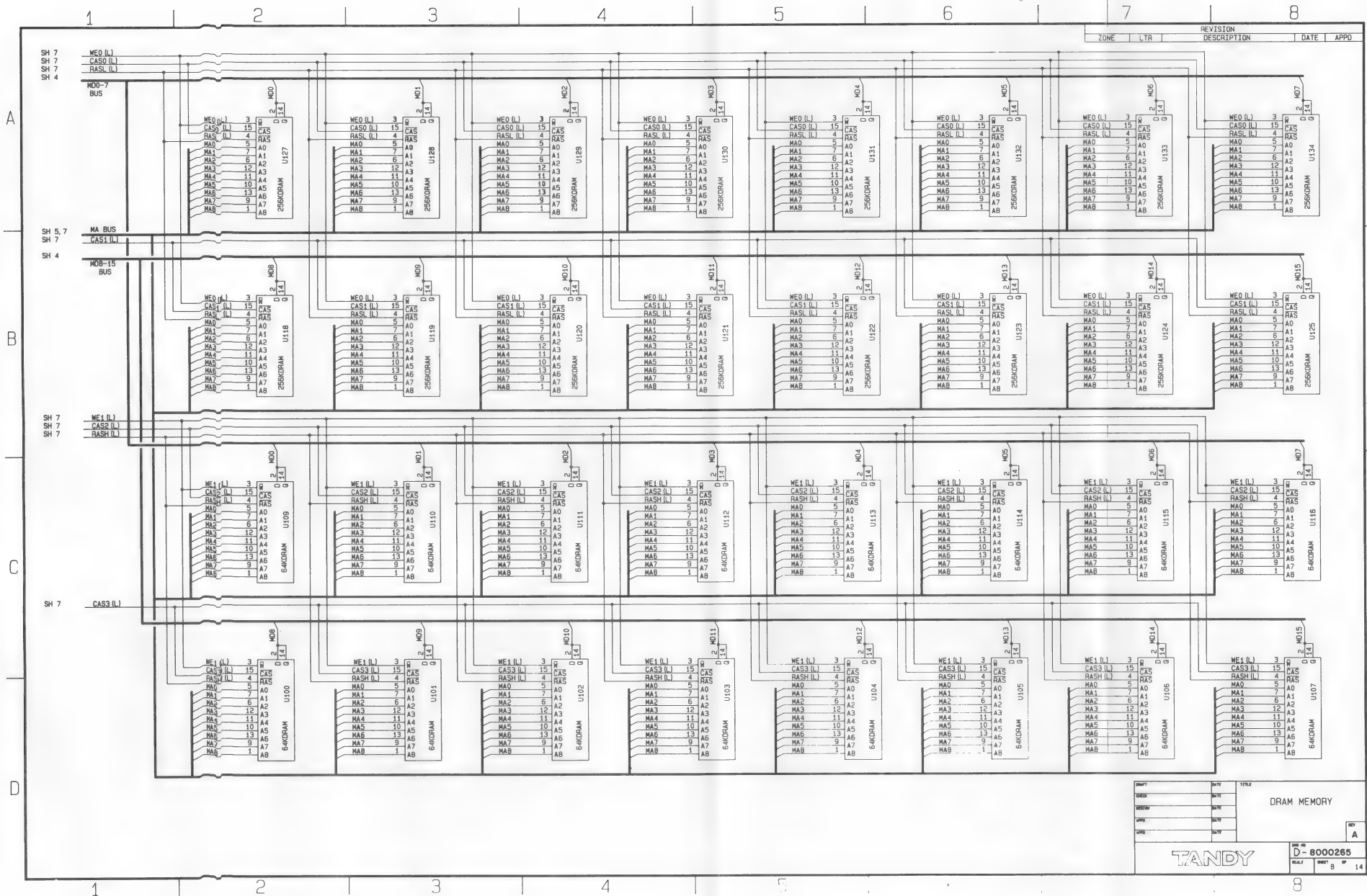




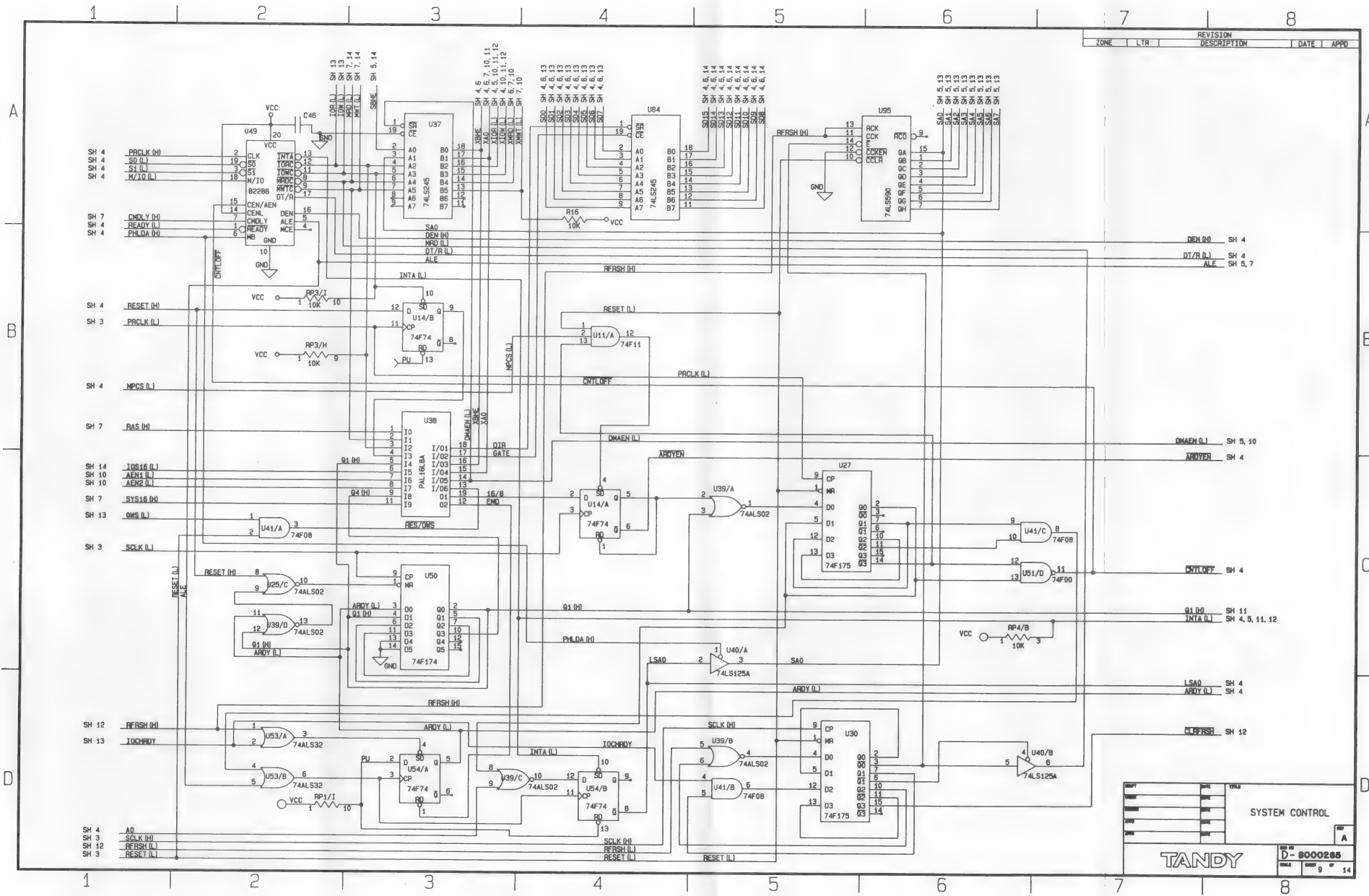








REVISION				
ZONE	LTH	DESCRIPTION	DATE	APPD



SYSTEM CONTROL
FORM A

TANDY
D-8000285

DATE
REV

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2

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4

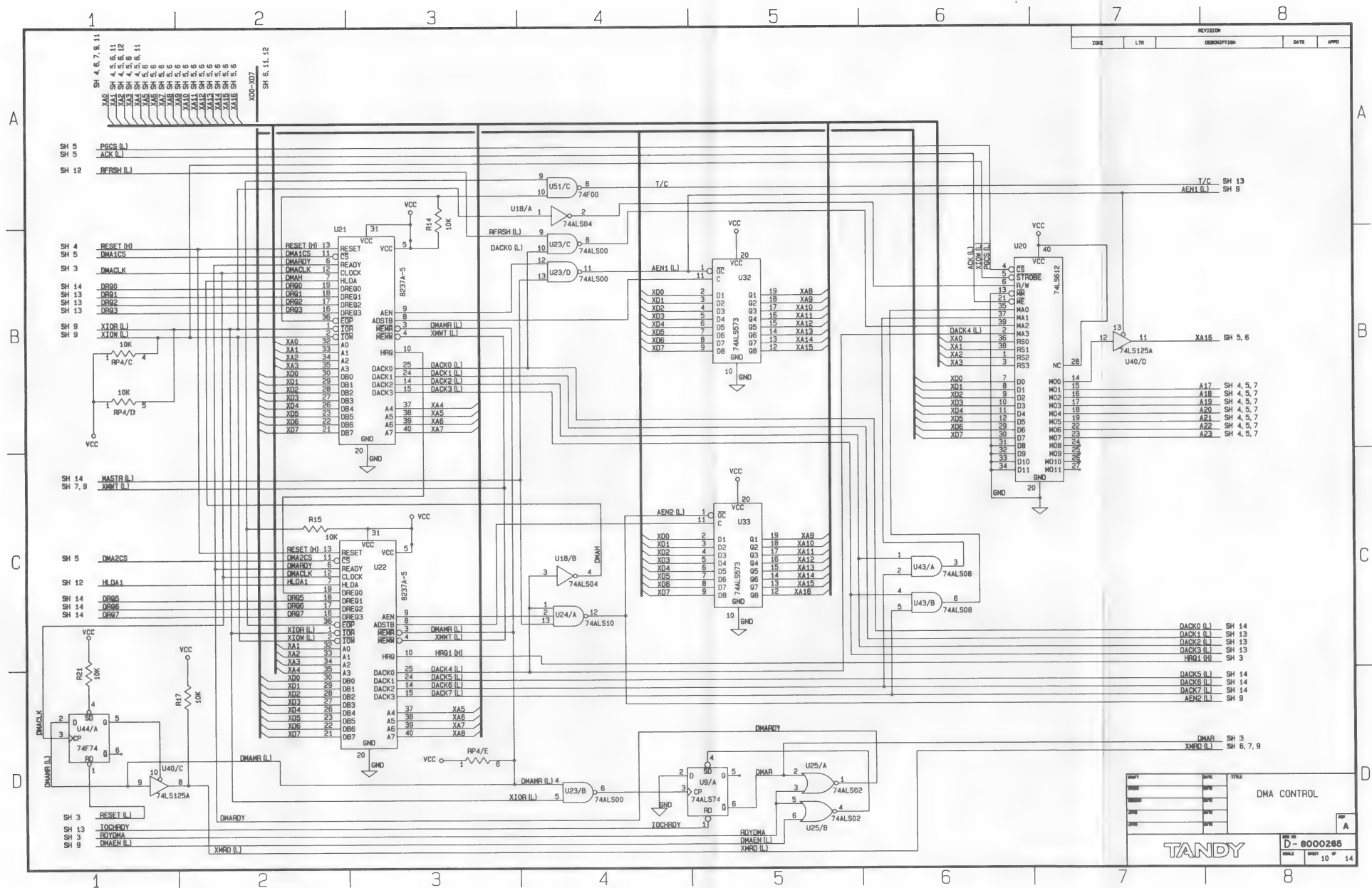
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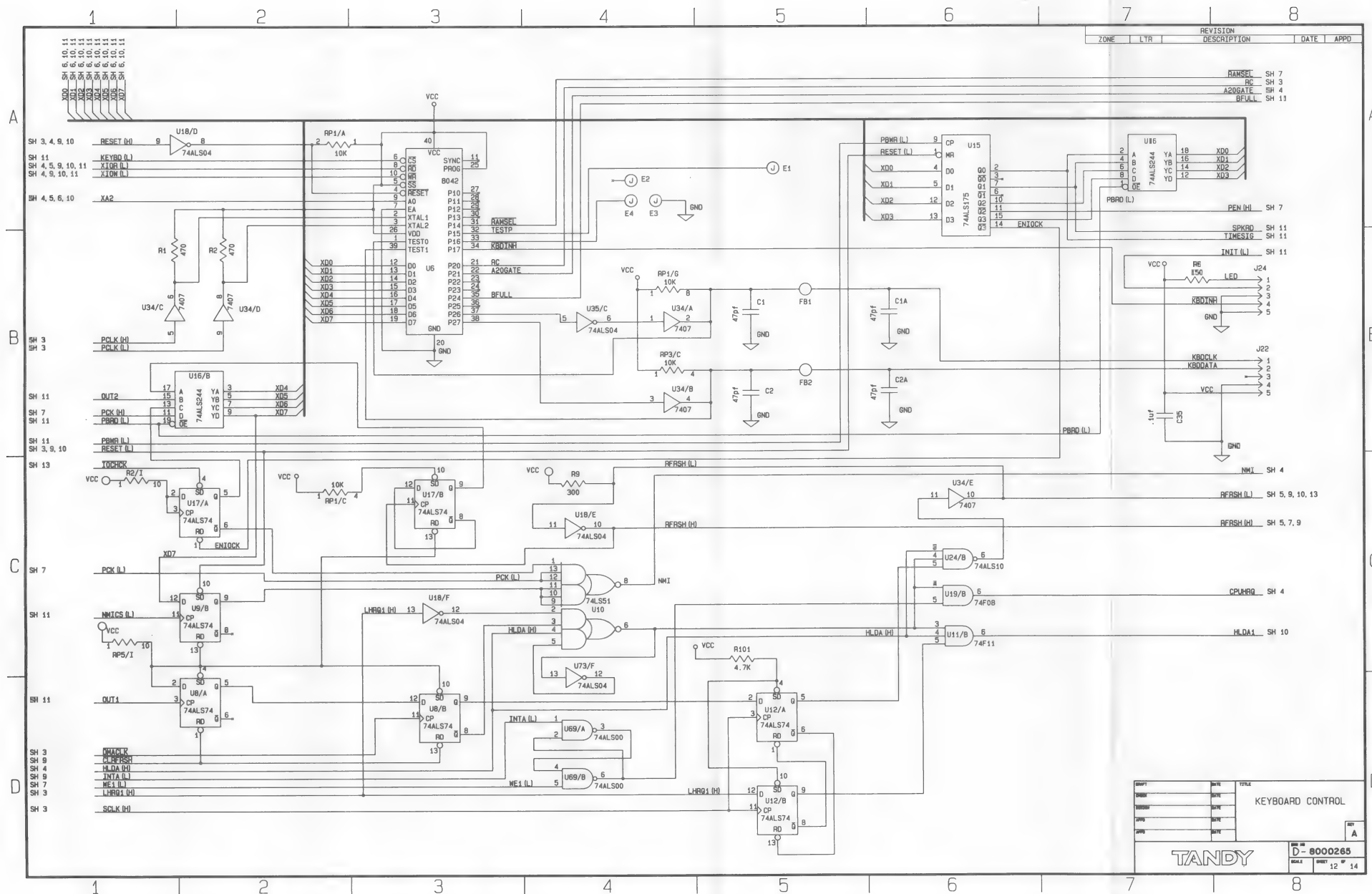
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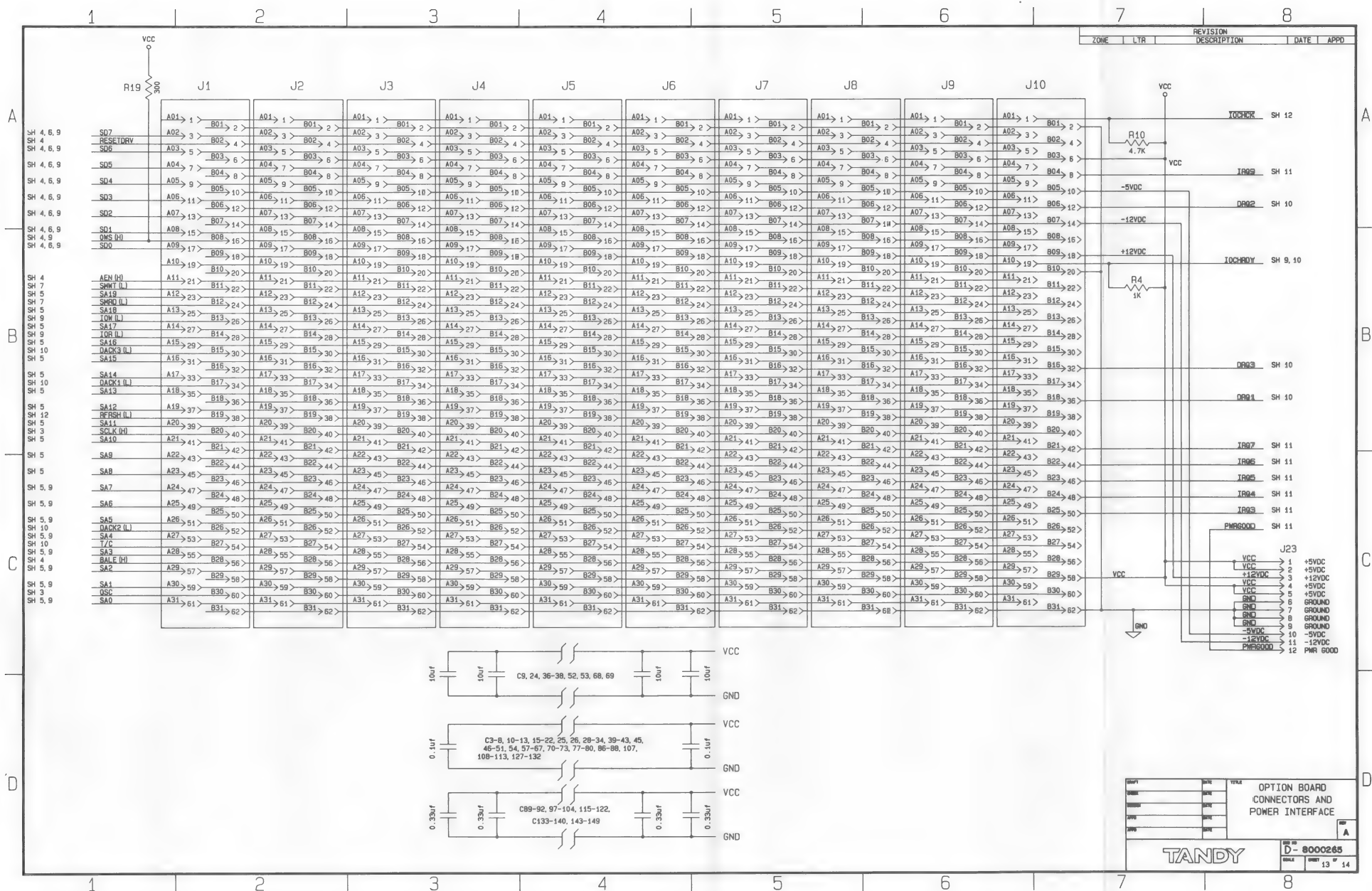
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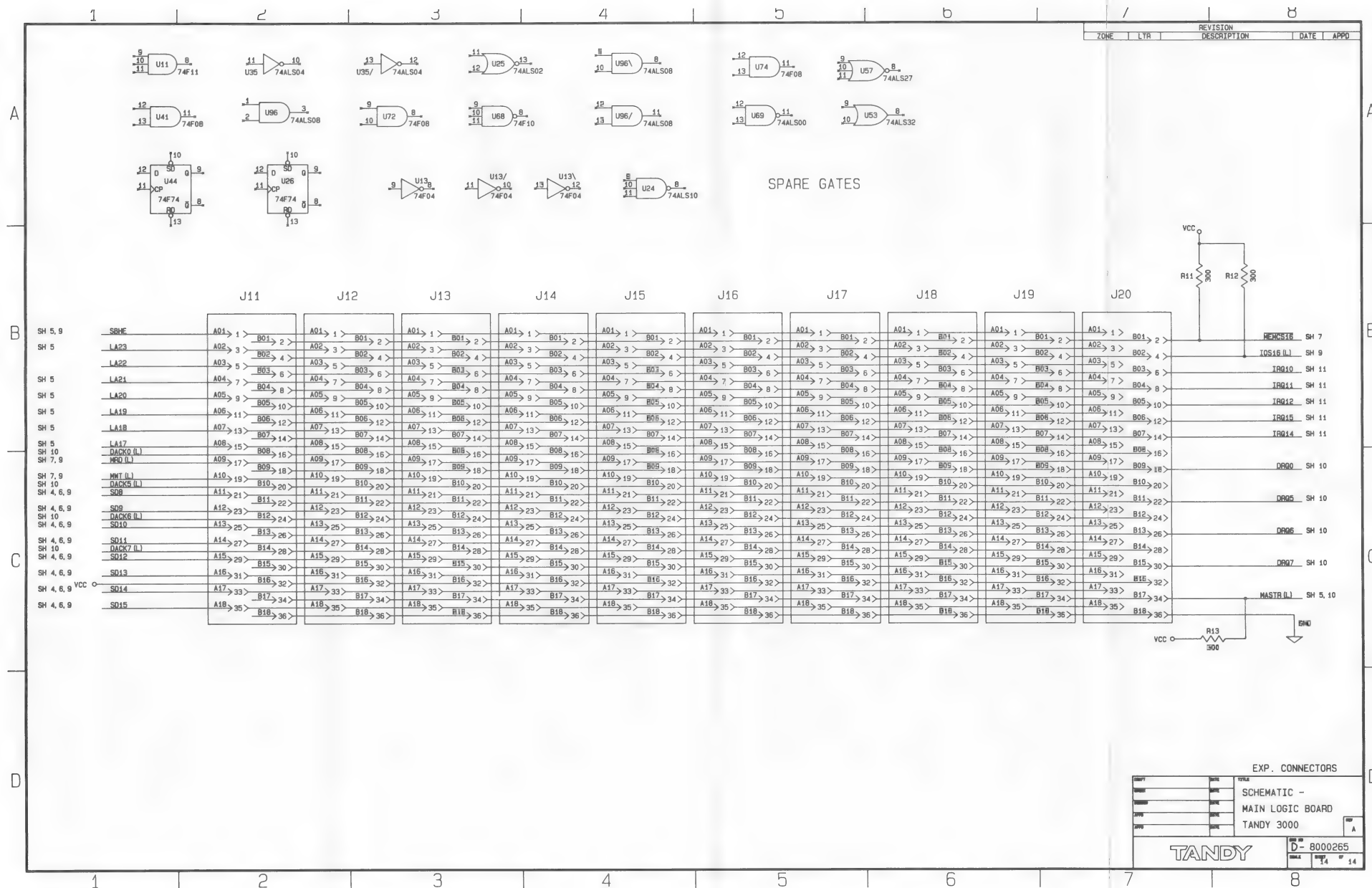
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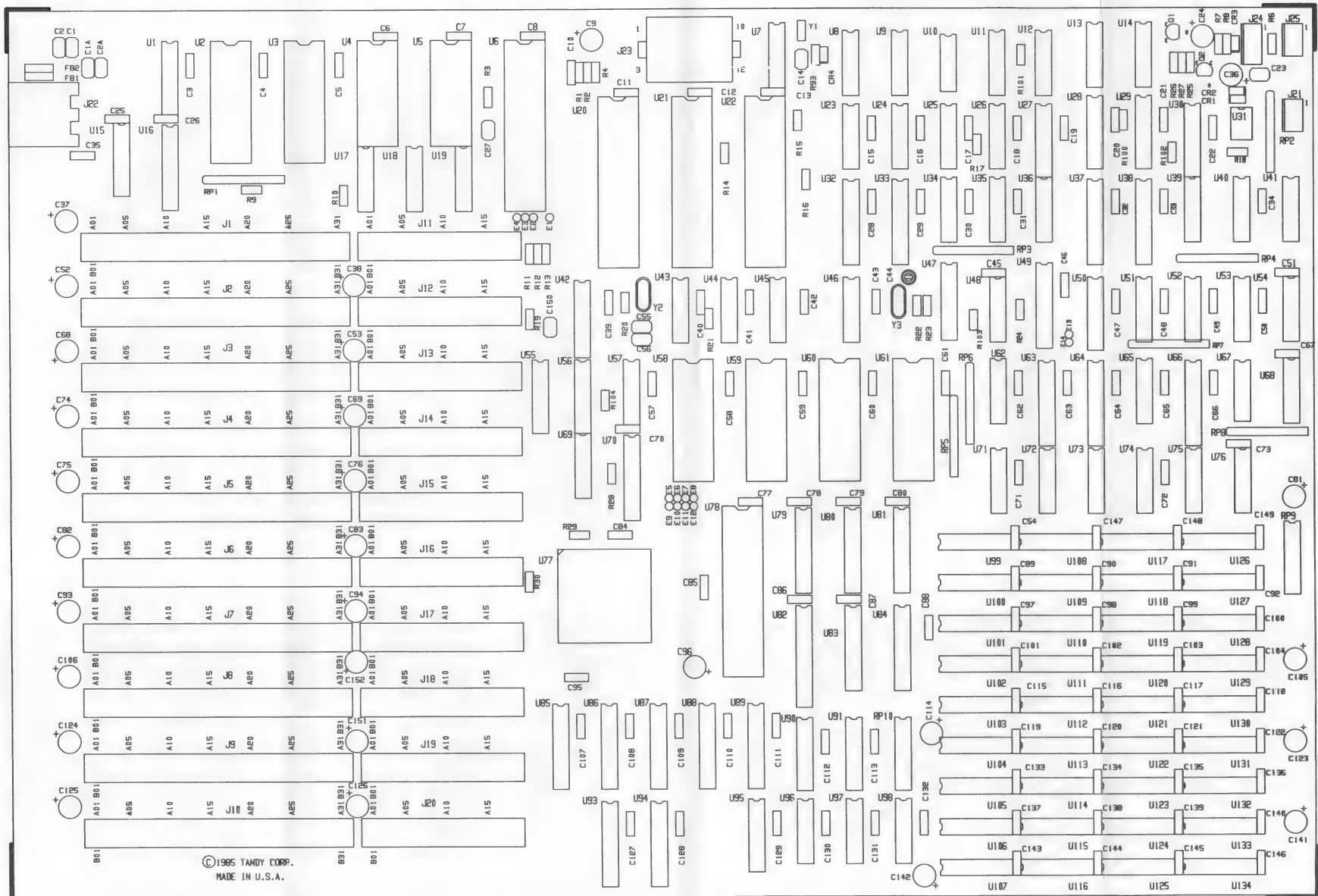
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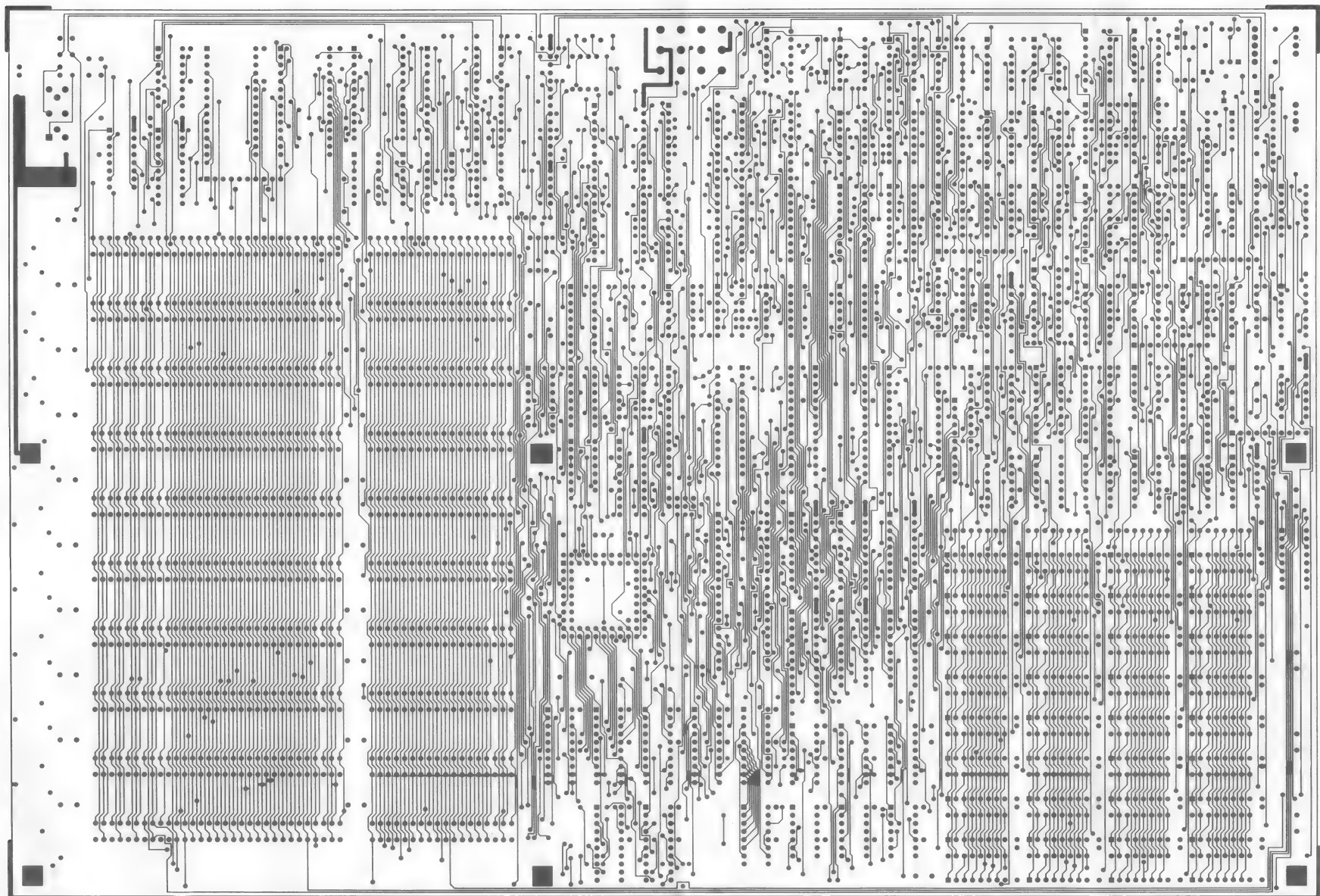


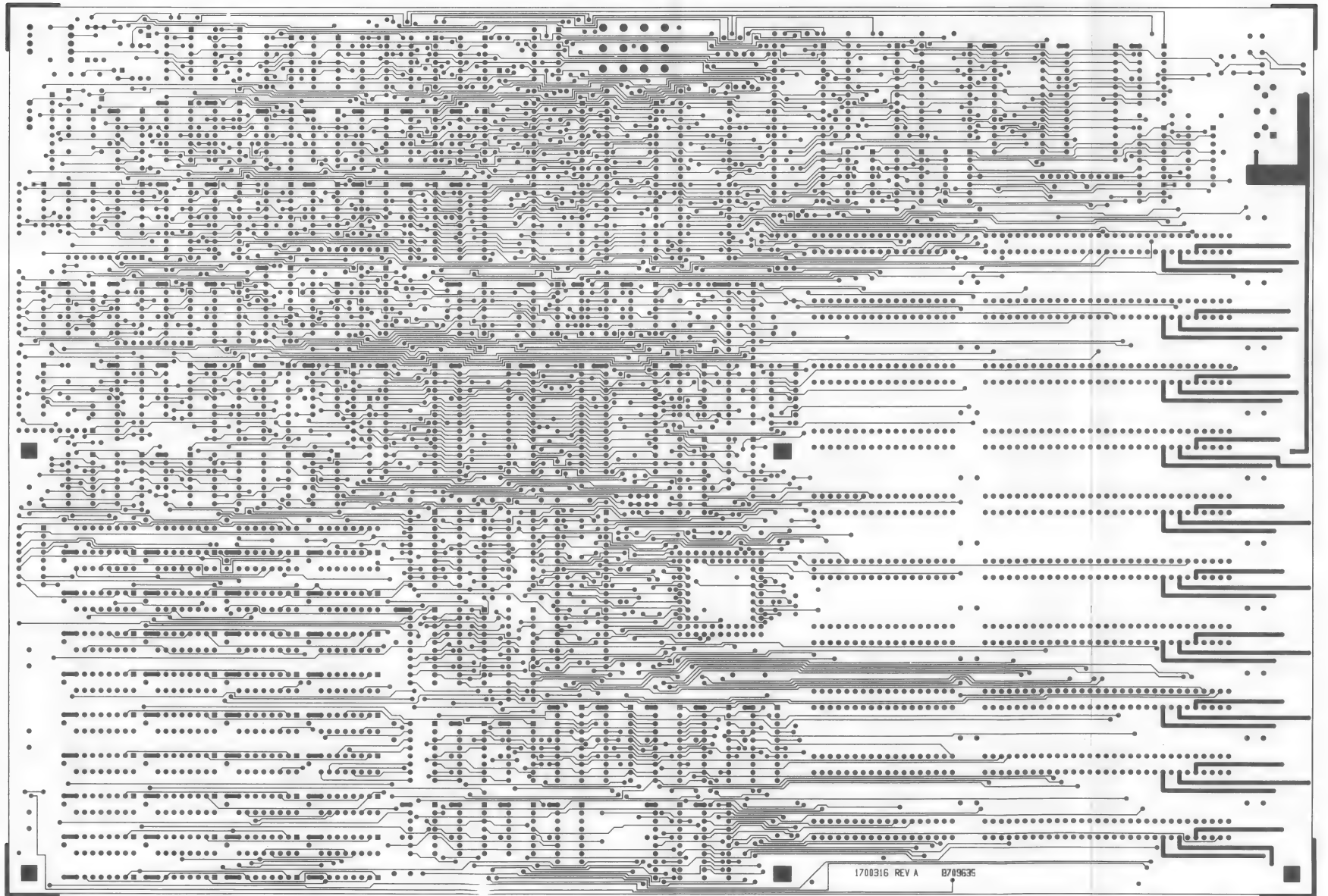


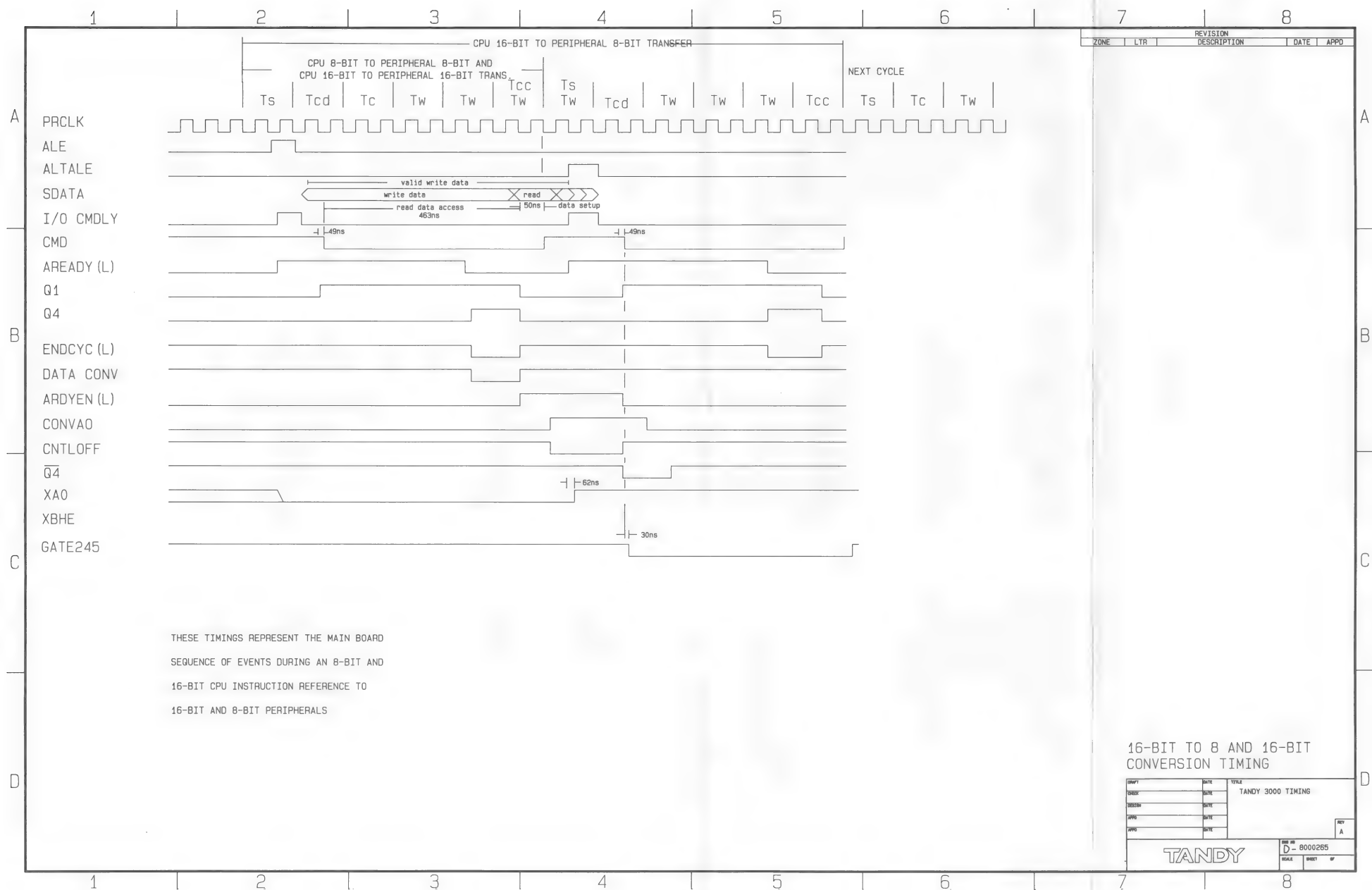


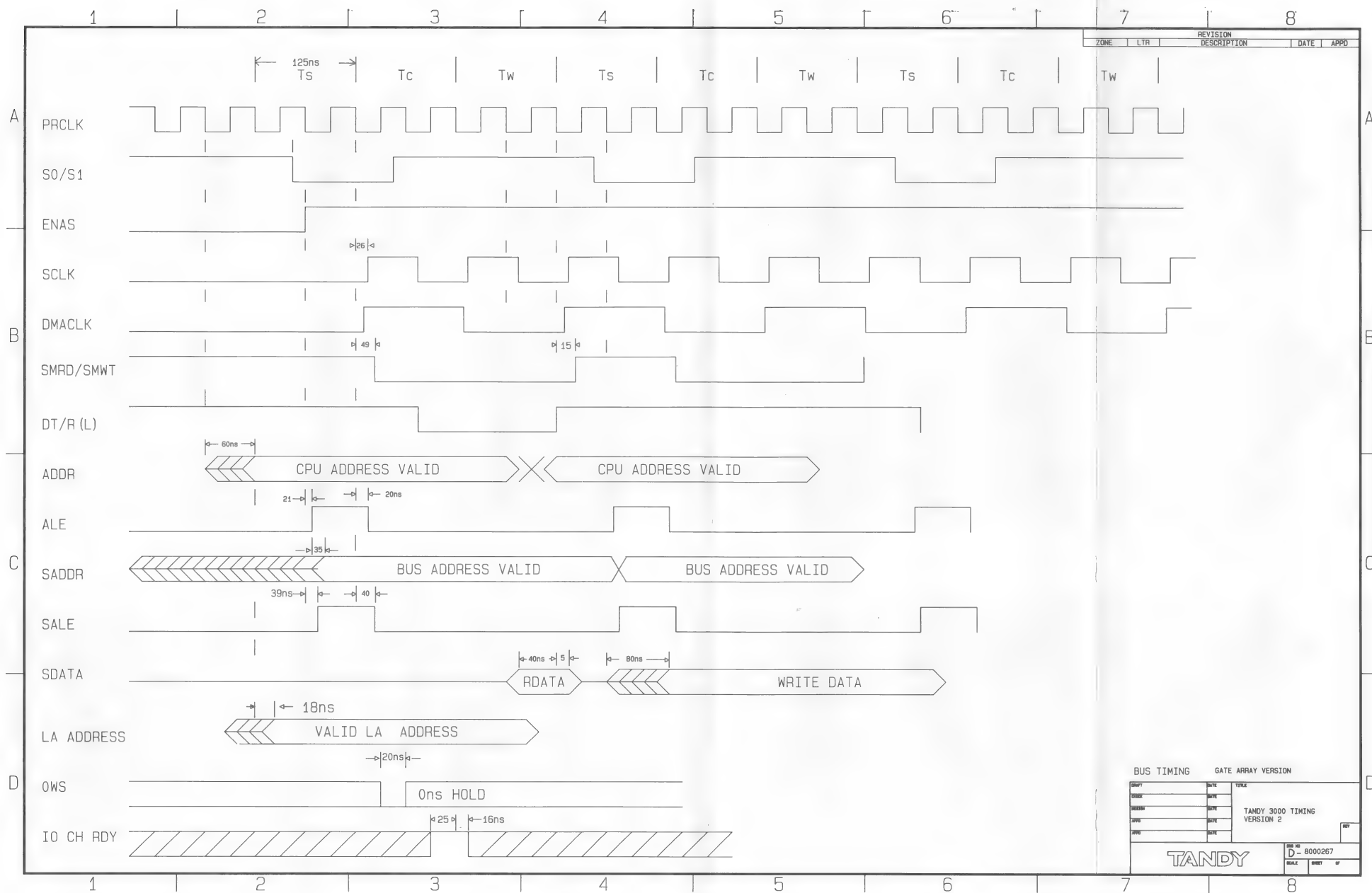


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BUS TIMING		GATE ARRAY VERSION	
DATE	TIME	DATE	TIME

TANDY 3000 TIMING
VERSION 2

TANDY

REV NO: D-8000267
SCALE: SHEET 1 OF 1

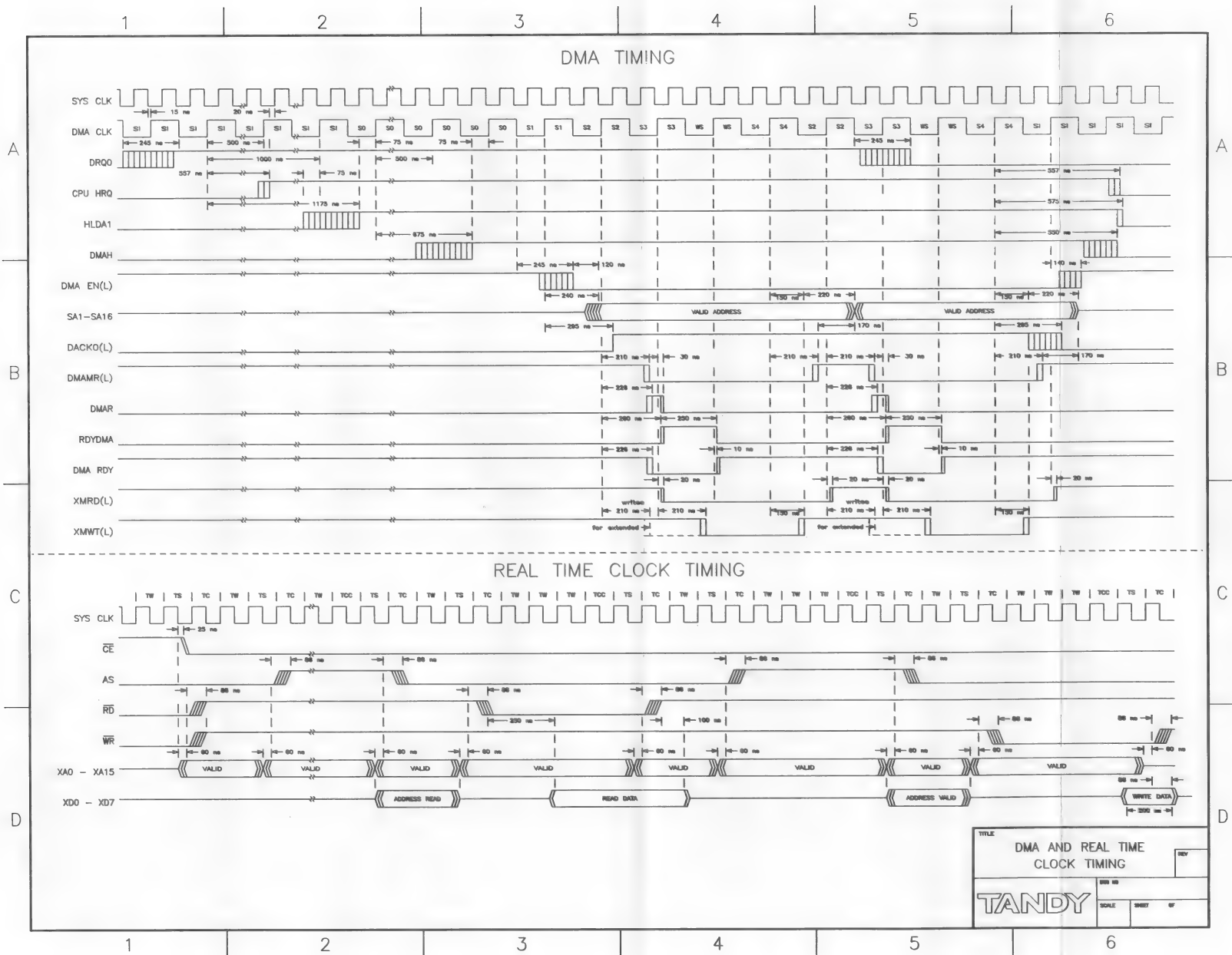


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4. Keyboard Buffer
5. Power-on-Reset
6. Basic Assurance Test
7. Commands
8. Keys

II. Schematics

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I. KEYBOARD THEORY OF OPERATION

1 Description

The TANDY Model 3000 system keyboard is a Low profile, 84 key, detachable, IBM-AT compatible keyboard, using an 8049 microprocessor, clocked by a 6 MHz crystal oscillator.

2 Interface

The keyboard has a bidirectional serial interface through a 5 pin DIN connector (pin 1 = clock, pin 2 = data, pin 3 = spare, pin 4 = ground, and pin 5 = +5 VDC; see Figure 5).

CLOCK AND DATA SIGNALS: When the keyboard sends data to the system through the 8049's P16 (see keyboard schematic), or receives commands through the 8049's INT* line, it generates the clock signal through P17 to time the data; the system can prevent the keyboard from sending by forcing the clock line to a logic 0 level, sensed on the 8049 T1 input. During basic assurance test, the keyboard allows the clock and data lines to go to a logic 1 level. Data/command transmission from/to the keyboard consists of 11-bit serial data streams; bit 1 = 0 start bit, bits 2 thru 9 = data bits 0 thru 7, bit 10 = odd parity bit, and bit 11 = stop bit.

KEYBOARD DATA OUTPUT: When the clock and data lines are both high (this is a request to transmit from the keyboard), the keyboard sends the 11 bit serial transmission; data will be valid before the falling edge, and beyond the rising edge of the clock (see Figure 2). The clock line is checked for a logic 1 level at least every 60 milliseconds, and if it goes low before the 10th bit is sent (system override has occurred), the keyboard buffer returns the data and clock lines to a logic 1 level, otherwise, the transmission is completed. When the clock line is low, data is stored in the keyboard buffer, otherwise, the keyboard is either idle or receiving data or commands.

KEYBOARD DATA INPUT: When the clock line is high and the data line is low (this is a request to send to the keyboard; see Figure 3), the keyboard will count 10 bits and then force the data line low and will count one more bit (this action signals the system that the keyboard has received its transmission; the clock line will be checked for a low level no less than 60 millisecond intervals by the keyboard. Each transmission to the keyboard requires a response from the keyboard before the next communication can take place; the keyboard will respond within 20 milliseconds, unless prevented by a held-lo clock signal from the system. If the keyboard response is invalid or has a parity error, the system sends the command or data again; a resend command should not be sent in this case.

3 Sequencing Key Code Scanning

Based on the programmed 8049 counter outputs (P20-P22), the keyboard detects all keys pressed through the 8049 DB0-DB7 and P24-P26 inputs, and sends their scan codes to the interface in correct sequence, regardless of the number of keys held down (keystrokes entered while the interface is inhibited will be lost, and not stored; see Figures 6-7).

4 Keyboard Buffer

The keyboard has a 16 character FIFO buffer contained in 8049 RAM (the 17th key stroke will be replaced with the overrun code 00H, and additional keystrokes will be lost).

5 Power on Reset

This function has an operational time span of a minimum of .3 seconds, and a maximum of .9 seconds, asserted at Pin 4 of the 8049.

6 Basic Assurance Test

This function is executed immediately after the power on reset, and lasts for .6 to .9 seconds; a successful test will send a AAH to the system, and an unsuccessful test will send FCH. The successful test defaults to typematic and make/break mode.

7 Commands

RESET (FFH): The keyboard acknowledges a reset by raising the clock and data lines for a minimum of 500 microseconds (the keyboard is disabled from the reset until the acknowledge is accepted or until another command overrides the reset), and then perform a basic assurance test.

RESEND (FEH): The keyboard acknowledges this command by resending the previous output again unless the previous output was a resend, which means it will resend the byte which precedes the resend. The keyboard will issue a resend command following receipt of an invalid input, or any input with incorrect parity.

NO-OPERATION (NOP, FDH thru F7H and F2H thru EFH): These commands are acknowledged, but unused.

SET DEFAULT (F6H): The keyboard responds with an acknowledge, clears its output buffer, sets default conditions, and continues scanning, if the keyboard was previously enabled.

ENABLE (F4H): The keyboard responds with an acknowledge, clears its buffer, and starts scanning.

SET TYPOMATIC RATE/DELAY (F3): The keyboard responds with an acknowledge, stops scanning, waits for the rate parameter, acknowledges the rate parameter, sets the rate and delay, and continues scanning, if the keyboard was enabled. If a command is received instead of the rate parameter, the function ends with no change to the existing rate and the new command is processed; the scanning is disabled.

ECHO (EEH): If enabled, the keyboard responds by issuing a EEH response, and continues scanning.

7 Commands (continued)

SET/RESET MODE INDICATORS (EDH): The keyboard responds with an acknowledge, disables scanning, and waits for the option byte. Upon receipt of the byte, the keyboard responds with an acknowledge, sets the indicators, and continues scanning if the keyboard is enabled. If another command is received in place of the option byte, execution of the function is stopped with no change to the indicator states, and the new command is processed, and scanning is resumed.

ACK (FAH): The keyboard issues an acknowledge response to any valid input other than an echo or resend command; if the keyboard is interrupted, while sending an acknowledge, the acknowledge is discarded and the new command is acted upon.

8 Keys

All keys are classified as make/break, which means when a key is pressed, the keyboard sends a make code, and when released, it sends a make code preceded by FOH (the keys are IBM typematic, which means when held down, they will continue to send make codes until released; only the first make code will be stored in the keyboard buffer). The typematic rate and delay parameter are determined by the value of the byte following the command; bit 7 is always 0, bits 6 and 5 serve as the delay parameter (delay = 1 plus the binary value of bits 6 and 5 multiplied by 250 milliseconds $\pm$ 20 %), and bits 4 thru 0 are the rate parameter as shown in the table below.

<u>BIT</u>	<u>RATE</u>	<u>BIT</u>	<u>RATE</u>	<u>BIT</u>	<u>RATE</u>	<u>BIT</u>	<u>RATE</u>
00000	30.0	00100	20.0	01000	15.0	01100	10.0
00001	26.7	00101	18.5	01001	13.3	01101	9.2
00010	24.0	00110	17.1	01010	12.0	01110	8.6
00011	21.8	00111	16.0	01011	10.9	01111	8.0
10000	7.5	10100	5.0	11000	3.7	11100	2.5
10001	6.7	10101	4.6	11001	3.3	11101	2.3
10010	6.0	10110	4.3	11010	3.0	11110	2.1
10011	5.5	10111	4.0	11011	2.7	11111	2.0

8 Keys (continued)

KEY SCAN CODES: Each key is assigned a unique 8 bit, make, scan code, which is sent when the key is pressed; the following table and figure indicate the key number scan code. (See the keyboard layout and code table for appropriate key position, and the keyboard section of the design detail specification for translated system codes.)

<u>KEY</u>	<u>CODE</u>	<u>KEY</u>	<u>CODE</u>	<u>KEY</u>	<u>CODE</u>	<u>KEY</u>	<u>CODE</u>	<u>KEY</u>	<u>CODE</u>	<u>KEY</u>	<u>CODE</u>
1	0E	15	66	30	14	46	1A	65	06	95	77
2	16	16	0D	31	1C	47	22	66	0C	96	75
3	1E	17	15	32	1B	48	21	67	0B	97	73
4	26	18	1D	33	23	49	2A	68	0A	98	72
5	25	19	24	34	2B	50	32	69	09	99	70
6	2E	20	2D	35	34	51	31	70	05	100	7E
7	36	21	2C	36	33	52	3A	71	04	101	7D
8	3D	22	35	37	3B	53	41	72	03	102	74
9	3E	23	3C	38	42	54	49	73	02	103	7A
10	46	24	43	39	4B	55	4A	74	01	104	71
11	45	25	44	40	4C	57	59	90	76	105	7F
12	4E	26	4D	41	52	58	11	91	6C	106	7C
13	55	27	54	43	5A	61	29	92	6B	107	7B
14	5D	28	5B	44	12	64	58	93	69	108	79

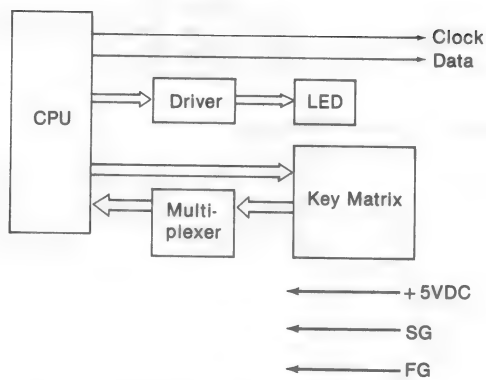


Figure 1 Keyboard Block Diagram

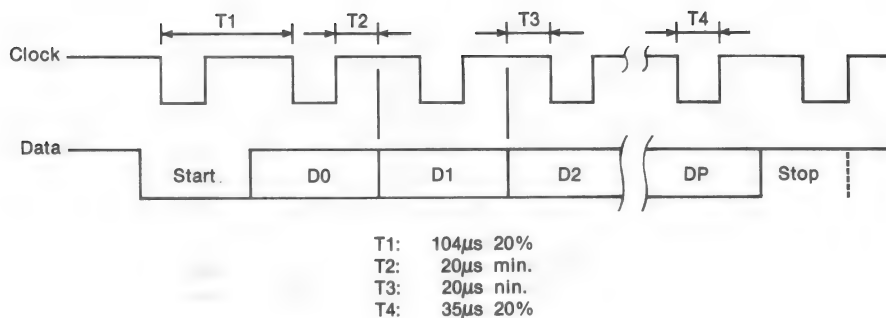


Figure 2 Keyboard Data Output

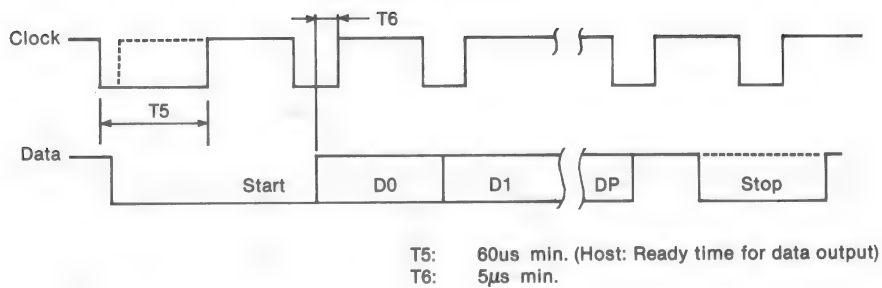


Figure 3 Keyboard Data Input

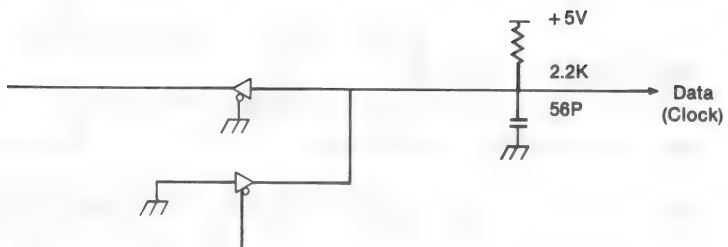


Figure 4 Interface Circuit Specification

NO	SIGNAL
1	CLOCK
2	Data
3	
4	Ground (SG)
5	5 Vdc
—	Ground (FG)

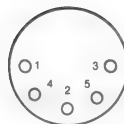


Figure 5 DIN Connector

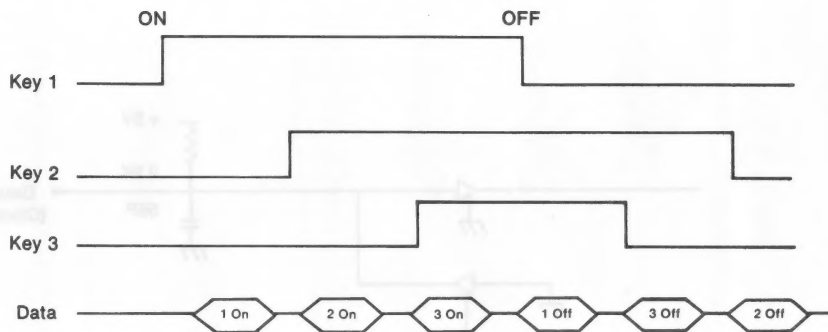


Figure 6 Key Code Sending Sequence

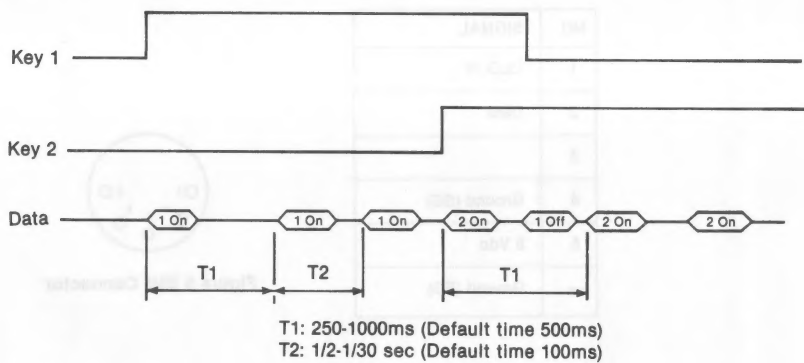
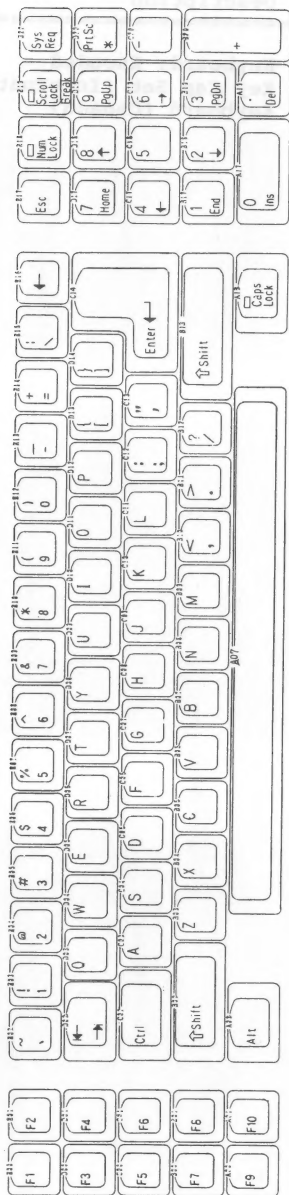


Figure 7 Typematic Cycle

CODE TABLE

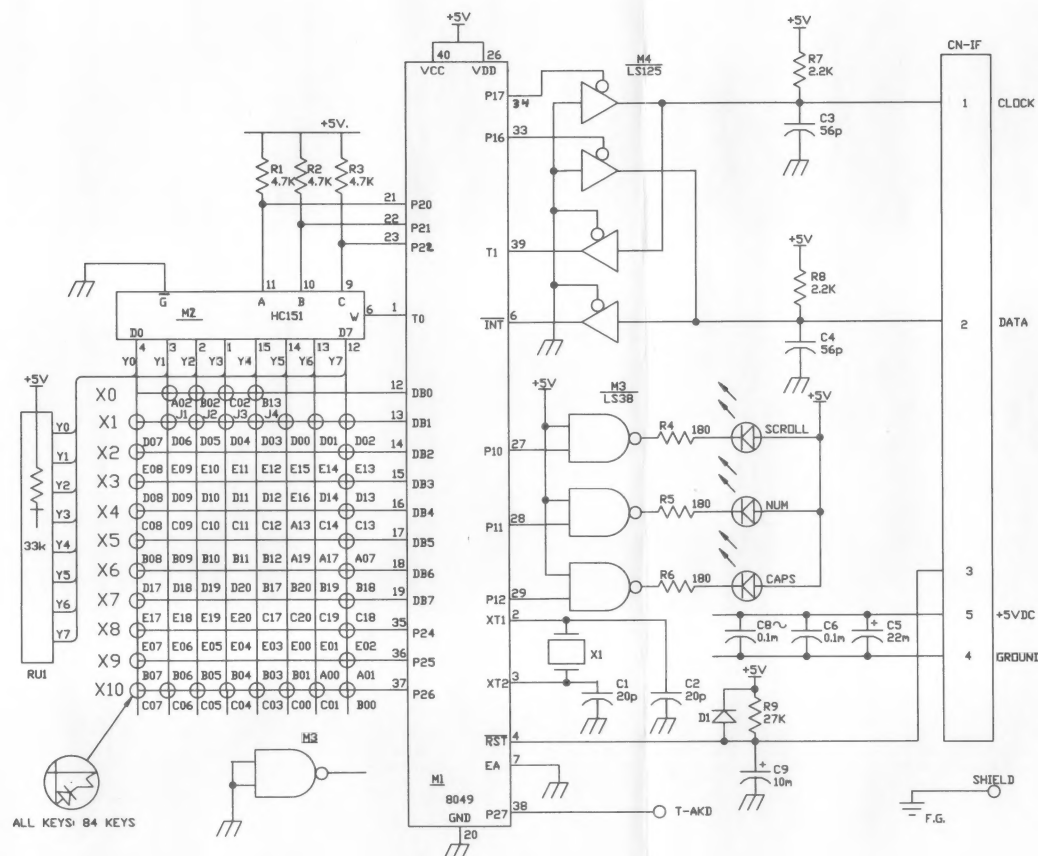
[illegible]

ROW



Keyboard Subassembly

=====			=====
Item	Quan	Description	Part No.
=====			=====
1	1	Keyboard, Encoded	AXX-0244
2	1	Key Cap Set (International)	8590202
3	1	Keyboard (Canada)	8790559



NOTES:

"REFERENCE DRAWING"

MATERIAL	UNLESS OTHERWISE SPECIFIED TOLERANCES	BY	BRAD LEPLEY	DATE	10-9-80	TITLE SCHEMATIC- CIRCUIT KEYBOARD FWITSU				
		CHECK		DATE						
		DESIGN		DATE						
		APPD		DATE						
FINISH	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING DO NOT SCALE THIS DRAWING					DRAWING NO. 8000270				
							SCALE	SHEET	1	OF
TANDY										
629										
USED ON										