TANDY®

Service Manual

25-1001

Tandy 1000® HD
Service Manual

Cat. No. 25-1001

Supplement to the Tandy® 1000
Service Manual

(Cat. No. 25-1000)

CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

Tandy 1000®HD
Service Manual
(Cat. No. 25-1001)

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Service Manual
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Tandy 1000®HD Service Manual

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WD10025-WX2 15

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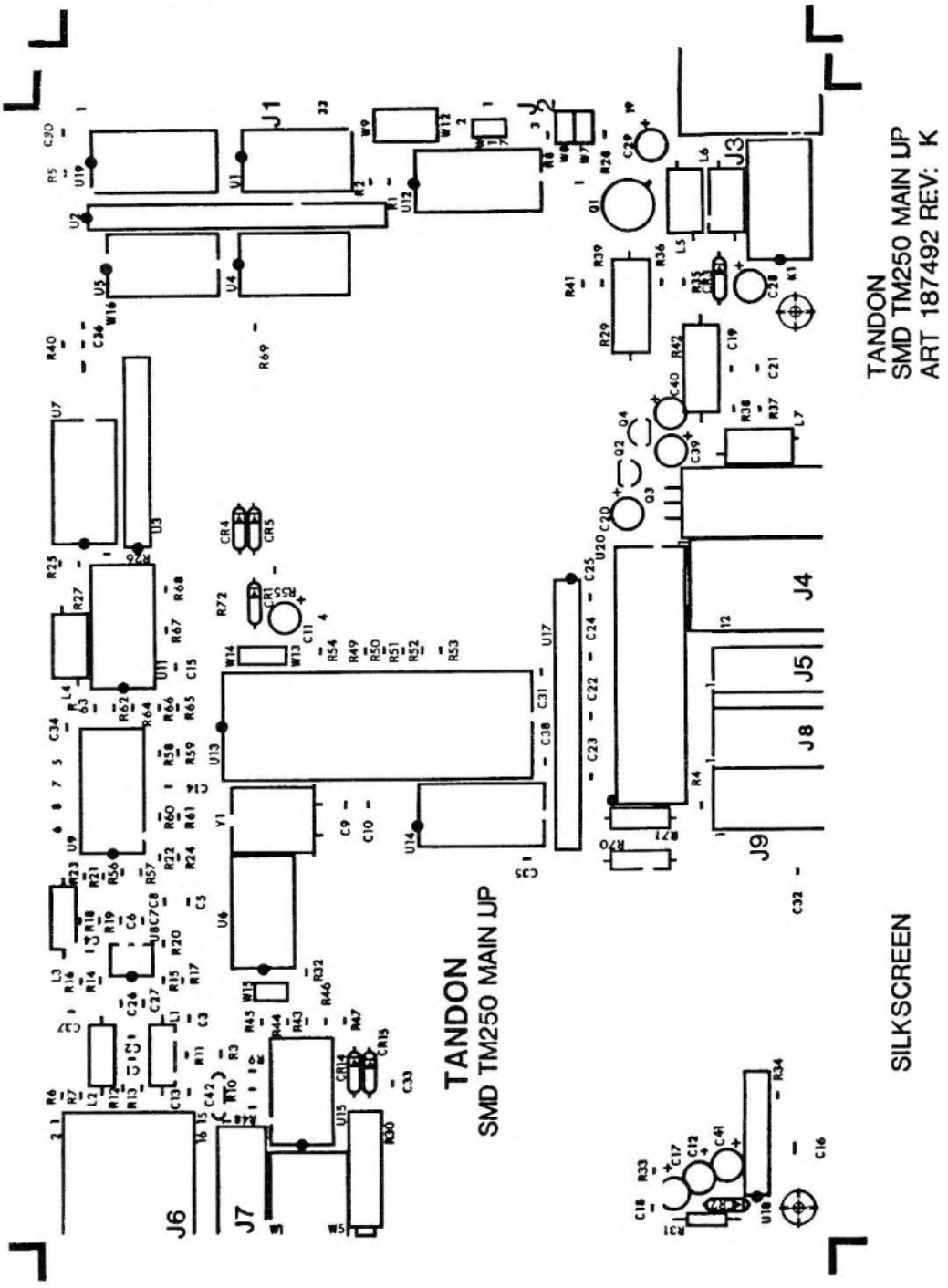
Component Information 39

TM252 Rigid Disk Drive
WD1010-05 Winchester Disk Controller
WD1002S-WX2 Winchester Disk Controller OEM Manual
WD10C20 Read/Write Channel Device
WD1015 Buffer Manager Control Processor
WD1015-14 Specification
WD1100-17 Logic Gate Array

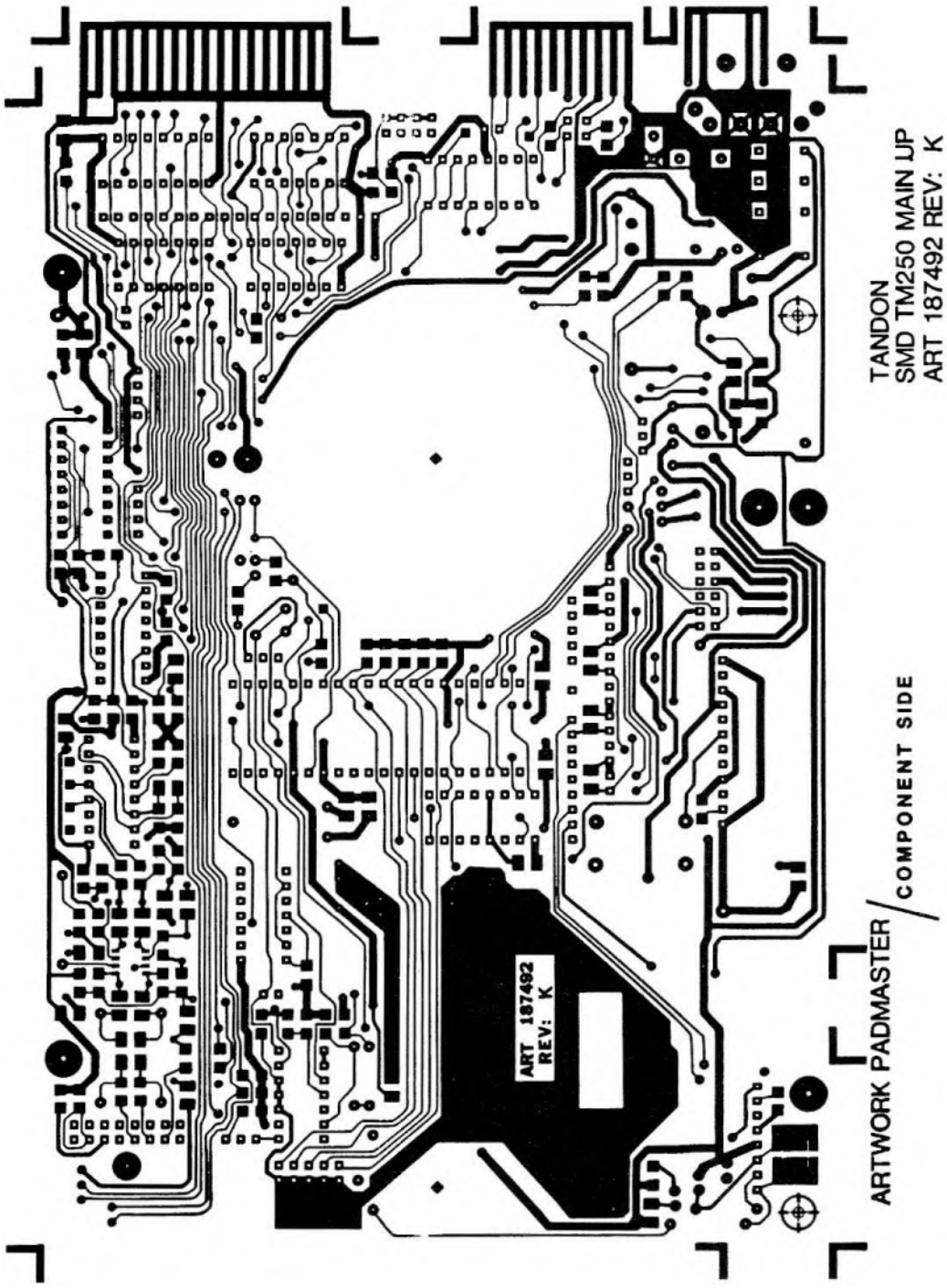
Introduction

This manual covers the service information for the internal hard disk drive on the Tandy 1000 HD. Included in this manual is information concerning the original main logic board used with the Tandy 1000 HD. If you are servicing a computer equipped with the **cost reduction main logic board,** consult the addendum on the cost reduction version of the Tandy 1000 (25-1000A) for information on servicing this main logic board.

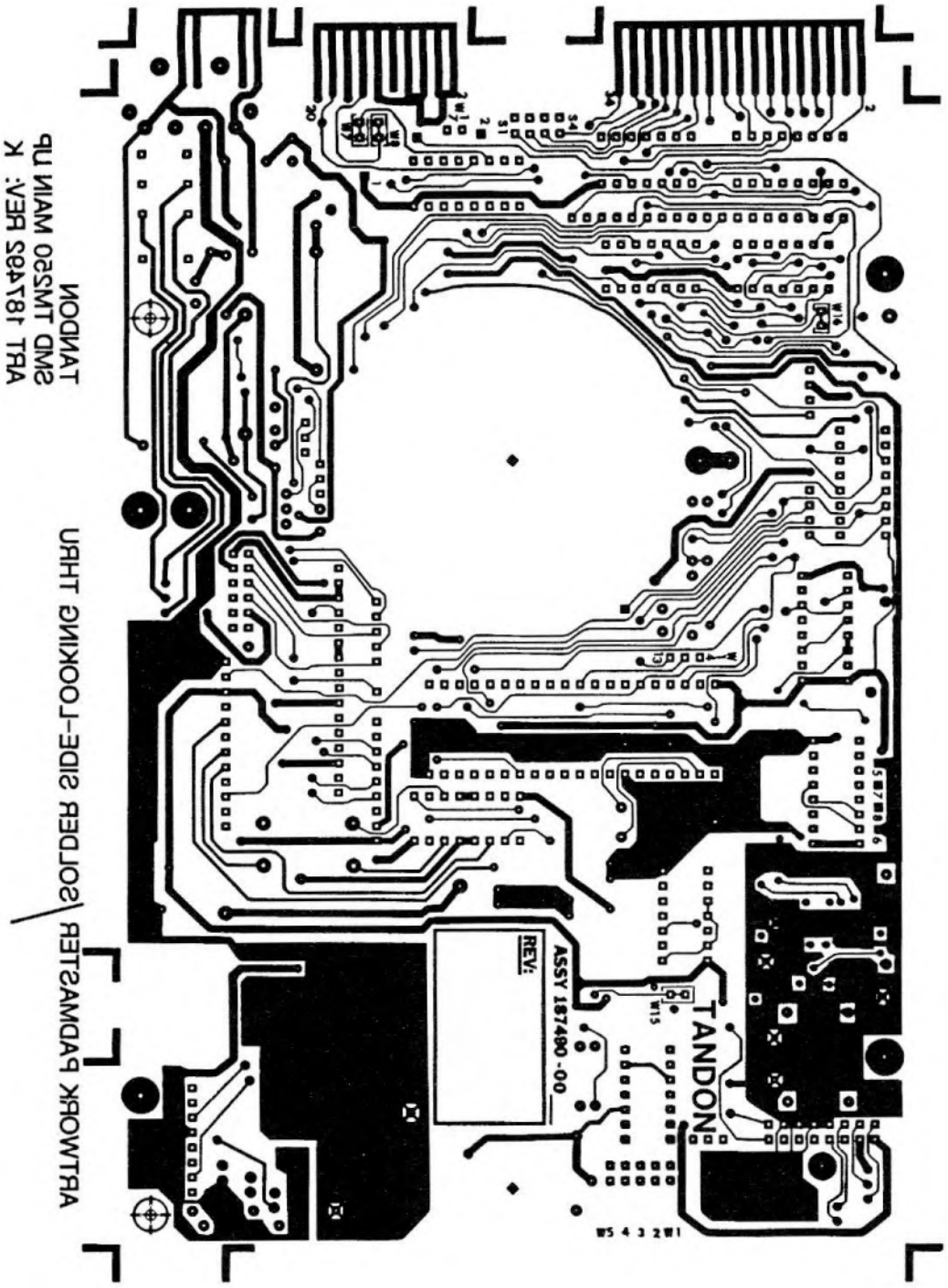
Component Layout



Silkscreen

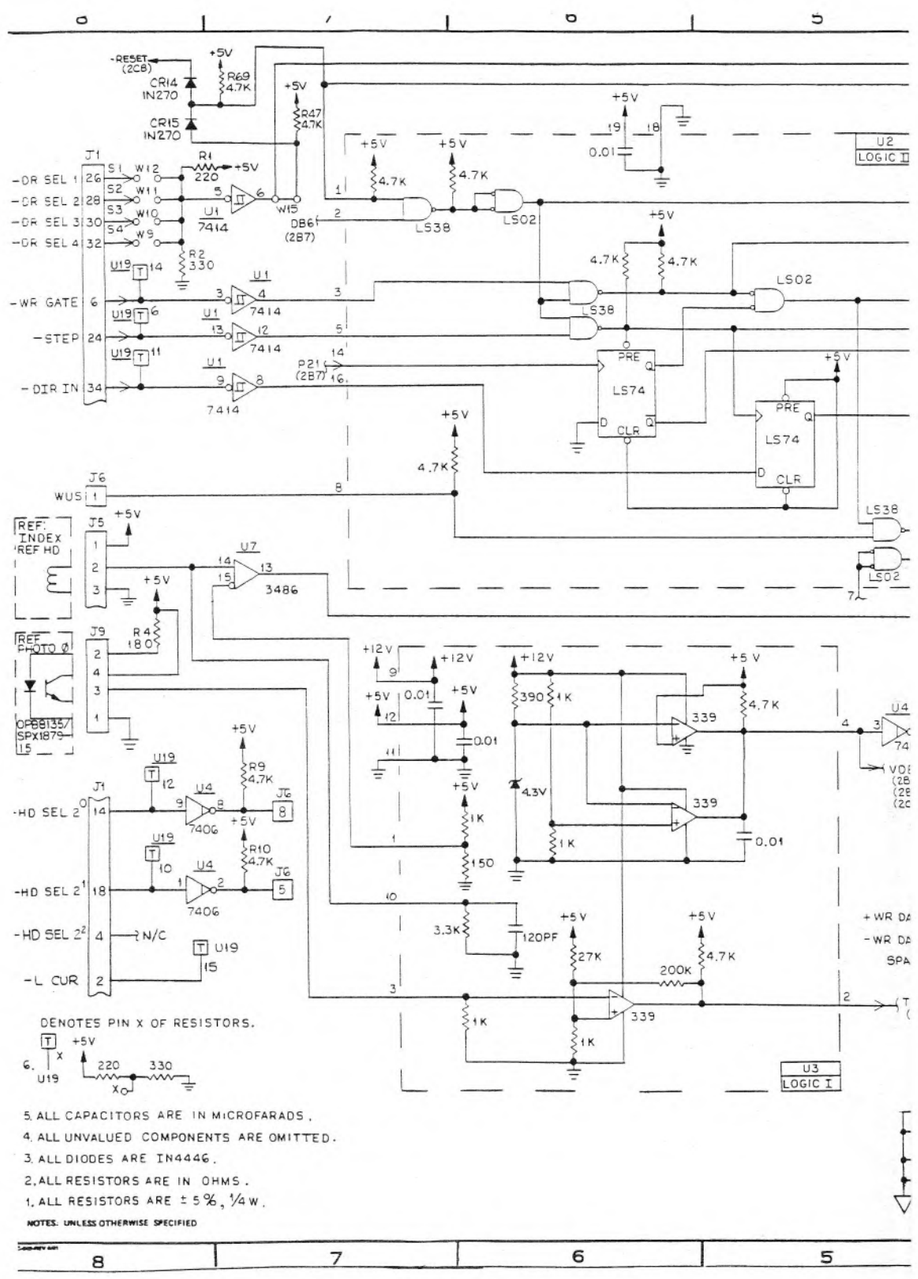


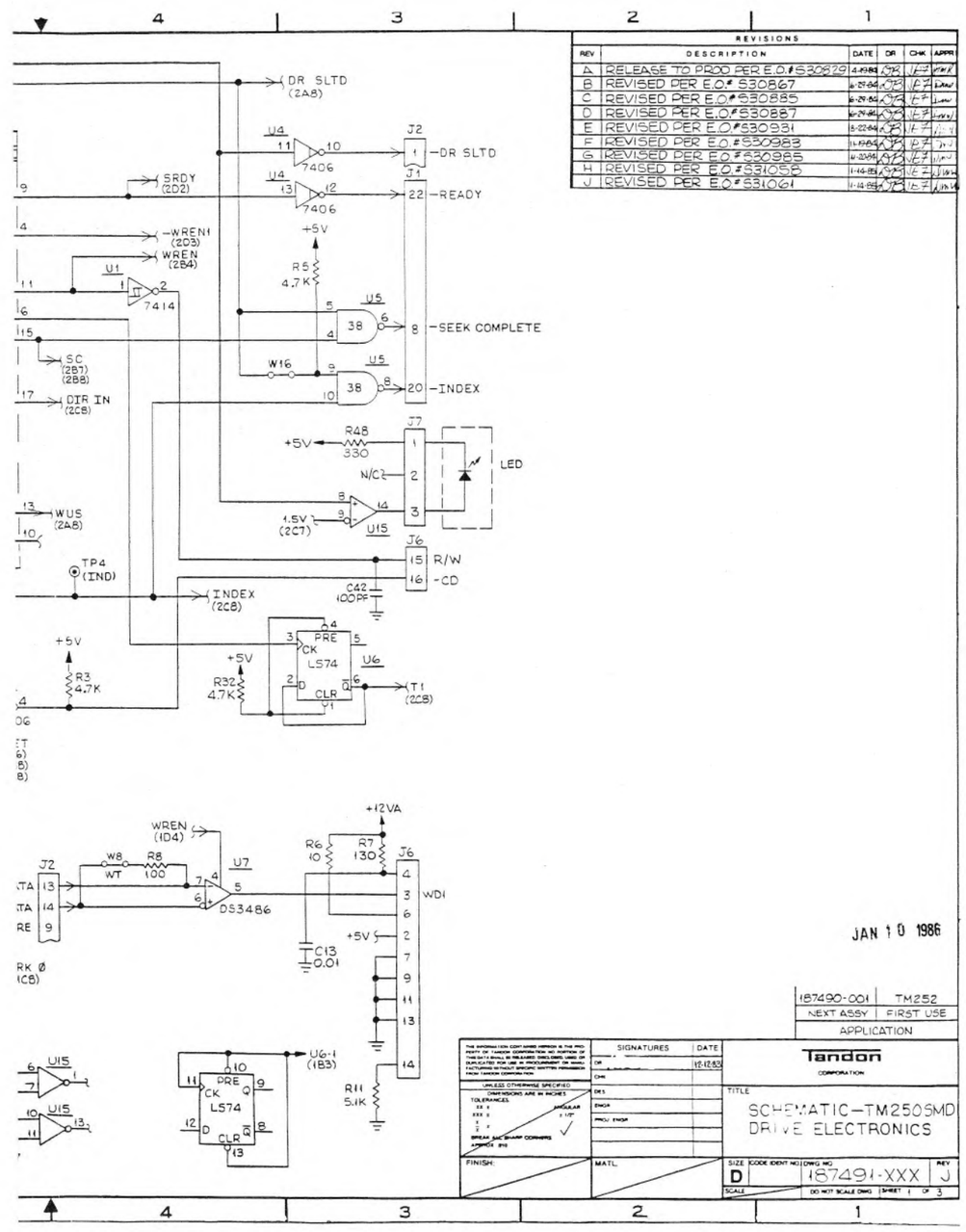
Component Side


TANDON
ASSY 187490-00
REV:
SOLDER SIDE-LOOKING THRU
ARTWORK PHOTOGRAPHED

Solder Side

Schematics





REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	RELEASE TO PROD PER E.O.# S30829	4-XX-84			
B	REVISED PER E.O.# S30867	6-29-84			
C	REVISED PER E.O.# S30885	6-29-84			
D	REVISED PER E.O.# S30887	6-29-84			
E	REVISED PER E.O.# S30931	8-22-84			
F	REVISED PER E.O.# S30983	11-XX-84			
G	REVISED PER E.O.# S30985	6-29-84			
H	REVISED PER E.O.# S31055	1-14-85			
J	REVISED PER E.O.# S31061	1-14-85			

JAN 10 1986

187490-001	TM252	
NEXT ASSY	FIRST USE	
APPLICATION		

Tandon CORPORATION

SIGNATURES | DATE: 12-17-85

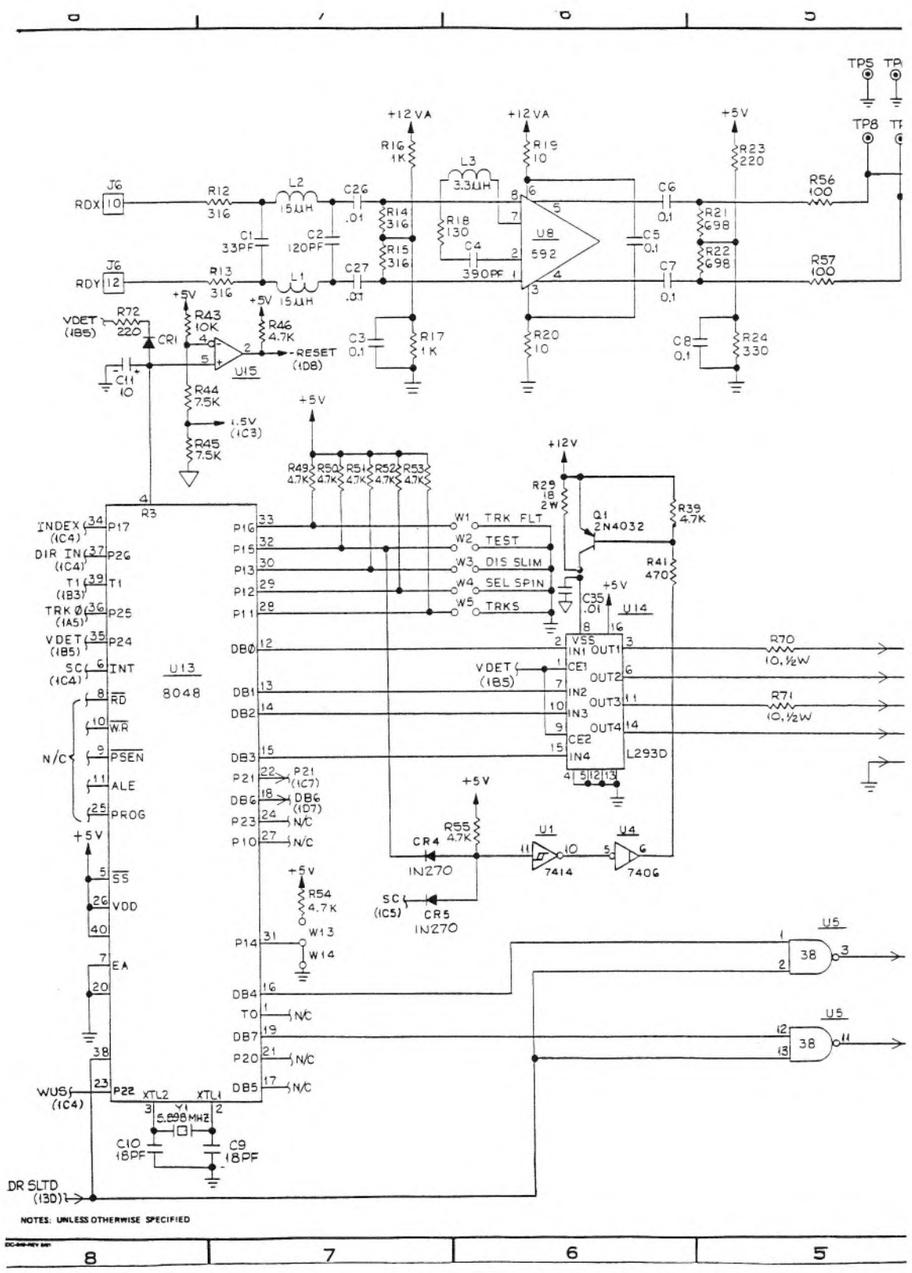
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; TOLERANCES: ANGULAR ±.1°; BREAK SHARP CORNERS

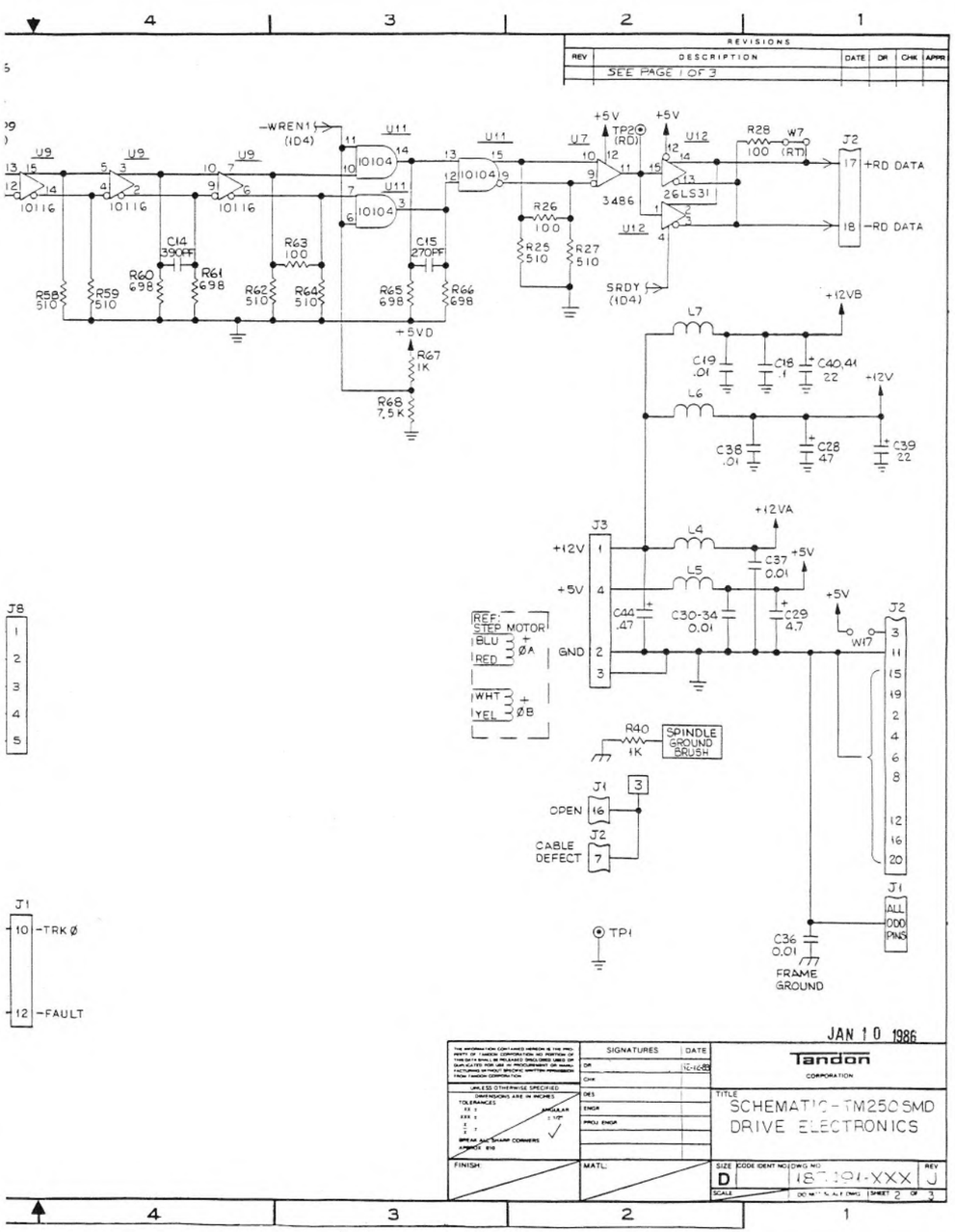
TITLE: SCHEMATIC—TM2505MD DRIVE ELECTRONICS

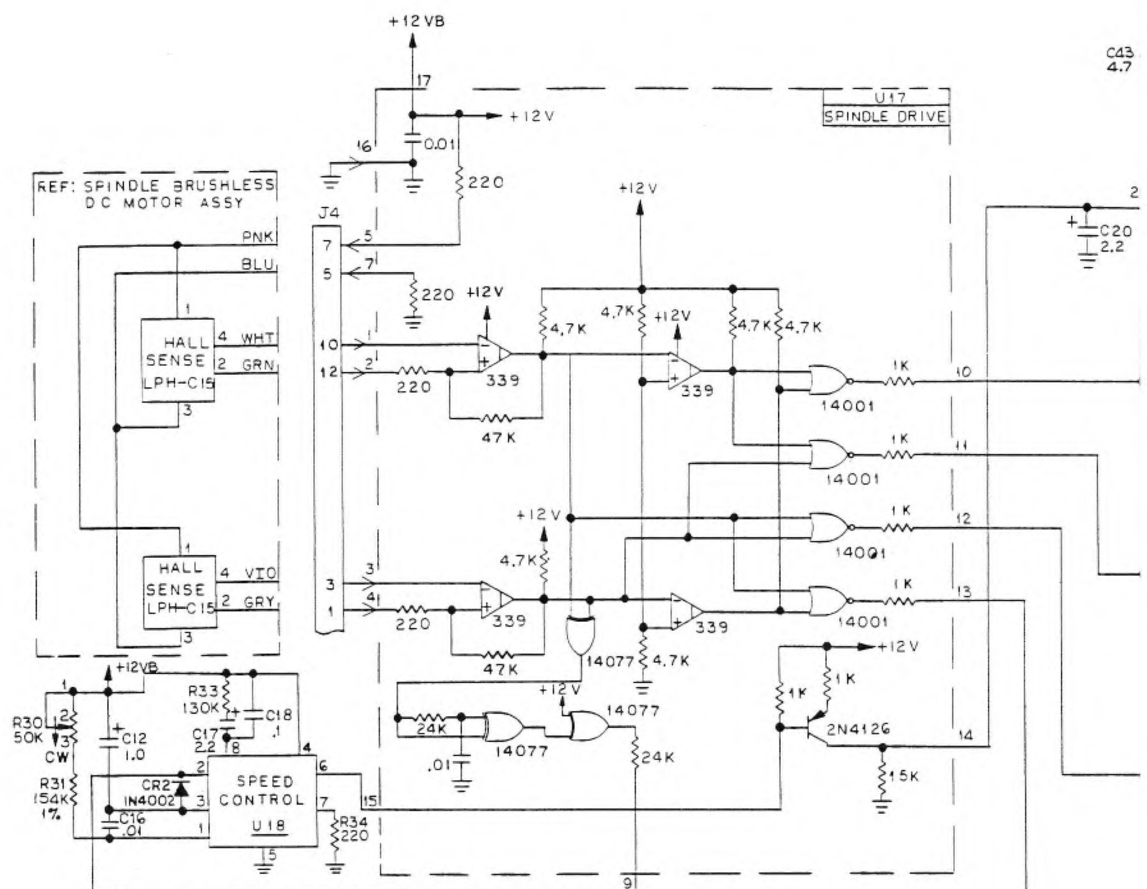
FINISH: | MATL:

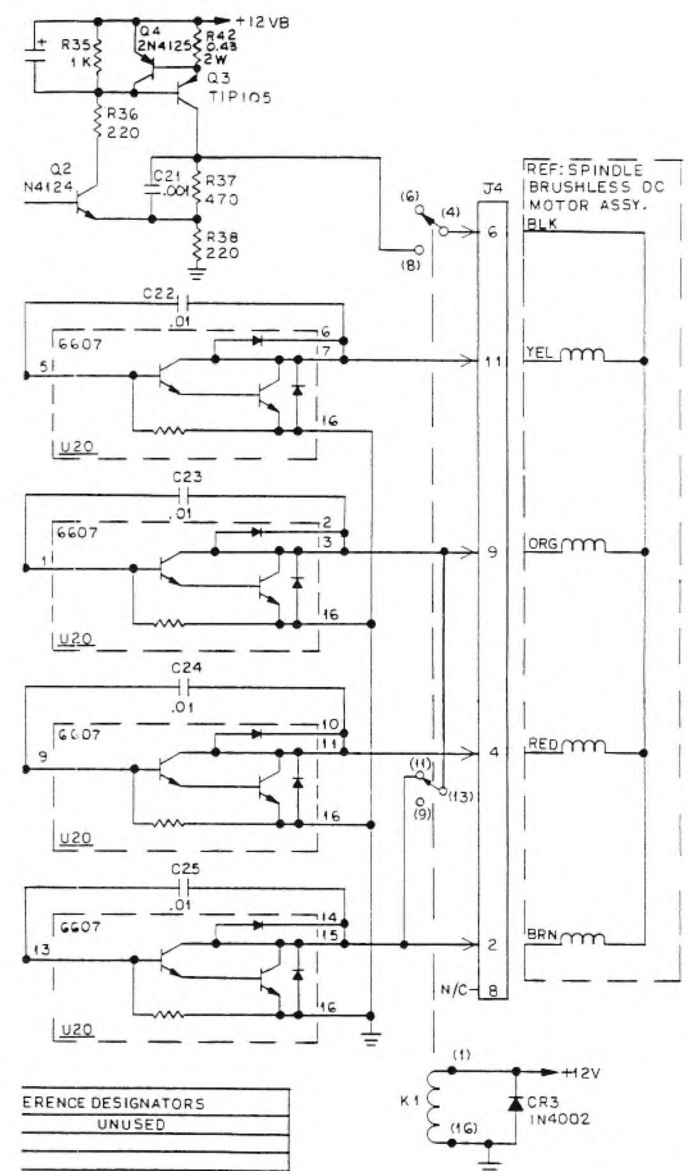
SIZE D | CODE IDENT NO | DWG NO 187491-XXX | REV J

SCALE | DO NOT SCALE DWG | SHEET 1 OF 3


8
7
6
5
TP5
TP8
+12VA
+5V
J6
RDX
RDY
R12 316
R13 316
L2 15µH
L1 15µH
C26 .01
C27 .01
C1 33PF
C2 120PF
R14 316
R15 316
R16 1K
L3 3.3µH
R18 130
C4 390PF
R19 10
R20 10
U8 592
C6 0.1
C5 0.1
C7 0.1
R21 698
R22 698
R23 220
R24 330
C8 0.1
R56 100
R57 100
VDET (1B5)
R72 220
CR1
R43 10K
R46 4.7K
RESET (1D8)
U15
C11 10
R44 7.5K
R45 7.5K
1.5V (1C3)
R3
R49 4.7K
R50 4.7K
R51 4.7K
R52 4.7K
R53 4.7K
INDEX (1C4)
DIR IN (1C4)
T1 (1B3)
TRKØ (1A5)
VDET (1B5)
SC (1C4)
P17
P26
T1
P25
P24
INT
RD
WR
PSEN
ALE
PROG
SS
VDD
EA
P22
XTL2
XTL1
WUS (1C4)
Y1 5.698 MHZ
C10 18PF
C9 18PF
U13 8048
P16
P15
P13
P12
P11
DBØ
DB1
DB2
DB3
P21
DB6
P23
P10
P14
DB4
T0
DB7
P20
DB5
W1 TRK FLT
W2 TEST
W3 DIS SLIM
W4 SEL SPIN
W5 TRK5
R25 18 2W
Q1 2N4032
R39 4.7K
R41 470
C35 .01
U14
VSS
IN1
OUT1
CE1
IN2
OUT2
IN3
OUT3
IN4
OUT4
CE2
L293D
VDET (1B5)
R70 10,½W
R71 10,½W
R55 4.7K
CR4 IN270
SC (1C5)
CR5 IN270
U1 7414
U4 7406
R54 4.7K
W13
W14
U5 38
DR SLTD (1B3)
NOTES: UNLESS OTHERWISE SPECIFIED


4
3
2
1
REVISIONS
REV
DESCRIPTION
DATE
DR
CHK
APPR
SEE PAGE 1 OF 3
-WREN1 (1D4)
U9 10116
U11 10104
U7 3486
U12 26LS31
TP2 (RD)
R28 100 (RT)
W7
J2
+RD DATA
-RD DATA
R26 100
R25 510
R27 510
SRDY (1D4)
R58 510
R59 510
R60 698
R61 698
C14 390PF
R62 510
R63 100
R64 510
C15 270PF
R65 698
R66 698
+5VD
R67 1K
R68 7.5K
L7
L6
C19 .01
C18 .1
C40,41 22
C38 .01
C28 47
C39 22
+12VB
+12V
+12VA
J3
L4
L5
C44 .47
C30-34 0.01
C37 0.01
C29 4.7
GND
W17
REF: STEP MOTOR
BLU
RED
WHT
YEL
ØA
ØB
R40 1K
SPINDLE GROUND BRUSH
J4
OPEN
CABLE DEFECT
J8
J1
-TRKØ
-FAULT
TP1
C36 0.01
FRAME GROUND
ALL ODD PINS
JAN 10 1986
SIGNATURES
DATE
DR
CHK
DES
ENGR
PROJ ENGR
Tandon CORPORATION
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGULAR
BREAK SHARP CORNERS
FINISH
MATL
TITLE
SCHEMATIC-TM250SMD
DRIVE ELECTRONICS
SIZE
D
CODE IDENT NO
DWG NO
18-191-XXX
REV
J
SCALE
SHEET 2 OF 3





SHUNT PLUG PROGRAMMING			
W1 - W13 SHUNT	FUNTION	FACTORY PROGRAMMED	USAGE
W1	TRK FAULT	O	INSTALL FOR EXCESS TRK FAULT
W2	TEST	O	INSTALL FOR FACTORY TEST
W3	DISABLE LIMIT	O	INSTALL TO DISABLE SOFT LIMITS
W4	SPIN SELECT	O	INSTALL FOR SPIN SELECT
W5	TRACKS	O	SPARE
RTW7	READ TERMINATOR	I	CLOSE ONLY AT END DRIVE OF DAISY CHAIN DATA
WTW8	WRITE TERMINATOR	I	CLOSE FOR RADIAL DATA
S4W9	DRIVE SELECT 4	O	INSTALL 1 OF 4 PLUGS ONLY PLUG CORRESPONDS TO DRIVE ADDRESS
S3W10	DRIVE SELECT 3	O	
S2W11	DRIVE SELECT 2	O	
S1W12	DRIVE SELECT 1	I	
W14		I	INSTALL FOR NO BACKLASH
W13		O	INSTALL FOR BACKLASH
W15	DRIVE SELECT	I	OPEN—ENABLES DRIVE TO CONTROLLER LINES WHEN NOT SELECTED
W16	INDEX		
W17	+5V TO J2-3	O	
U19	TERMINATOR PAK		

O = OMIT
I = INSTALL

REF		ERENCE DESIGNATORS
LAST USED		UNUSED
C44		
CR15		
J9		
L5		
Q4		
R72		
RP1		
TP8	TP	3
U20		
W17	W6	
K1		

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE PAGE 1 OF 3				

I.C. LOCATION AND VOLTAGE CHART				
LOCATION	TYPE	+5V	+12V	GROUND
U1	74LS14	14		7
U2	210933 HYBRID I.C.	19		18
U3	210932 HYBRID I.C.	8	5	7
U4	7406	14		7
U5	7438	14		7
U6	74S74	14		7
U7	DS3486	16		8
U8	592		6	3
U9	10116	1,16		8
U10				
U11	10104	1,16		8
U12	26LS31	16		8
U13	8048	26,40		20
U14	L293	16		8
U15	339		3	12
U17	210935 HYBRID I.C.		15	14
U18	M51970L		4	5
U19	220/330 TERM PAK	16		8
U20	6607			16

JAN 10 1986

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGULAR
BREAK ALL SHARP CORNERS

SIGNATURES	DATE
DR	12-12-83
CHK	
DES	
ENGR	
PROJ ENGR	

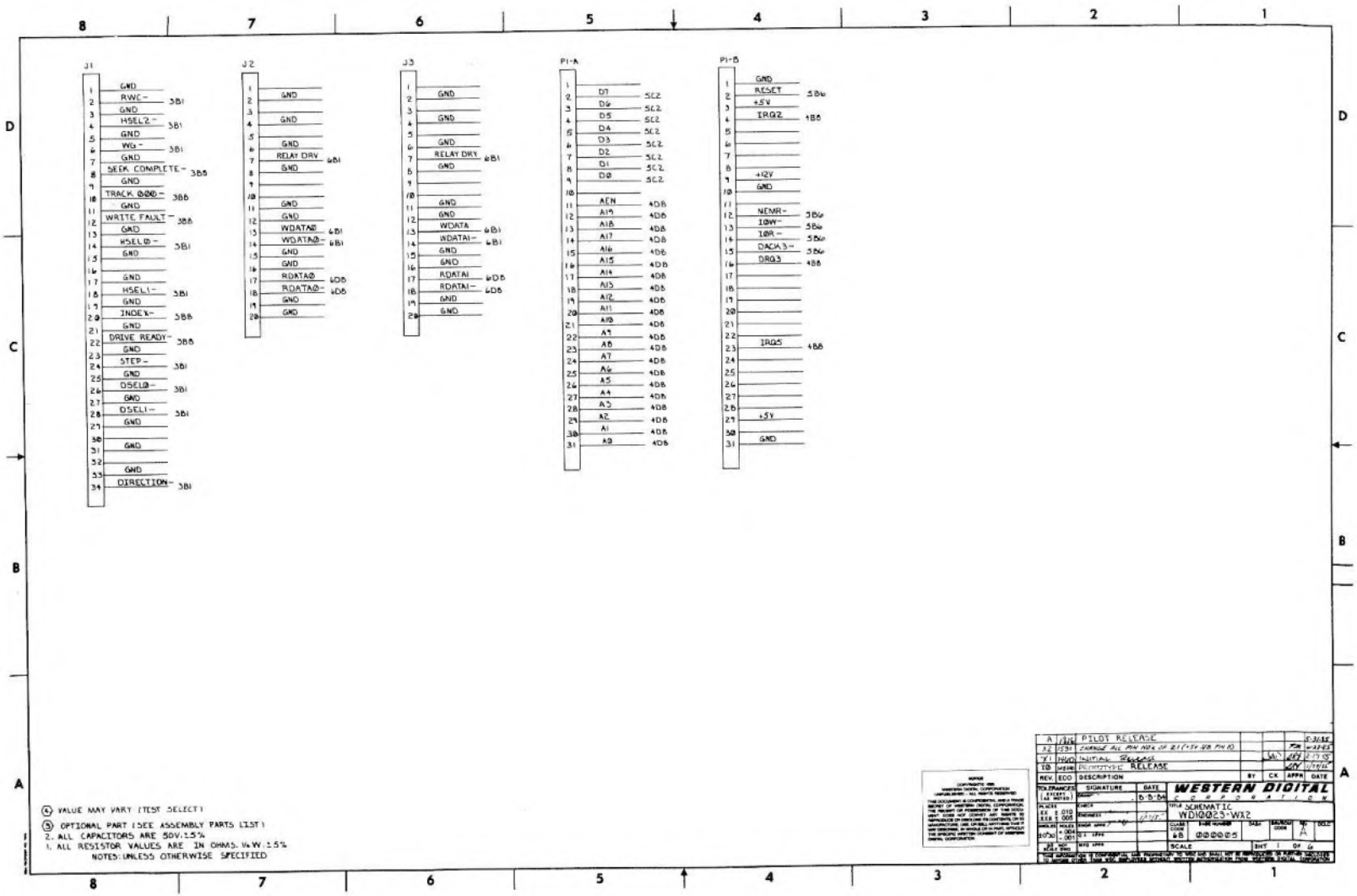
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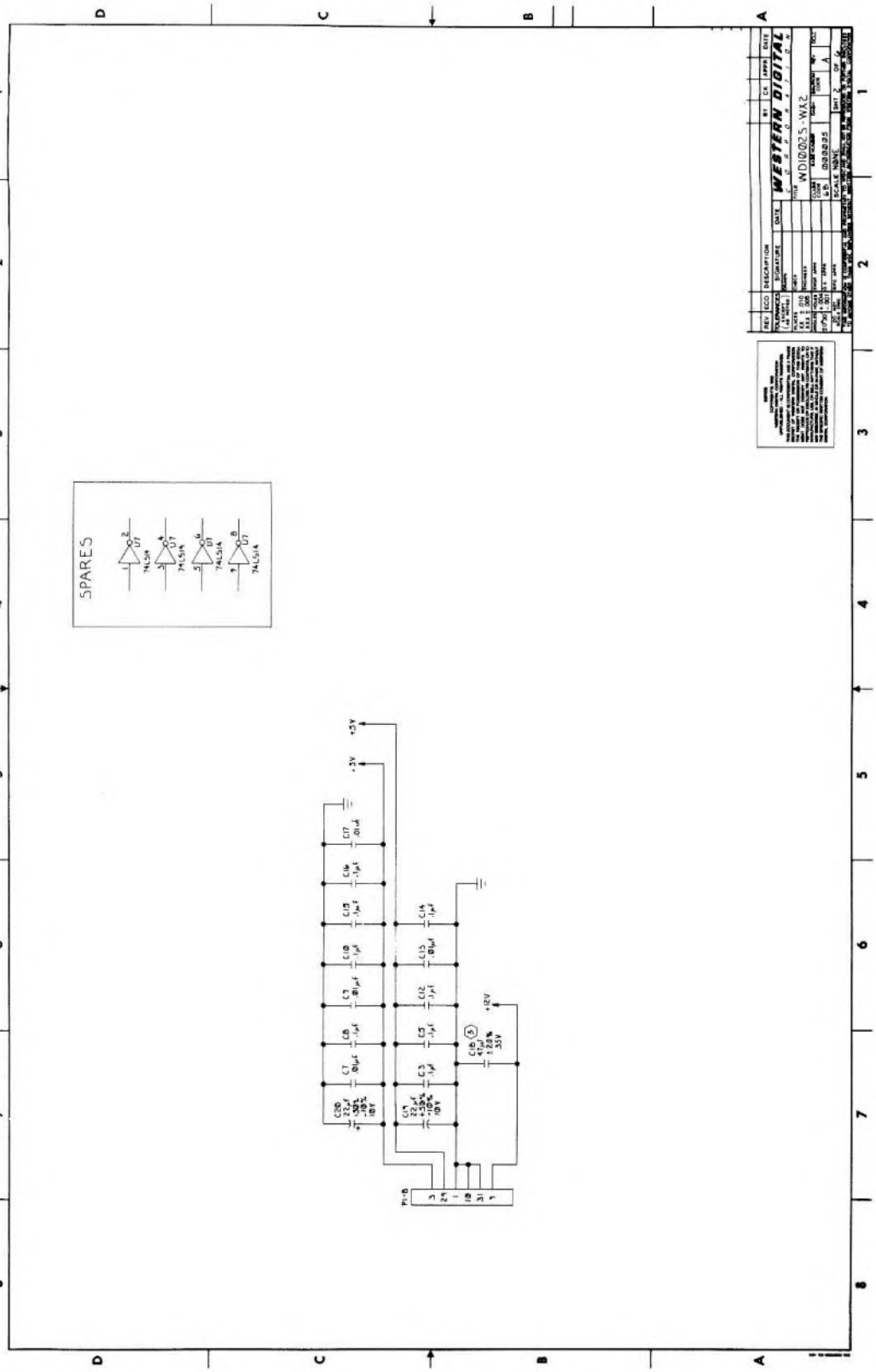
Tandon CORPORATION

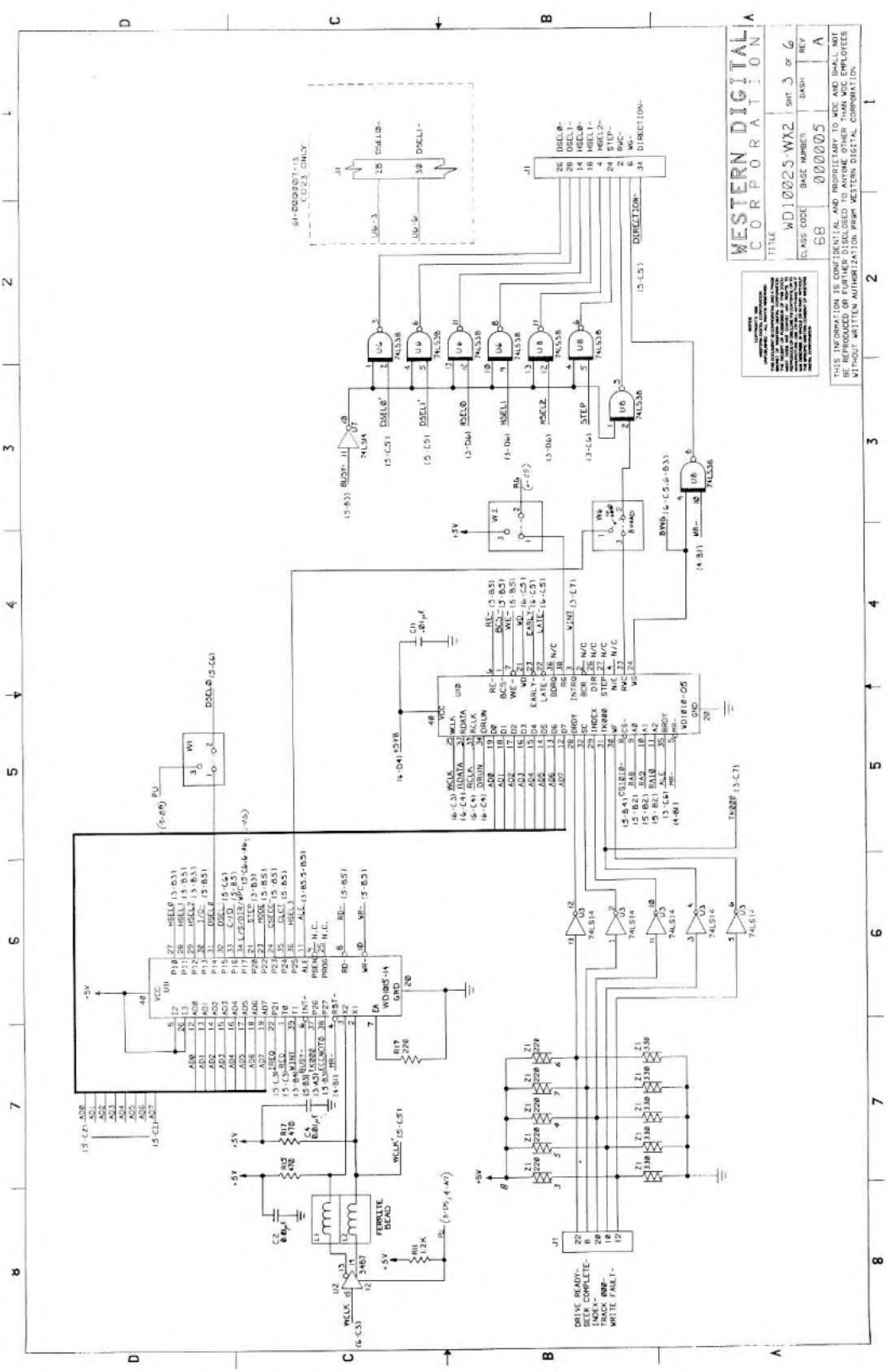
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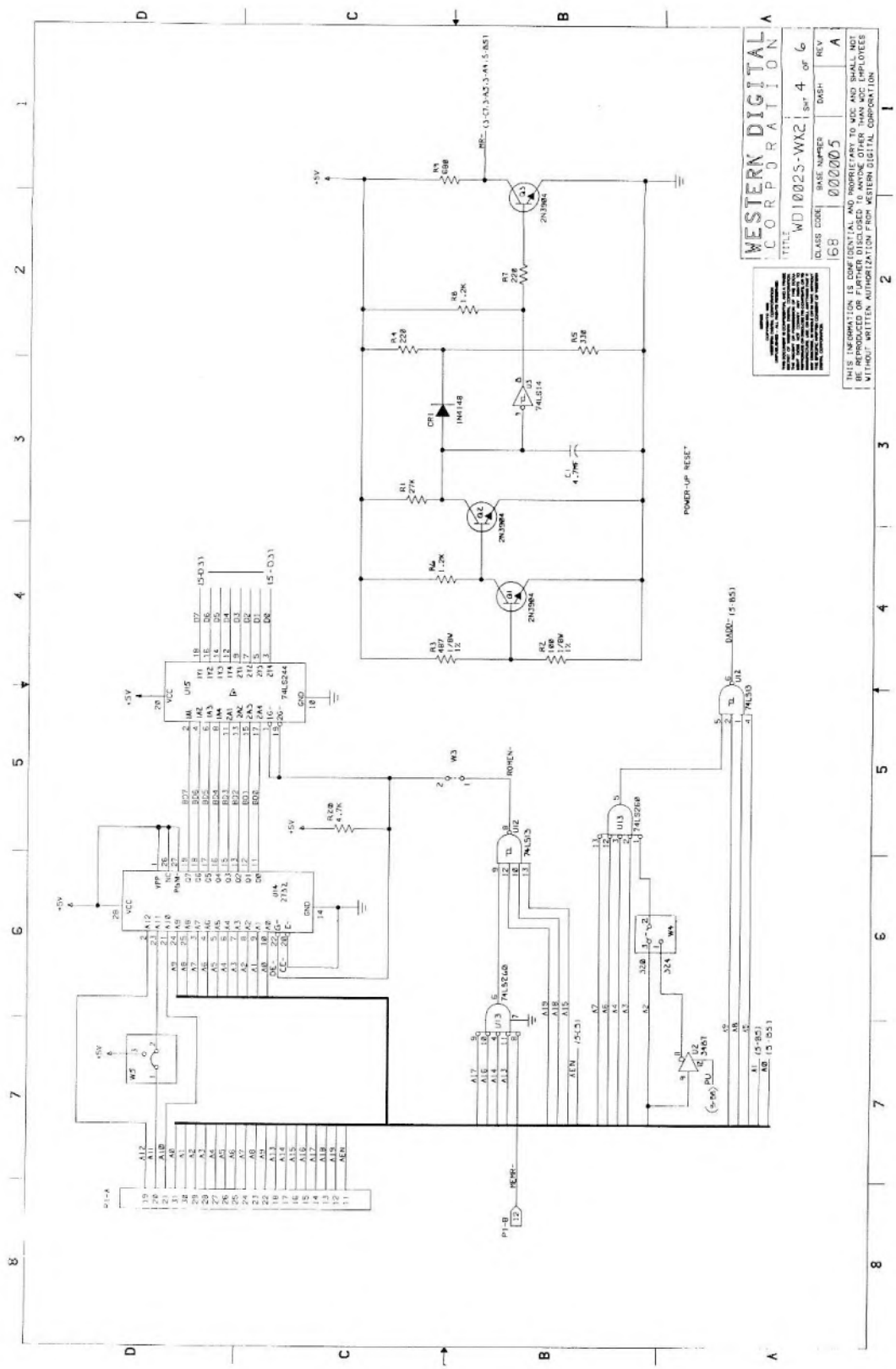
SIZE D | CODE IDENT NO | DWG NO 187491-XXX | REV J
SCALE | DO NOT SCALE DWG | SHEET 3 OF 3

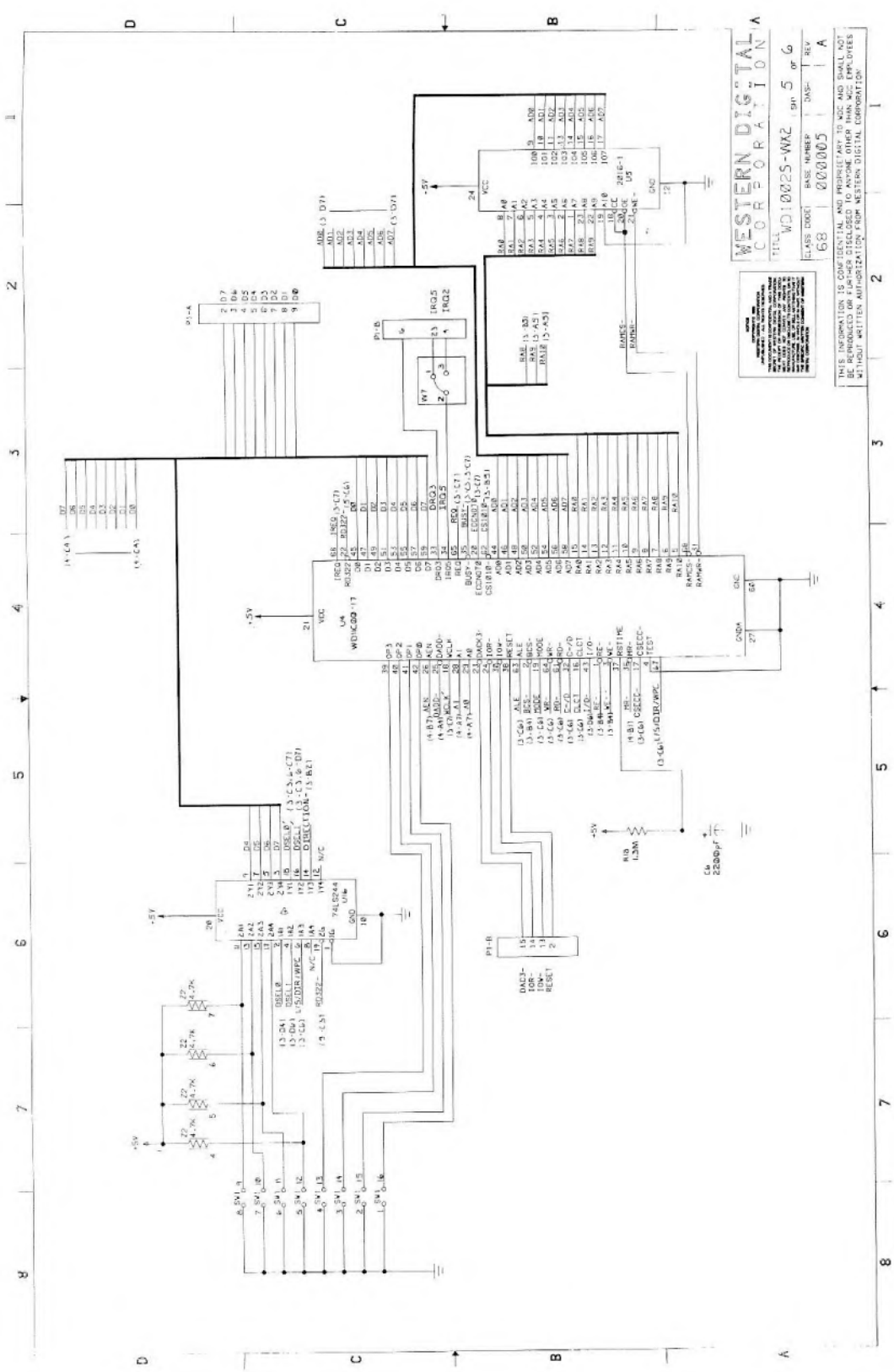
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

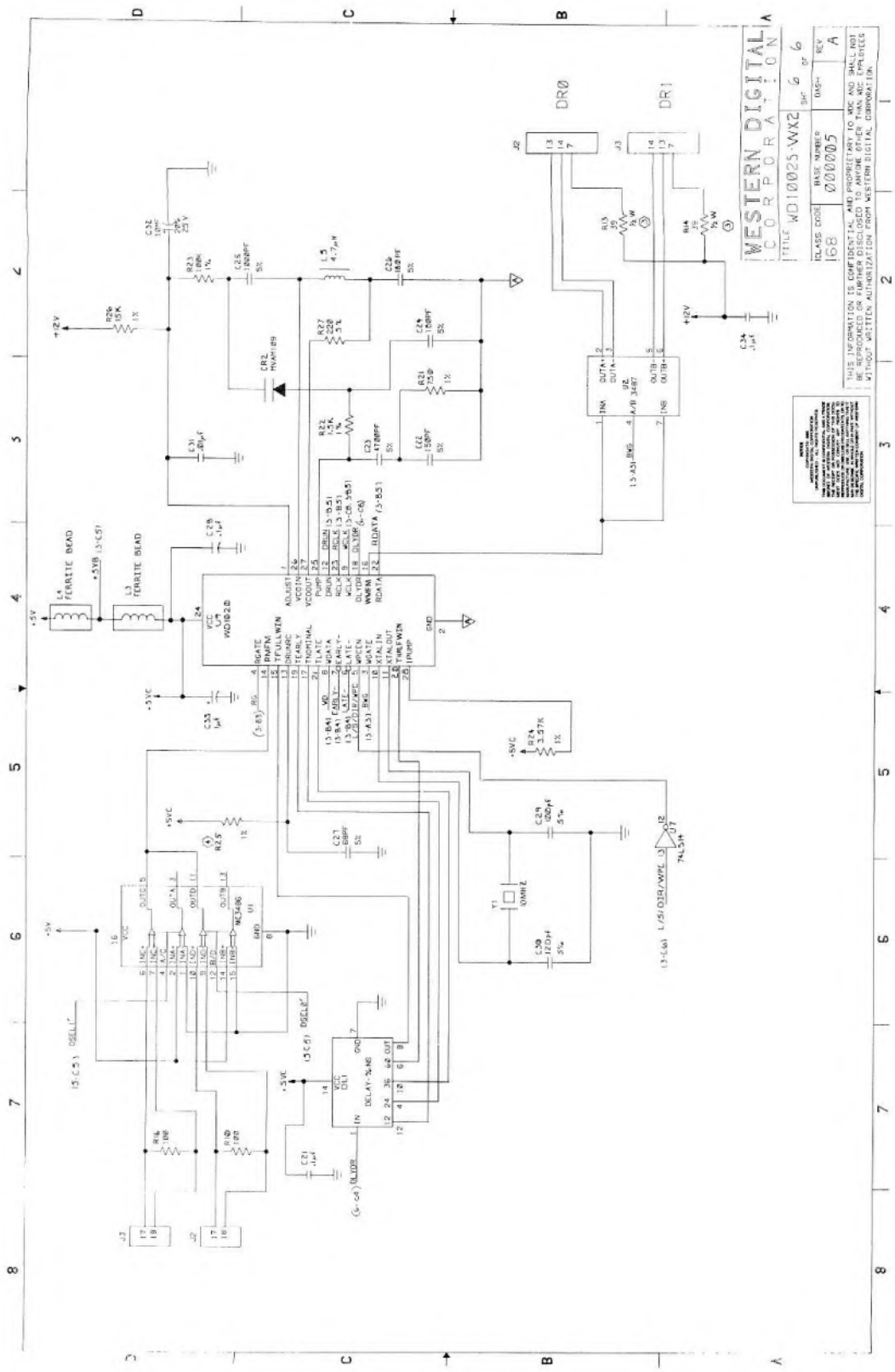

J1
1 GND
2 RWC- 3B1
3 GND
4 HSEL2- 3B1
5 GND
6 WG- 3B1
7 GND
8 SEEK COMPLETE- 3B6
9 GND
10 TRACK 000- 3B6
11 GND
12 WRITE FAULT- 3B6
13 GND
14 HSEL0- 3B1
15 GND
16
17 GND
18 HSEL1- 3B1
19 GND
20 INDEX- 3B6
21 GND
22 DRIVE READY- 3B6
23 GND
24 STEP- 3B1
25 GND
26 DSEL0- 3B1
27 GND
28 DSEL1- 3B1
29 GND
30
31 GND
32
33 GND
34 DIRECTION- 3B1
J2
1
2 GND
3
4 GND
5
6 GND
7 RELAY DRV 6B1
8 GND
9
10
11 GND
12 GND
13 WDATA0 6B1
14 WDATA0- 6B1
15 GND
16 GND
17 RDATA0 6D8
18 RDATA0- 6D8
19 GND
20 GND
J3
1
2 GND
3
4 GND
5
6 GND
7 RELAY DRV 6B1
8 GND
9
10
11 GND
12 GND
13 WDATA 6B1
14 WDATA- 6B1
15 GND
16 GND
17 RDATA 6D8
18 RDATA- 6D8
19 GND
20 GND
P1-A
1
2 D7 5C2
3 D6 5C2
4 D5 5C2
5 D4 5C2
6 D3 5C2
7 D2 5C2
8 D1 5C2
9 D0 5C2
10
11 AEN 4D8
12 A19 4D8
13 A18 4D8
14 A17 4D8
15 A16 4D8
16 A15 4D8
17 A14 4D8
18 A13 4D8
19 A12 4D8
20 A11 4D8
21 A10 4D8
22 A9 4D8
23 A8 4D8
24 A7 4D8
25 A6 4D8
26 A5 4D8
27 A4 4D8
28 A3 4D8
29 A2 4D8
30 A1 4D8
31 A0 4D8
P1-B
1 GND
2 RESET 5B6
3 +5V
4 IRQ2 4B8
5
6
7
8
9 +12V
10 GND
11
12 NEMR- 3B6
13 IOW- 5B6
14 IOR- 5B6
15 DACK3- 3B6
16 DRQ3 4B8
17
18
19
20
21
22
23 IRQ5 4B8
24
25
26
27
28
29 +5V
30
31 GND
8 7 6 5 4 3 2 1
D C B A
④ VALUE MAY VARY (TEST SELECT)
③ OPTIONAL PART (SEE ASSEMBLY PARTS LIST)
2. ALL CAPACITORS ARE 50V ±5%
1. ALL RESISTOR VALUES ARE IN OHMS, ¼W ±5%
NOTES: UNLESS OTHERWISE SPECIFIED
A 1/86 PILOT RELEASE
X2 1091 CHANGE ALL PIN NOs OF J1 (34 PIN D)
X1 1190 INITIAL RELEASE
10 MAR PRELIMINARY RELEASE
REV ECO DESCRIPTION BY CK APPR DATE
TOLERANCES (EXCEPT AS NOTED) SIGNATURE DATE
DRAWN 8-8-84
CHECK
ENGINEER
MFG APPR
SCALE
WESTERN DIGITAL CORPORATION
TITLE SCHEMATIC
WD1002S-WX2
SIZE A
DWG NO 000005
REV
SHT 1 OF 6


SPARES
WESTERN DIGITAL
WD1002S-WX2


WESTERN DIGITAL CORPORATION
WD10025-WX2
SHT 3 OF 6
DASH
REV
A
CLASS CODE
68
BASE NUMBER
000005
THIS INFORMATION IS CONFIDENTIAL AND PROPRIETARY TO WDC AND SHALL NOT BE REPRODUCED OR FURTHER DISCLOSED TO ANYONE OTHER THAN WDC EMPLOYEES WITHOUT WRITTEN AUTHORIZATION FROM WESTERN DIGITAL CORPORATION


WESTERN DIGITAL CORPORATION
WD10025-WX2
SHT 4 OF 6
BASE NUMBER
000005
DASH
REV
A
CLASS CODE
168
THIS INFORMATION IS CONFIDENTIAL AND PROPRIETARY TO WDC AND SHALL NOT BE REPRODUCED OR DISCLOSED TO ANYONE OTHER THAN WDC EMPLOYEES WITHOUT WRITTEN AUTHORIZATION FROM WESTERN DIGITAL CORPORATION
POWER-UP RESET
2N3904
74LS14
74LS244
74LS245
74LS30
74LS138
74LS08
74LS32
74LS04
74LS51
2732
IN4148


WESTERN DIGITAL CORPORATION
WD1002S-WX2
SHT 5 OF 6
68
000005
REV A
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WESTERN DIGITAL CORPORATION
TITLE WD10025-WX2
BASE NUMBER 000005
DASH-
REV A
SHT 6 OF 6
CLASS CODE 168
THIS INFORMATION IS CONFIDENTIAL AND PROPRIETARY TO WDC AND SHALL NOT BE REPRODUCED OR FURTHER DISCLOSED TO ANYONE OTHER THAN WDC EMPLOYEES WITHOUT WRITTEN AUTHORIZATION FROM WESTERN DIGITAL CORPORATION.
DR0
DR1
WD1002D
WC3486
74LS14
+12V
+5V
-5VC
DSELL

Parts Lists

10 MEG Fixed Drive

Symbol	Description	RS Part No.
	Strap, Ground	AHC-0156
	Screw, Pan Hd, 2-56x1/4	AHD-1050
	Nut, Hex, Small pattern, 2-56	AHD-7010
C1	Cap Chip, 33 PF, 5%,%0V, NPO	
C2	Cap Chip, 120 PF, 5%, 50V, NPO	
C3,5-8,18	Cap Chip, 0.1 UF, +80-20%, 50V	
C4,14	Cap Chip, 390 PF, 5%, %0V, NPO	
C9,10	Cap Chip, 18 PF, 5%, 50V, NPO	
C11	Cap, 10MF, ±20%, 16V, Elect, RAD	CC-106MDAP
C12	Cap, 1 UF, ±20%, 25V, RAD Elec	CC-105MFAP
C13,19,22-27	Cap Chip, 0.01 UF, +80-20%, 50V	
C15	Cap Chip, 270 PF, 5%, 50V, NPO	
C16	Cap Chip, 0.01 UF, 5%, 50V, NPO	
C17,20	Cap, 2.2 UF, ±20%, 50V, RAD Elec	CC-225MJAP
C21	Cap Chip, 0.001 UF, 20%, 50V, Z5U	
C28	Cap, 47 MF, ±10%, 16V, Elect, RAD	CC-476KDAP
C29	Cap, 4.7 UF, ±20%, 16V, RAD Tant	CC-475MDTP
C30-38	Cap Chip, 0.01 UF, +80-20%, 50V	
C39-41	Cap, 22 MF, ±20%, 16V, Elect, RAD	CC-226MDAP
C42	Cap, 100PF, 5% 50V, X7R, RAD	CC-101JJCP
C43	Cap, 4.7MF, ±20%, 35V, RAD Elec	CC-475MGAP
C44	Cap, 0.47 UF, ±20%, 50V, RAD Elec	CC-474MJAP
CR1	Diode, IN4446	ADX-1879
CR2,3,6-13	Diode, IN4002 Rectifier	DX-0206
CR4,5,14,15	Diode, IN270	
J4	Conn, Rt Angle, Male (2x6)	AJ-4051
J5,8,9	Conn, Rt Angle, Male (1x12)	AJ-1050
J6	Conn, Rt Angle, Male (2x8)	AJ-1051
J7	Conn, Rt Angle, Male (1x3)	AJ-1049
K1	Relay, DPDT	AR-8007
L1,2	Inductor, 15 UH, 10% Axial	ACA-1014
L3	Inductor, 3.3 UH, 10% Axial	ACA-8384
L4-7	Inductor, Ferrite VK200 10/313	ACA-8282

10 MEG Fixed Drive

Symbol	Description	RS Part No.
Q1	Transistor, 2N4032	MX-4651
Q1	Insulator, Transistor Pad	
Q2	Transistor, 2N4124 NPN	AMX-4178
Q3	Transistor, TIP 105	MX-4944
Q3	Heat Sink, Plate	
Q3	Insulating Washer, #4	
Q3	Screw, 4-40x3/8 PH Flat HD	AHD-2018
Q3	Insulator, Sil-Pad	
Q3	Lock Washer, Split, #4	AHD-8335
Q3	Nut, Hex, 4-40, small pattern	AHD-7289
Q3	Washer, Flat, #4	AHD-8541
Q4	Transistor, 2N4125	AMX-4330
R1,23,34 36,38	Res, Car 220 Ohm, 5%, 1/4W	ND-0149EEC
R2,24,48	Res, Car 330 Ohm, 5%, 1/4W	ND-0159EEC
R3,5,9,10, 32,39,46,47, 49-55,69	Res, Car 4.7K Ohm, 5%, 1/4W Chip	ND-0247EEC
R4	Res Chip, 180 Ohm, 5%, 1/4W	ND-0144EEN
R6,19,20	Res, Car 10 Ohm, 5%, 1/4W Chip	ND-0281EEC
R7,18	Res Chip, 130 Ohm, 5%, 1/4W	ND-0533BEN
R8,26,28, 56,57,63	Res Car, 100 Ohm, 5%, 1/4W	ND-0132EEC
R11	Res Chip, 5.1K Ohm 5%, 1/4W	
R12-15	Res Chip, 316 Ohm, 1%, 1/4W	
R16,17,35, 40,67	Res, Car 1K Ohm, 5%, 1/4W	ND-0196EEC
R21,22,60, 61,65,66	Res Chip, 698 Ohm, 1% 1/4W	ND-0568BEN
R25,27,58 59,62,64	Res Chip, 510 Ohm, 5%, 1/4W	ND-0173EEN
R29	Res, 180HM, 5%, 2W	N-0075EEH
R30	Pot, 50K Ohm, 10 Turn	AP-1972
R31	Res, 154K, 1%, 1/8W	N-0681BBE
R33	Res Chip, 130K Ohm, 5%, 1/4W	ND-0379EEN
R37,41	Res, Car 470 Ohm, 5%, 1/4W	ND-0169EEC
R42	Res, 0.43 Ohm, 5%, 2W	N-0679EHH
R43	Res Chip, 10K Ohm, 5%, 1/4W	ND-0281EEC
R44,45,68	Res Chip, 7.5K Ohm, 5%, 1/4W	ND-0266EEN
R70,71	Res, Car F 10 Ohm, 5%, 1/2W	N-0063EFC
R72	Res, Car F 220 Ohm, 5%, 1/4W	N-0149EEC

10 MEG Fixed Drive

Symbol	Description	RS Part No.
TP1,2,4-8	Terminal, Tin	
U1	IC 74LS14 Motorola 14 Pin	MX-6181
U2	Hybrid, Logic II, 210933	
U3	Hybrid, Logic I, 210932	
U4	IC, TTL NS7406 14 Pin	AMX-3675
U5	IC, 7438 14 Pin	AMX-3683
U6	IC, SN74LS74N 14 Pin	MX-3808
U7	IC, MC3486 Motorola 16 Pin	MX-4658
U8	IC, TL592, 8 Pin SOIC	MX-4652
U9	IC, MC10116 Motorola 16 Pin	MX-5857
U11	IC MC10104 Motorola 16 Pin	MX-5856
U12	IC 26LS31 Natl. Semi. 16 Pin	MX-5854
U13	Assy, 8048, Pgm'd Rev F	
U13	Socket, 40 Pin	AJ-6017
U14	IC, L293D SGS 16 Pin	MX-4653
U15	IC, LM339N RCA 14 Pin	MX-5405
U17	Hybrid, Spindle Drive, 210935	
U18	IC, M51970L	MX-4943
U19	Socket, Dip, 16 Pin	AJ-7366
U19	Res Net,220/330, 16 Pin Dip	
U20	Transistor, Array, QUAD, 6607	MX-4945
W1-5	Conn, Rt Angle, Male (2x5)	AJ-1052
W9-12	Conn, Rt Angle, Male (2x4)	AJ-4048
W12,14	Programming Jumpers	AJ-1056
W13,14	Terminal, Gold	AJ-1053
W15,16	Buss Wire, Solid 24 AWG	
Y1	Crystal, 5.89824 MHz	MX-0080

WD1002S-WX2

Symbol	Description	RS Part No.
	Printed Circuit Board	
	Screw, 4-40 x 1/4 Mach PH Phil	AHD1413
C1	Cap, TANT 4.7mf, 15V 20%	CC475MDTA
C2,4,7,9, 11,13,17, 31	Cap, 0.01mf, +80%-20%, 50V	CF2219
C3,5,8,10, 12,14,15, 16,28, 34,21	Cap, 0.1mf, +80-20%, 50V	CF2212
C6	Cap, 2200pf, ± 10%, 50V	CC222KJCA
C27	Cap, 68pf, 5% 50V Cer N750	CF2213
C18	Cap, 47mf, 20%, 35V	CC476MGAP
C19,20	Cap, 22mf, 10V + 5%-10%	CC226JCAA
C22	Cap, 150 pf, 5% 50V	CF2302
C23	Cap, 4700pf, 5%, 50V Cer	CC472JJCA
C24,26	Cap, 180pf, 5% 50V	CC181JJCA
C25	Cap, 1000pf, 5%, 50V	CF2222
C29	Cap, 100pf, 5% 50V	CC101JJCA
C30	Cap, 120pf, 5%, 50V, AX	CF2299
C32	Cap, TANT 10mf, 20% 25V	CC106MFTA
C33	Cap, 1mf, TANT, 10% 35V	CC105KGTA
CR1	Diode, IN4148	DX0022
CR2	Diode, Tuning MVAM109	DX0392
DL1	Delay Line, 96 NS 5TAP, DIP14	MX5180
J1	Conn., 34 Pin	AJ1024
J2,3	Conn., 20 Pin	AJ1023

WD1002S-WX2

Symbol	Description	RS Part No.
L1,2,3,4	Ferrite bead	
L5	Inductor, 4.7uH, ± 1%	ACA1010
Q1,2,3	Transistor, 2N3904	2N3904
R1	Res, 27K Ohm 1/4W 5%	N0316EEC
R2	Res, 100 Ohm, 1/8W 1%	N0132BBE
R3	Res, 487 Ohm, 1/8W 1%	N0810BBE
R4,7,27,19	Res, 220 Ohm, 1/4W 5%	N0149EEC
R5	Res, 330 Ohm 1/4W 5%	N0159EEC
R8,6,11	Res, 1.2K Ohm, 1/4W 5%	N0199EEC
R9	Res, 680 Ohm, 1/4W 5%	N0183EEC
R10,16	Res, 100 Ohm, 1/4W, 5%	N0132EEC
R13,14	Res, 10 Ohm, 5%, 1/2W	N0063EFC
R15,17	Res, 470 Ohm 1/4W 5%	N0169EEC
R18	Res, 1.3M Ohm, 1/4W 5%	N0793EEC
R20	Res, 4.7K Ohm 1/4W 5%	N0247EEC
R21	Res, 750 Ohm 1/8W ± 1%	N0185BBE
R22	Res, 1.5K Ohm 1/8W, 1%	N0206BBE
R23	Res, 100K, Ohm 1/8W 1%	N0371BBE
R24	Res, 3.57K Ohm 1%	N0809BBE
R25	Res, Test select 1/8W 1%	
R26	Res, 15K Ohm 1/8W 1%	N0297BBE
SW1	Connector 8 Pin Dual row	AJ1013
U1	IC, MC3486, Quad RS422 Line RCVR	AMX5772
U2	IC, MC3487, Quad RS422 Line DRVR	MX6790
U3	IC, 74LS14, Hex Inv. W/Schmitt Trig	MX6181
U4	IC, WD11C00-17 Rev. "D"	MX5179
U4	Socket, Chip Carrier, 68 Pin Solder Tail	AJ1047
U5	IC, 2016 2K x 8 RAM (200NS)	MX5177
U6,8	IC, 74LS38, Quad Dual in NAND W/OC	AMX4328
U7	IC, 74LS04 Hex Inverter	AMX3552
U9	IC, WD10C20 Read/Write Data Sep	MX5178
U10	IC, WD1010A-05 Winchester Controller	MX2130
U10	Socket, IC DIP 40 Pin	AJ1046

WD1002S-WX2

Symbol	Description	RS Part No.
U11	IC, WD1015-14 Microcontroller Mask	MX3074
U12	IC, 74LS13, Dual 4 In NAND W/Schmitt Trig	MX5175
U13	IC, 74LS260, Dual 5 in NOR	AMX4664
U14	IC, Custom Bios Eprom	MX-5181
U14	Socket, IC, DIP 28 Pin	AJ1027
U15,16	IC, 74LS244 Octal Driver, 3 State	AMX3864
W1,2,4,5, 6,7	Conn., Post header 3 Pin	
W3	Conn., Post header 2 Pin	AJ1025
Y1	Crystal, 10.000 Mhz	MX1269
Z1	Res NTWK, 8 pin sip, 220/330 Ohm, 2%,1/8W	ARX0037
Z2	Res NTWK, 8 pin sip, 4.7K 2% 1/8W	ARX0038

Tandy 1001 Main Logic Main Assembly

Qty	Description	RS Part No.
1	Chassis-Main	8729314
1	Support-Disk Drives	8729313
1	Panel-Option Board	8729312
1	Outline PCB Power Supply (54w P.S. Stuffed)	8489073
1	Outline PCB Option Board	
1	Outline PCB ROM Board	
1	Case (ROM Cartridge)	
1	Enclosure Power Supply	8729323
1	Panel Rear	
1	Case Top	8719438
1	Button Reset, Front	8719440
1	Button Reset, Rear	8719441
1	Cable Signal Floppy Disk	8709447
1	Cable AC in	
1	Cable Switch (AC Power to Switch-Line)	8709555
1	Cable Switch (AC Power to Switch-Neutral)	8709554
1	Fan	8790412
1	Speaker	8490009
1	Cable, Speaker	

Tandy 1001 Main Logic Sub Assembly

Symbol	Description	RS Part No.
	Main Logic T1000 HD PCB Rev. "A"	8709556A
C1,5,11,12, 14,15,16, 17,20,21, 28-39,47- 50,52-57, 77-81,84- 87,89-91, 93,95,98, 102,106, 116,117, 122,123, 128	Capacitor 0.1 mfd 50v 80% Axial	8374104
C6	Capacitor 0.022 mfd 50/63v 10%	8393225
C13,51, 82,104	Capacitor 22 mfd 16v ±20 Axial	8316221
C18,19,22, 24,27,46, 92,96,97, 99	Capacitor 20 pfd 50v +80-20	8300204
C25	Capacitor 180 pfd 50v 10%	8301184
C40-43	Capacitor 68 pfd 50v 10%	8300684
C44,45	Capacitor 0.01 mfd 50v 20%	8303104
C54A,118- 121	Capacitor 470 pfd 50v 10%	8301474
C76	Capacitor 0.47 mfd 50v 80/20%	8384475
C85A,107, 26	Capacitor 10 mfd 16v Axial	8316101
C88,109, 126	Capacitor 0.1 mfd 50v 80%	8304104
C94,100, 110-115	Capacitor 2200 pfd 50V 10%	8302224
C101,103	Capacitor 2.2 mfd 16v Lytic Axial	8315221
C108	Capacitor 10 mfd 10v 20% TANT Radial	8336101

Tandy 1001 Main Logic Sub Assembly

Symbol	Description	RS Part No.
C124	Capacitor 100 mfd 6.3v TANT Radial	8337100
C125	Capacitor 330 pfd 50v 5%	8301332
CR1	Diode 1N5235 6.8v	8150235
CR6	Zener Diode 1N4148 75v	8150148
E5,6,8,9, 20-22	Staking Pins	8529014
F1	Fuse, 0.25A Pico	8479034
FB1	Ferrite Bead	8419014
J2	Connector, 2-pin Straight Header	8519193
J3,4	Connector, 6-pin Rt. Angle	8519095
J5	Connector, 8-pin	8519203
J6	Connector, Dual 17-pin Straight Header	8519120
J7	Connector, 9-pin St. Frict. Lock	8519191
J8,9,10	Connector, Dual 31-pin Straight Card Edge	8519236
J12	Connector, 9-pin Rt. Angle Male "D" Sub (Low Cost, Snap In)	8519235
J13	Connector, 9-pin Rt. Angle Female "D" Sub	8519245
J14	Connector, Dual RCA Phono Jack Rt. Angle	8519213
J14B-R81	Capacitor, 10 mf 25V Lytic Non	8396101
Q1	Transistor 2N3906	8100906
Q2	Transistor VMOS VN0104N3	8190104
Q3	Transistor 2N3904	8110904
R1	Resistor 0 ohm 1/4 watt 5%	8290000
R2,16,18, 24,29, 53,75	Resistor 2.2K ohm 1/4 watt 5%	8207222
R3	Resistor 82.5K ohm 1/4 watt 5%	8200382
R4 (from J10-B30 to ground)	Resistor 560 ohm 1/4 watt 5%	8207156
R5,8,12, 13	Resistor 1 MEG ohm 1/4 watt 5%	8207510

Tandy 1001 Main Logic Sub Assembly

Symbol	Description	RS Part No.
R6,7,10, 11,14,21, 23,32,52, 68,69, 66A,67	Resistor 10K ohm 1/4 watt 5%	8207310
R9	Resistor 680K ohm 1/4 watt 5%	8207468
R17,28,36, 37,40-45, 32A	Resistor 33 ohm 1/4 watt 5%	8207033
R19	Resistor 330 ohm 1/4 watt 5%	8207133
R20,26,27, 48,70, 76,82 (1 from U101-19 to ground)	Resistor 4.7K ohm 1/4 watt 5%	8207247
R25,35	Resistor 910 ohm 1/4 watt 5%	8207191
R28A	Resistor 27 ohm 1/4 watt 5%	8207027
R29A,75A	Resistor 470 ohm 1/4 watt 5%	8207147
R34,46, 47,72	Resistor 1K ohm 1/4 watt 5%	8207210
R46A,47A	Resistor 47 ohm 1/4 watt 5%	8207047
R54,65	Resistor 680 ohm 1/4 watt 5%	8207168
R55	Resistor 1.2K ohm 1/4 watt 5%	8207212
R56	Resistor 3.3K ohm 1/4 watt 5%	8207233
R57	Resistor 1.1K ohm 1/4 watt 5%	8207211
R58	Resistor 750 ohm 1/4 watt 5%	8207175
R59	Resistor 270 ohm 1/4 watt 5%	8207127
R60	Resistor 22 ohm 1/4 watt 5%	8207022
R61	Resistor 620 ohm 1/4 watt 5%	8207162
R62	Resistor 75 ohm 1/4 watt 5%	8207075
R63	Resistor 2.7K ohm 1/4 watt 5%	8207227
R64,80,81	Resistor 100K ohm 1/4 watt 5%	8207410
R66,88	Resistor 10 ohm 1/4 watt 5%	8207010
R73	Resistor 9.1K ohm 1/4 watt 5%	8207291
RP1	Resistor pak 10K ohm 8-pin sip	8292310
RP2,3	Resistor pak 1K ohm 8-pin sip	8290212
RP4	Resistor pak 10K ohm 10-pin sip	8290010

Tandy 1001 Main Logic Sub Assembly

Symbol	Description	RS Part No.
RP5	Resistor pak 33 ohm 16-pin dip	8290044
RP6	Resistor pak 33 ohm 8-pin sip 1/8w	8295033
RP7	Resistor pak 4.7K ohm 8-pin sip	8292246
RP8	Resistor pak 2.2K ohm 8-pin sip	8290039
S1	Switch, Reset	8489065
U1,40,107, 109,111	IC 74LS04 Hex Inverter	8020004
U6,29, 58,44	IC 74F04 Hex Inverter	8015004
U9	IC 128K ROM	8040128
U9,10	Socket 28-Pin DIP	8509007
U11,12,25-28,33,34, 48,49,54, 55,65-68	IC 64K x 1 Dram 150NS	8043665
U11,12,25-28, 33,34,48,49, 54,55,65-68, 96	Socket 16-Pin DIP	8509003
U13,18,42 43,59,60, 82,113	IC 74LS244 Octal Buffer	8020244
U14,62,97	IC 74LS245 Tranceiver	8020245
U14,53,62, 97,103	Socket 20-Pin DIP	8509009
U15,16, 37,23,47	IC 74F109 JK Flip Flop	8015109
U17,51,87, 93,98,112	IC 74LS32 Quad 2-IN OR	8020032
U19	LM339 Quad Comparato	8050339
U22,70, 78,117	IC 74LS08 Quad 2-IN AND	8020008
U24	IC 7407 Hex Buffer	8000007
U29-3 to 29-7	Capacitor 220 pfd 50v 10%	8301223

Tandy 1001 Main Logic Sub Assembly

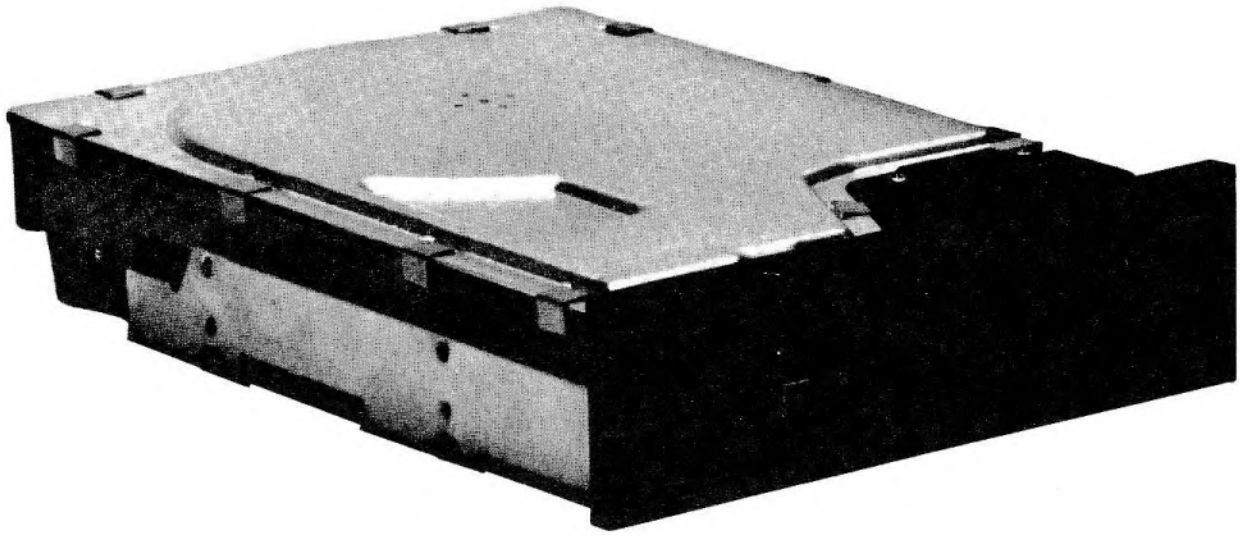
Symbol	Description	RS Part No.
U30, 115	IC 74LS112 J K Flip Flop	8020112
U31	IC 74LS161A Counter	8020161
U35,56	IC 74LS374 Flip Flop	8020374
U36,41, 57,61	IC 74LS373 Octal Latch	3020373
U38	IC 74F138 Multiplexer	8015138
U39	IC 74F161 Counter	8015161
U45	IC 8284A Clock Generator	8040284
U45	Socket 18-Pin DIP	8509022
U46,53, 80,103	IC 82S153	8075153
U46	Socket 20-Pin DIP	8509024
U50	IC 74LS195A Shift Register	8020195
U52	IC 8272 FDC	8040272
U52,76,88, 101,108	Socket 40-Pin DIP	8509002
U58-pin 8	Resistor 68 ohm 1/4 watt 5%	8207068
U63	IC 8259A Interupt Controller	8040259
U63	Socket 28-Pin DIP	8509025
U64	IC 8088 CPU	8048088
U64	Socket 40-Pin DIP	8509023
U69	IC FDC9216 Data Seperator	8040216
U69	Socket 8-Pin DIP	8509011
U71,99	IC 74LS273 Octal Flip Flop	8020273
U72-75	IC 74ALS253 Multiplexer	8025253
U76	IC Semi-Custom Video Array	8079001
U77	IC 74LS86 Quad 2-IN OR	8020086
U79	IC 74LS138 Decoder	8020138
U81	IC 74S260 Dual 5-IN NOR	8010260
U83	IC 74LS38 Quad 2-IN NAND Buffer	8020038
U84	IC 7416 Hex Inverter	8000016
U85	IC 74LS14 Hex Inverter	8020014
U86	IC 74LS02 2-IN NOR	8020002
U88	IC MCM6845	8040845
U89	IC 74LS157 Quad Multiplexer	8020157
U90	IC 74LS153 Dual Multiplexer	8020153
U91	IC 74LS164 Shift Register	8020164

Tandy 1001 Main Logic Sub Assembly

Symbol	Description	RS Part No.
U92	IC 74LS00 Quad 2-IN NAND	8020000
U94, 104, 116	IC 74LS74 Flip FLop	8020074
U96	IC SN76496 Tone Generator	8040496
U100, 106	IC 74LS174 Flip Flop	8020174
U101	IC 8255A-5 Program Interface	8040255
U102	IC 74LS05 Hex Inverter	8020005
U105	IC 14529	8030529
U108	IC Custom Gate Array, Printer	8041087
U110	IC 74LS125A Quad Buffer	8020125
U114	IC 8253-5 Timer	8040253
U114	Socket 24-Pin DIP	8509001
U118	LM386N-1 Audio Amp	8050386
U119	LM358	8050358
VR1	Regulator 78L05, ACP +5v	8052805
Y1	Crystal 8 Mhz (18pf Loading Capacity)	8409006
Y2	Oscillator 28.63636 Mhz 50ppm	8409039

Component Information

TM252
RIGID DISK DRIVE
PRODUCT SPECIFICATION AND USER'S MANUAL



Tandon CORPORATION
20320 PRAIRIE STREET
CHATSWORTH, CALIFORNIA 91311

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However, while every effort has been made to keep the information contained herein current and accurate as of the date of publication, no guarantee is given or implied as to its accuracy.

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SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

This manual provides useful information to assist the customer when incorporating the Tandon rigid disk drive into a system.

Tandon Corporation's TM252 drive is a full feature, 12.75 megabyte, one-half height, 5-1/4-inch, rigid disk drive. It is a compact data storage device containing two 130-millimeter plated aluminum recording platters and four recording heads within a sealed housing.

1.1 SCOPE OF THE DOCUMENT

Section 1 of this manual contains a general description of the disk drive. Section 2 contains the product specifications. Section 3 provides information on operation of the drive.

1.2 PURPOSE OF THE DRIVE

The 5-1/4-inch disk drive is a rotating disk memory device designed for random access data storage and retrieval. Typical applications include word processing systems, entry level microprocessor systems, intelligent calculators, program storage, small business computer systems, and any application in which low cost, random access data storage is required.

1.3 MAJOR FEATURES

MICROPROCESSOR CONTROL

The TM252 drive features an onboard microprocessor, providing five major functions:

1. Self-calibration on power-up.
2. Buffered seek timing for improved access times.
3. Improved positioning with reduced hysteresis.
4. Write current switching for optimal recording quality.
5. Power and track fault detection.

DAISY CHAIN CAPABILITY

The drive provides the address selection and gating functions necessary to daisy chain a maximum of four units at the user's option. The last drive on the daisy chain terminates the interface. The terminations are accomplished by a resistor array plugged into a DIP socket.

INDUSTRY STANDARD INTERFACE COMPATIBILITY

The drive is compatible with controllers that use an ST506 industry standard interface.

AIR FILTRATION

A self-contained, recirculating air filtration system supplies clean air through a 0.3-micron filter. A secondary absolute filter is provided to allow pressure equalization with the ambient atmosphere without contamination. The entire head-disk-actuator compartment is maintained at a slightly positive pressure to further ensure an ultraclean environment.

COMPACT SIZE

The reduced height of the drive occupies only one-half the mounting space required for a conventional drive.

1.4 FUNCTIONAL DESCRIPTION

The drive is fully self-contained, and requires no operator intervention during normal operation. During the power-up sequence, the spindle motor reaches 3,600 RPM, and the positioning mechanism recalibrates the recording heads to Track 0. At this time, a Ready signal on the interface indicates the drive is ready for operation.

The head is positioned over the desired track by means of a four-phase stepper motor/band assembly and its associated electronics. This positioner uses a one-step rotation to cause a one-track radial movement. Subsequently, the recording heads can be positioned over the desired cylinders, and the data can be read or written from the appropriate track by selecting the desired head.

Typically, the drive uses MFM write and read data recording methods. Data recovery electronics include a low-level read amplifier, differentiator, a zero-crossover detector, and digitizing circuits. No data encoding or decoding feature is provided on the drive.

The drive has the following sensor systems:

1. An optical Track 0 switch senses when the Head/Carriage Assembly is positioned at Track 0.
2. An index sensor, which consists of a magnetic pick-up and index hole positioned to provide an analog signal when an index hole is detected.

1.5 PHYSICAL DESCRIPTION

A representative drive is shown in Figure 1-1. The drive contains 130 millimeter storage media that rotate at 3,600 RPM, using a direct drive, brushless D. C. motor. The recording is accomplished by non-contact standard recording heads that are moved by an open loop, precision split band positioning device and stepper motor.

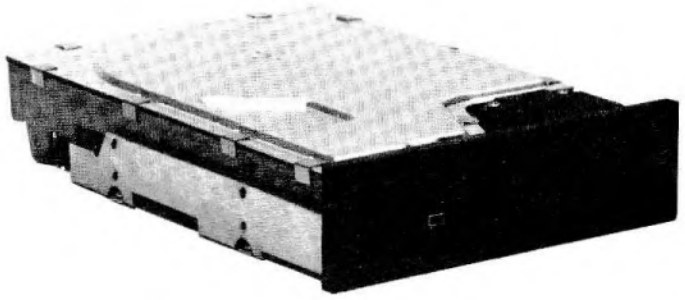


FIGURE 1-1
DISK DRIVE

The Head Disk Assembly is enclosed in a sealed cast aluminum housing, which includes an air filtration system to ensure a contamination-free environment. The housing is shock mounted to a metal frame that has threaded holes on the sides and bottom for mounting the drive onto a chassis. An optional snap-on front cover may be attached.

In addition, the drive includes the read/write and control electronics, servo spindle control electronics, and an index sensor.

SECTION 2

PRODUCT SPECIFICATIONS

INTRODUCTION

This section contains the mechanical and operational, reliability and environmental specifications for the TM252 disk drives.

2.1 MECHANICAL SPECIFICATIONS

The mechanical and physical dimensions are contained in Figure 2-1.

2.2 ELECTRICAL AND OPERATIONAL SPECIFICATIONS

The electrical and operational specifications are contained in Table 2-1. Typical starting current requirements at nominal voltage are contained in Figure 2-2.

2.3 RELIABILITY SPECIFICATIONS

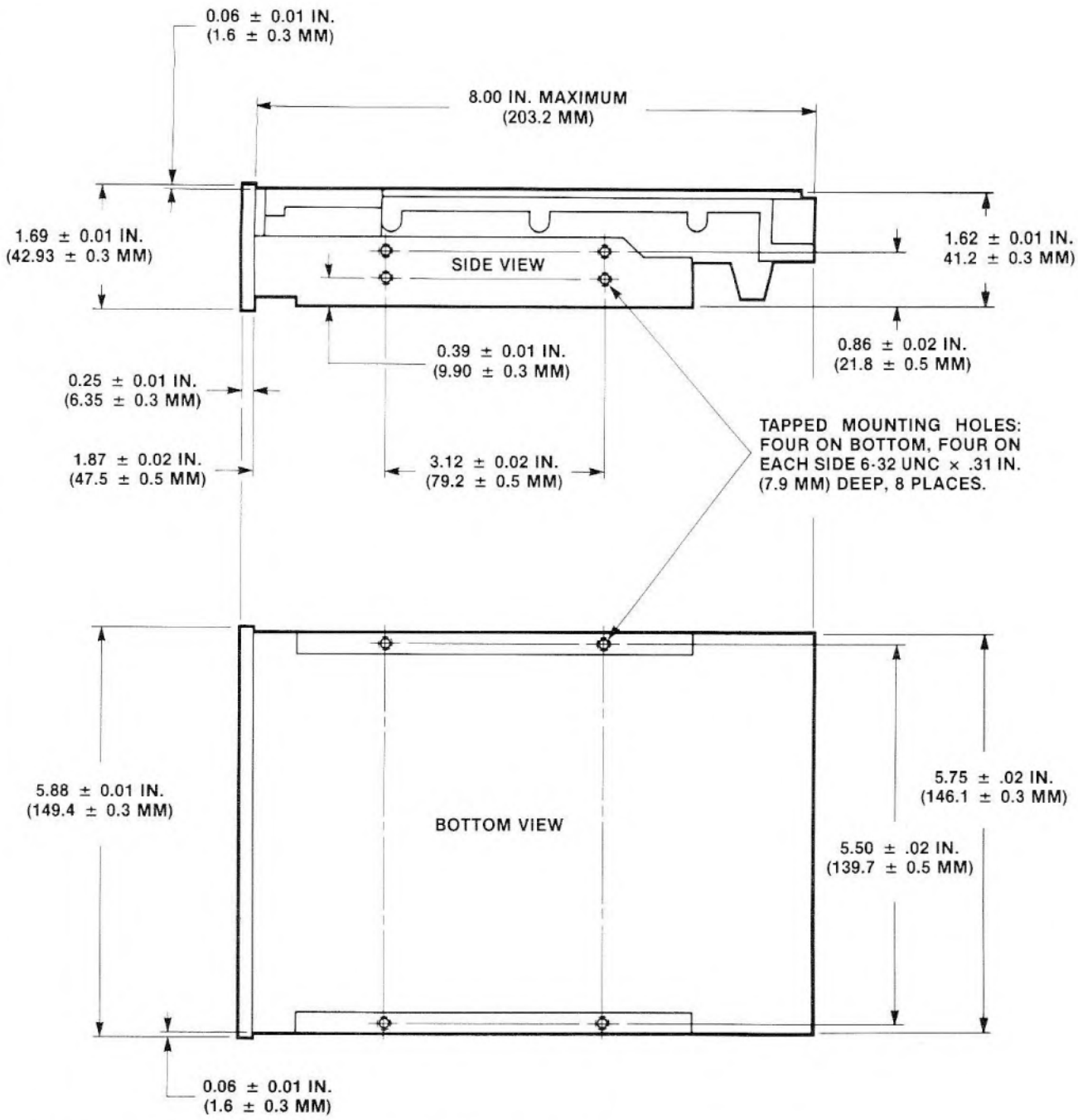
The reliability specifications are contained in Table 2-2.

2.4 ENVIRONMENTAL SPECIFICATIONS

The environmental specifications are contained in Table 2-3.

This product is recognized under U. L. EMRT2, Component-Data Processing Equipment, Electronic.

Certified.



NOTE: WEIGHT IS 3.25 POUNDS, 1.47 KILOGRAMS, MAXIMUM.

FIGURE 2-1
DISK DRIVE OUTLINE DRAWING

TABLE 2-1
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Media	Hardcoated, 130 millimeter, plated aluminum disk
Number of Disks	2
Tracks Per Inch	345 TPI
Spacing, track to track	2.9 milinches
Number Of Cylinders	306 cylinders
Number Of Tracks	1,224 tracks
Disk Speed	3,600 RPM ± 1 percent
Average Latency	8.33 milliseconds
Start Time	15 seconds maximum
Stop Time	15 seconds maximum
Seek Time, track to track	3 milliseconds
Head Settling Time, last track accessed	15 milliseconds
Average Access Time, including head settling time, 3 millisecond step rate	321 milliseconds
Average Access Time Using Buffered Seek, including head settling time	85 milliseconds
Transfer Rate	5 megabits per second

TABLE 2-1 (CONTINUED)
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Maximum Flux Reversal Density	9,090 FRPI
Unformatted Capacity Per Drive	12.76 megabytes
Unformatted Capacity Per Surface	3.19 megabytes
Unformatted Capacity Per Track	10.4 kilobytes

POWER REQUIREMENTS

Start Up: + 12 volts D. C., 2.0 amperes typical, 2.4 amperes maximum, not to exceed 12 seconds.

Running: + 12 volts D. C. ± 10 percent, 1.4 amperes typical, 1.8 amperes maximum with no more than 50 millivolts Periodic and Random Deviation (PARD).

+ 5 volts D. C. ± 5 percent, 0.5 amperes typical, 0.8 amperes maximum running, with no more than 50 millivolts PARD.

There are no restrictions in sequencing supplies on or off.

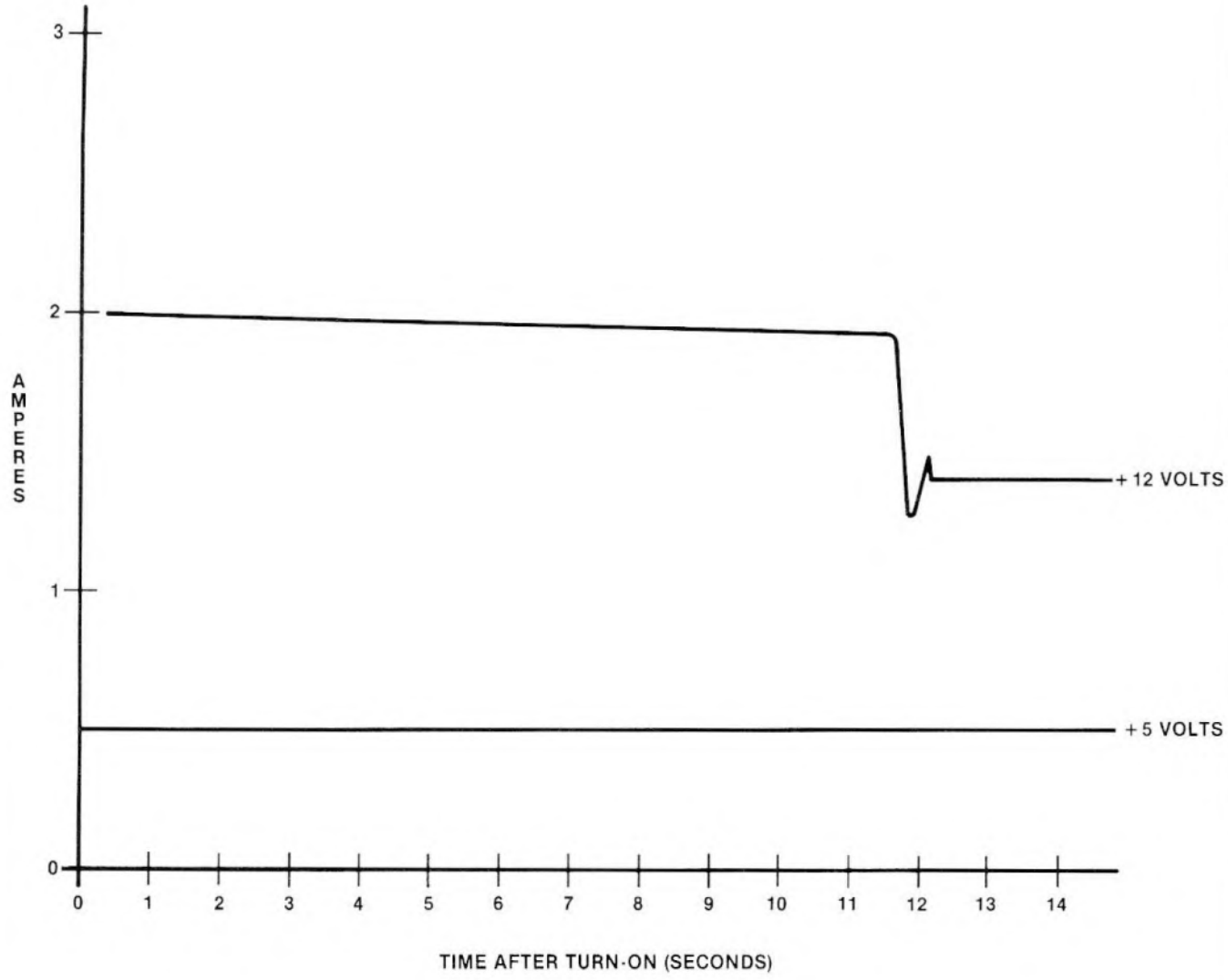


FIGURE 2-2
TYPICAL STARTING CURRENTS

TABLE 2-2
RELIABILITY SPECIFICATIONS

SOFT AND HARD READ ERROR RATES, EXCLUSIVE OF MEDIA DEFECTS

For data that has been verified previously as error free, and when used in conjunction with a data separator and phase lock loop of good design, the recoverable (soft) read error rate for any subsequent read operation shall not exceed one error in 1×10^{10} bits transferred. A recoverable read error is an error that may be corrected within five attempts to reread the data.

The nonrecoverable (hard) read error rates shall not exceed one error in 1×10^{12} bits transferred. A nonrecoverable read error is an error that may not be corrected within five attempts to reread data, providing that the writing of the data previously has been verified as correct. The seek error rate is not to exceed one error in 1×10^{6} seeks.

MEDIA DEFECTS

Any defects on the media surface will be identified on a defect map provided with each drive. This defect map will indicate the head number, track number, and number of bytes from index for each defect. Each defect shall be no longer than 16 bits. More than one defect per track is to be counted as one defect. Cylinders 000 and 001 are guaranteed error free.

The defect map is offered as a guide only. The number of defects and their location can change due to customer system variations such as data separators.

NOTE

Prior to shipment from the factory, the heads are parked at Cylinder 305. This must be done each time the drive is to be relocated, and should be done prior to a power shutdown sequence.

Maximum Allowable Defects	4 per surface, 10 per drive
Mean Time Between Failures	11,000 power on hours (typical useage)
Mean Time To Repair	30 minutes
Component Design Life	5 years
Preventative Maintenance	Not required

TABLE 2-3
ENVIRONMENTAL SPECIFICATIONS

Ambient Temperature	
Operating	4°C to 50°C, 39°F to 122°F
Nonoperating	−40°C to 60°C, −40°F to 140°F
Temperature Gradient	
Operating	10°C per hour, 18°F per hour
Nonoperating	Below that causing condensation
Relative Humidity	8-to-80 percent, noncondensing
Relative Humidity Gradient	
Operating	20 percent per hour
Nonoperating	Below that causing condensation
Maximum Wet Bulb Temperature	26°C, 78.8°F, without condensation
Elevation	
Operating	Density Altitude: −457 to 3,050 meters, −1,500 to 10,000 feet
Nonoperating	−457 to 12,195 meters, −1,500 to 40,000 feet
Heat Dissipation	78 BTU per hour, 22.5 watts

TABLE 2-3 (CONTINUED)
ENVIRONMENTAL SPECIFICATIONS

Vibration	
Operating	The drive will operate with a read/write error rate no greater than the specified limit while subjected to vibration levels at 5 to 500 Hz of 0.5 G, maximum, input. Dwell at resonant frequencies for 30 minutes. Resonant frequencies are defined as frequencies where 1.0 G or higher in/out response is created.
Nonoperating	A constant acceleration input may be applied with the desired frequency swept, stopping at resonant frequencies for 30 minutes. The drive will meet specified error rates and have no additional media defects after vibraiton levels at 5 to 500 Hz of 2 G's, maximum, are applied in each of the 3 mutually perpendicular axes, 1 axis at a time.
Shock	
Operating	The drive will operate with an error rate no greater than the specified limit while a half sine wave shock pulse of 10 G's with a duration of 11 milliseconds is applied in either direction, in each of the 3 perpendicular axes, 1 axis at a time.
Nonoperating	The drive will survive a series of 6 drops, 1 each side, top and bottom, a minimum of 40 G's squarewave shock pulse of 10 milliseconds duration.

SECTION 3

OPERATION

INTRODUCTION

This section contains information pertinent to the handling, inspection, installation, and operation of the TM252 drive.

3.1 UNPACKING THE DRIVE

Each drive is shipped in a protective container which, when bulk packaged, minimizes the possibility of damage during shipment.

The following procedure is recommended for unpacking the drive.

1. Place the shipping container on a flat work surface.
2. Visually examine the shipping container for damage.
3. Cut the tape on the shipping container.
4. Remove the foam lid and pads from the shipping container.
5. Remove the inner container.
6. Remove the drive from the inner container.
7. Place the drive on a foam lined surface.
8. Notify the carrier immediately if any damage is found.

CAUTION

Do not manually rotate the stepper motor or spindle motor. Damage to the heads and disk may result.

NOTE

The inside chamber of the drive is a sealed compartment that must not be opened.

When returning the drive to the service center, park the heads at cylinder 305 (see page 2-6). Be sure to use the prior steps in reverse order, and ensure the foam stiffeners are in the proper location, with the cardboard dividers properly in place between the drives (see Figure 3-1).

3.2 PREINSTALLATION CHECKOUT

Before applying power to the drive, inspect for the following:

1. Ensure the front panel is secure.
2. Ensure the circuit board is secure.
3. Ensure the connectors are firmly seated.
4. Ensure there is no debris or foreign material between the frame and the head/disk casting.
5. Ensure the head/disk housing can move freely on the shock mounts of the frame.
6. Ensure the termination resistor pack and jumper blocks are firmly seated and in the correct configuration.

3.3 MOUNTING THE DRIVE

The drive can be mounted in any vertical or horizontal plane. Eight 6-32 tapped holes are provided for mounting: four on each side and four on

the bottom of the frame (see Figure 2-1). The drive is manufactured with some critical internal alignments that must be maintained. Hence, it is important the mounting hardware does not introduce significant stress on the drive.

Any mounting scheme in which the drive is part of the structural integrity of the enclosure is not permitted. Mounting schemes should allow for adjustable brackets or incorporate resilient members to accommodate tolerances.

DUST COVER

The design of an enclosure should incorporate a means to prevent contamination from loose items, e. g., dust, lint, and paper chad since the drive does not have a dust cover.

FREE AIR FLOW

When the drive is mounted so the components have access to the free flow of air, normal convection cooling allows operation over the specified temperature range (see Table 2-3).

CONFINED ENVIRONMENT

When the drive is mounted in a confined environment, air flow must be provided to maintain specified air temperatures in the vicinity of the motors and the circuit boards.

3.4 INTERFACE CONNECTORS

The electrical interface between the drive and the host system is via three connectors. J1 provides control signals for the drive (see Figure 3-2). J2 provides for the radial connection of read/write data signals (see Figure 3-3). J3 provides for D. C. power (see Figure 3-4).

Table 3-1 contains interface lines. The interface description of the connectors, and the location of each, is contained in this section.

J1/P1 CONNECTOR

Connection to J1 is through a thirty-four-pin circuit board connector. Figure 3-2 contains the dimensions of this connector. The pins are numbered 1 through 34. The recommended mating connector for P1 is 3M ribbon connector P/N 3463-0001, without ears. A key slot is provided between Pins 4 and 6.

J2/P2 CONNECTOR

Connection to J2 is through a 20-pin circuit board connector. Figure 3-3 contains the dimensions of this connector. The recommended mating connector for P2 is 3M ribbon connector P/N 3461-0001, without ears. A key slot is provided between Pins 4 and 6.

J3/P3 CONNECTOR

D. C. power connector J3 is a four-pin AMP Mate-N-Lok connector, P/N 350211-1, mounted on the component side of the circuit board. The recommended mating connector, P3, is AMP P/N 1-480424-0, utilizing AMP pins P/N 60619-4. J3 pins are labeled on the J3 connector (see Figure 3-4). J3 cabling must be 18 AWG, minimum.

GROUND CONNECTOR

A ground connector, located on the rear of the head/disk assembly is Faston AMP P/N 61761-2. The recommended mating connector is AMP P/N 62187-1. To realize error rates (see Table 2-2), it must be connected directly to the centrally located system logic ground via an 18 AWG, minimum, cable.

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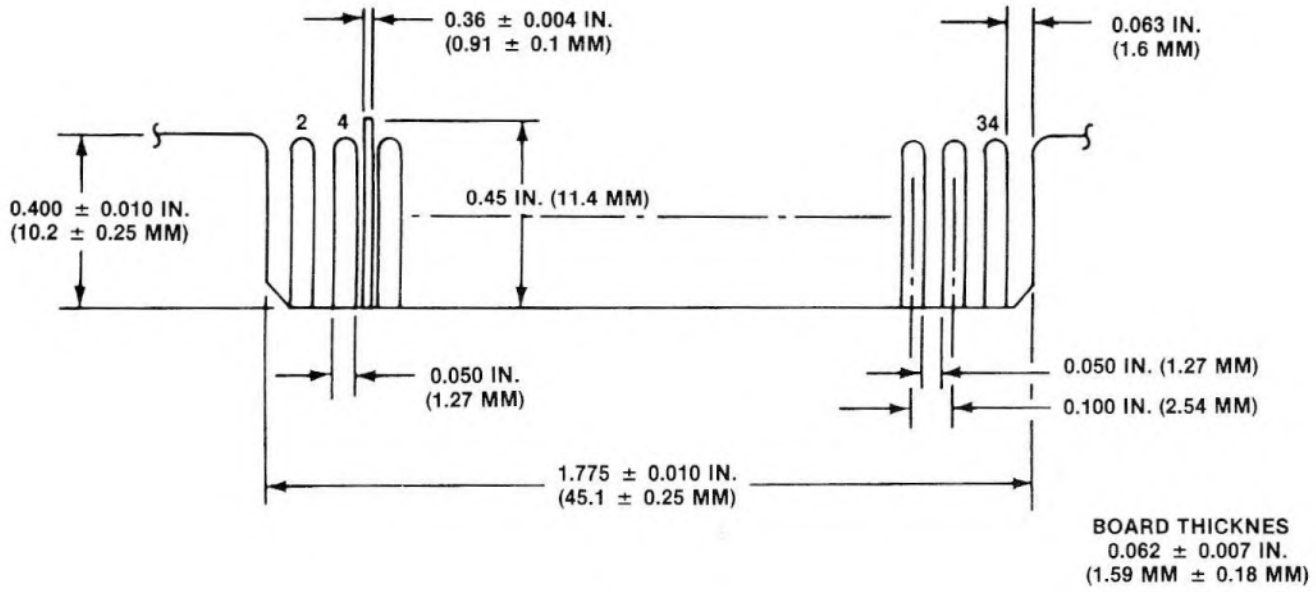


FIGURE 3-2
J1 EDGE CONNECTOR DIMENSIONS

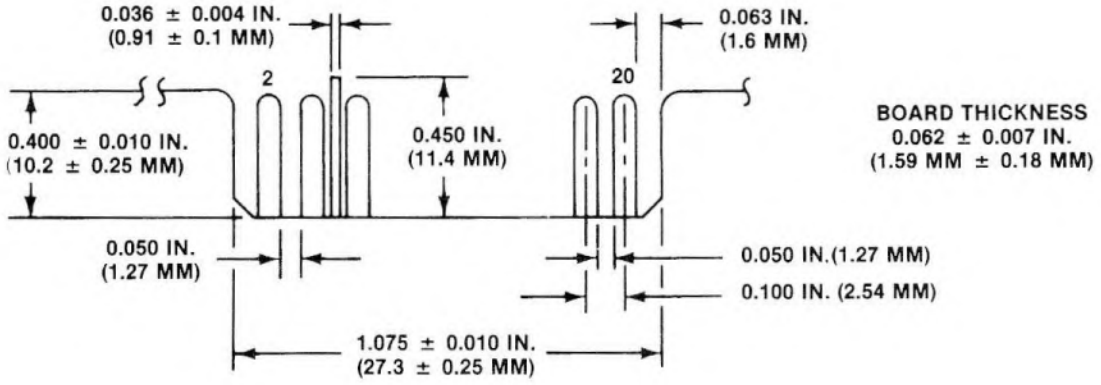


FIGURE 3-3
J2 EDGE CONNECTOR DIMENSIONS

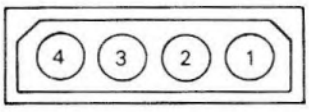


FIGURE 3-4
J3 POWER CONNECTOR

TABLE 3-1
DRIVE INTERFACE SIGNALS AND PIN ASSIGNMENTS

Connector	Interface Pin Number: Signal	Ground	Signal Type	I/O	Name of Signal
P1	2	(1)	S	I	Spare
↑	4	(3)	S	I	Spare
	6	(5)	S	I	Write Gate
	8	(7)	S	O	Seek Complete
	10	(9)	S	O	Track 0
34-Pin	12	(11)	S	O	Fault
Ribbon	14	(13)	S	I	Head Select 2^0
Daisy	16	(15)	—	—	Reserved (To J2-7)
Chain	18	(17)	S	I	Head Select 2^1
↓	20	(19)	S	O	Index
	22	(21)	S	O	Ready
	24	(23)	S	I	Step
	26	(25)	S	I	Drive Select 0
	28	(27)	S	I	Drive Select 1
	30	(29)	S	I	Drive Select 2
	32	(31)	S	I	Drive Select 3
P1	34	(33)	S	I	Direction In
P2	1	(2)	S	O	Drive Select
↑	3	(4)	S	—	Spare
	5	(6)	—	—	Reserved
	7	(8)	—	—	Reserved (To J1-16)
20-Pin	9	(10)	—	—	Spare
Ribbon	11	(12)	—	—	Ground
Radial	13	—	D	I	+ Write Data
↓	14	—	D	I	− Write Data
	15	(16)	—	—	Ground
	17	—	D	O	+ Read Data
	18	—	D	O	− Read Data
P2	19	(20)	—	—	Ground
P3	1			—	+ 12 volts D. C. In
4-Pin	2			—	+ 12 volts D. C. Return
Radial	3			—	+ 5 volts D. C. Return
P3	4			—	+ 5 volts D. C. In

NOTES:

S = Single Ended
D = Differential
I = Drive Input
O = Drive Output

3.5 INTERFACE LINE DESCRIPTIONS

The interface for the TM252 drive is available in one configuration. It is compatible with industry standard drives. Compatibility is defined as using the same pin assignment where the signal and function are common. Table 3-1 contains pin assignments.

The interface may be connected in the radial or daisy chain configuration (see Figures 3-5 and 3-6).

INPUT CONTROL SIGNALS

The input control signals are of two kinds: those to be multiplexed in a multiple drive system and those that do the multiplexing. The input control signals to be multiplexed are: Reduced Write Current, Write Gate, Head Select Line 2^0, Head Select Line 2^1, Step, and Direction In. The multiplexing signal is Drive Select 0, Drive Select 1, Drive Select 2 or Drive Select 3.

The input signals have the following electrical specifications, as measured at the drive. Figure 3-7 illustrates the recommended circuit.

True: 0.0 volt D. C. to 0.4 volt D. C. at I = −40 milliamperes, maximum

False: 2.5 volts D. C. to 5.25 volts D. C. at I_L = 250 microamperes, maximum (open)

All input signals share a 220/330 ohm resistor pack for line termination. Only the last drive in the chain should have the resistor pack installed.

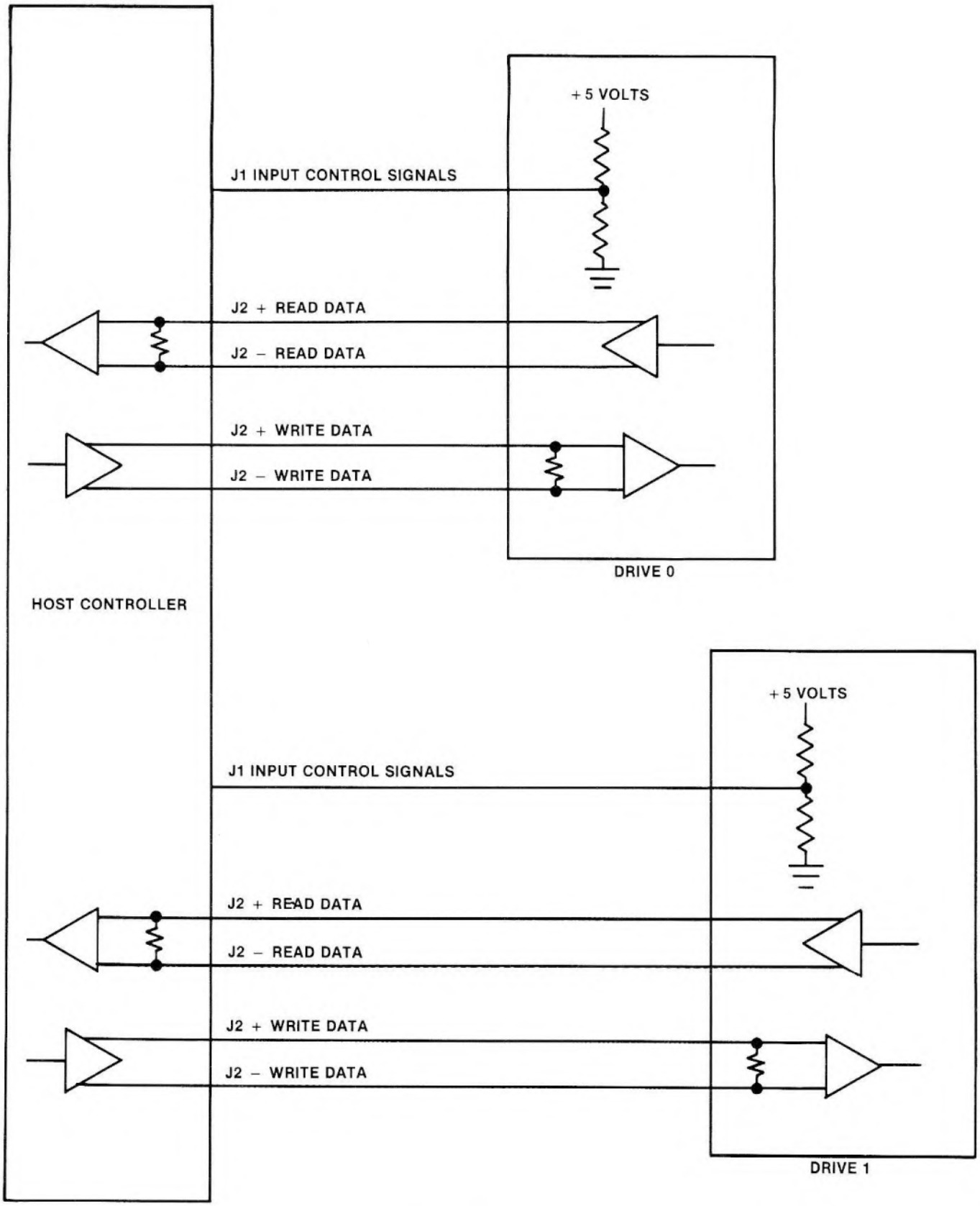


FIGURE 3-5
RADIAL CONFIGURATION

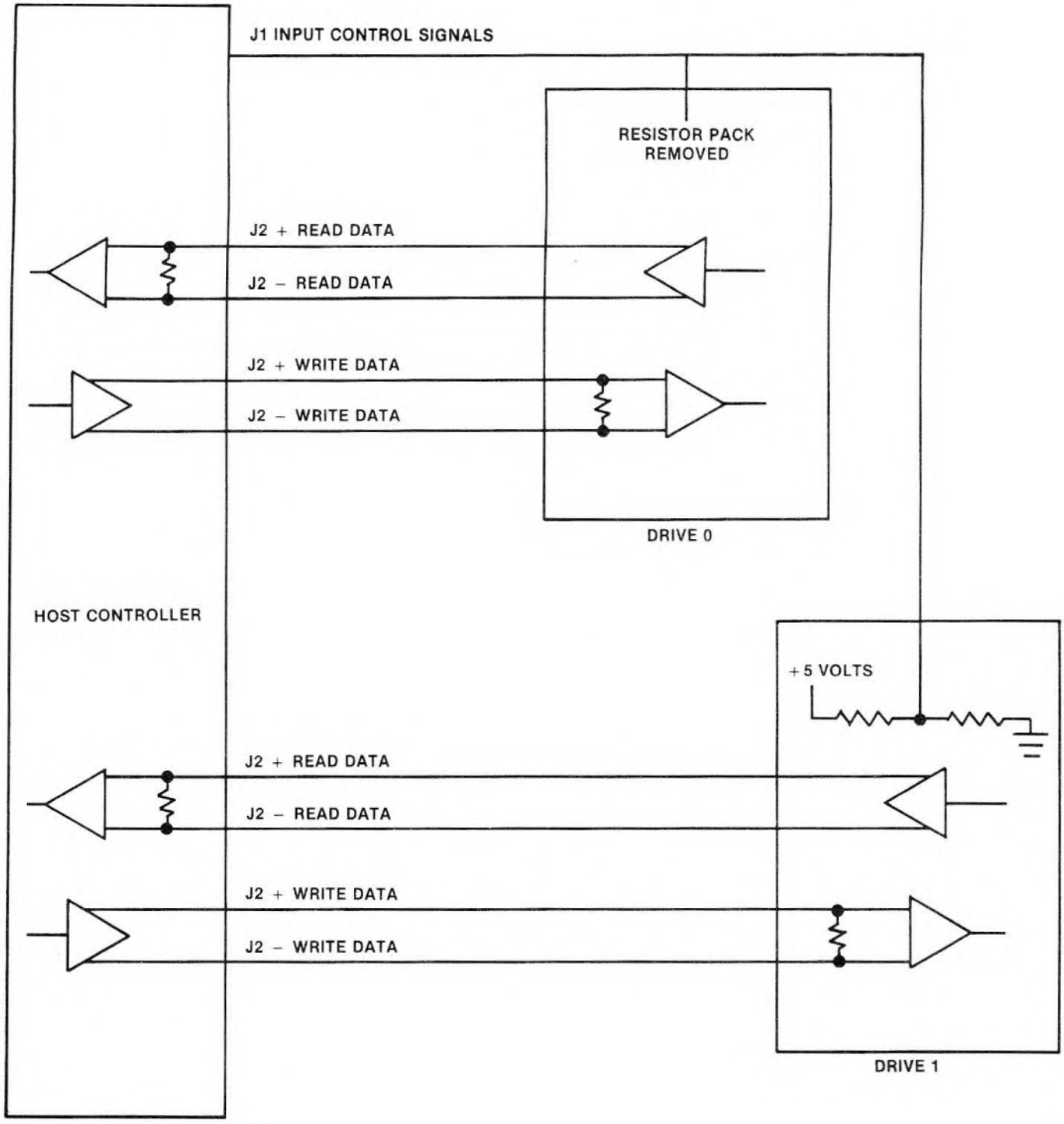


FIGURE 3-6
DAISY CHAIN CONTROL LINES

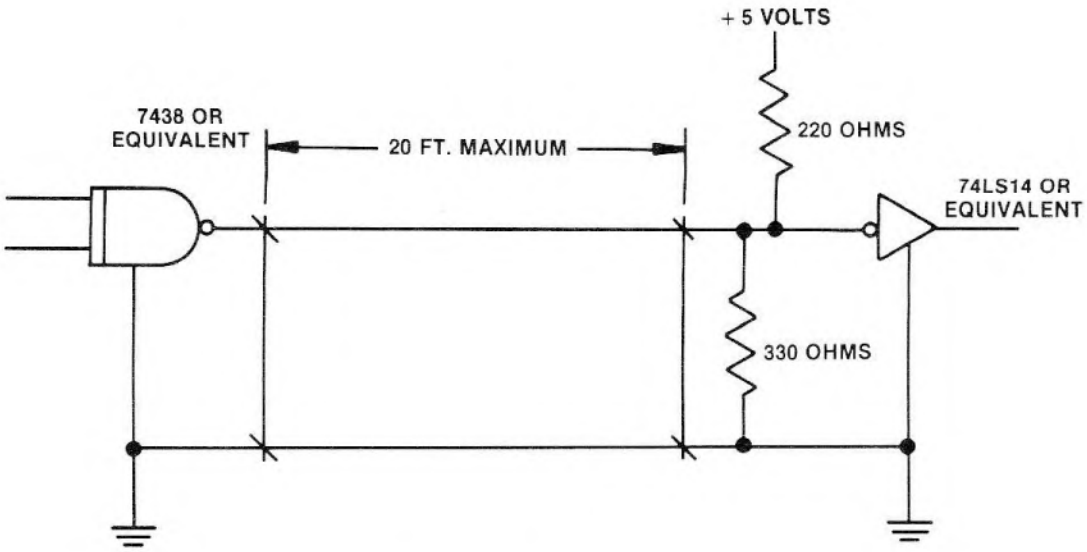


FIGURE 3-7
CONTROL SIGNAL/DRIVER RECEIVER CIRCUIT COMBINATION

WRITE GATE

The active state of this signal or logical zero level enables write data to be written on the disk. The inactive state of this signal enables the data to be transferred from the drive. In addition, the inactive state enables the step pulse to step the read/write actuator.

HEAD SELECT LINES 2^0 AND 2^1

These two lines provide for the selection of each read/write head in a binary coded sequence. Head Select Line 2^0 is the least significant line. The heads are numbered 0 through 3. When all Head Select lines are false, Head 0 is selected. Table 3-2 describes which head is selected for the head select lines.

Head recovery time (head-to-head select, write-to-read recovery, or read-to-write recovery) is 2.4 microseconds, maximum.

STEP

This interface line is a control signal that causes the read/write heads to move with the direction of motion defined by the Direction In line.

The access motion is initiated at the logical true-to-logical false transition or the trailing edge of this signal pulse. Any change in the Direction In line must be made at least 100 nanoseconds before the true-to-false edge of the step pulse. The quiescent state of this line should be held logically false.

The read/write head moves at the rate of the incoming step pulses. The minimum time between successive steps is three milliseconds, except during execution of a buffered seek. The minimum pulse width is one microsecond. Figure 3-8 illustrates the step timing.

Table 3-2
HEAD SELECT LINES

Head Select Lines 2^1	Head Select Lines 2^0	Head Selected
1	1	0
1	0	1
0	1	2
0	0	3

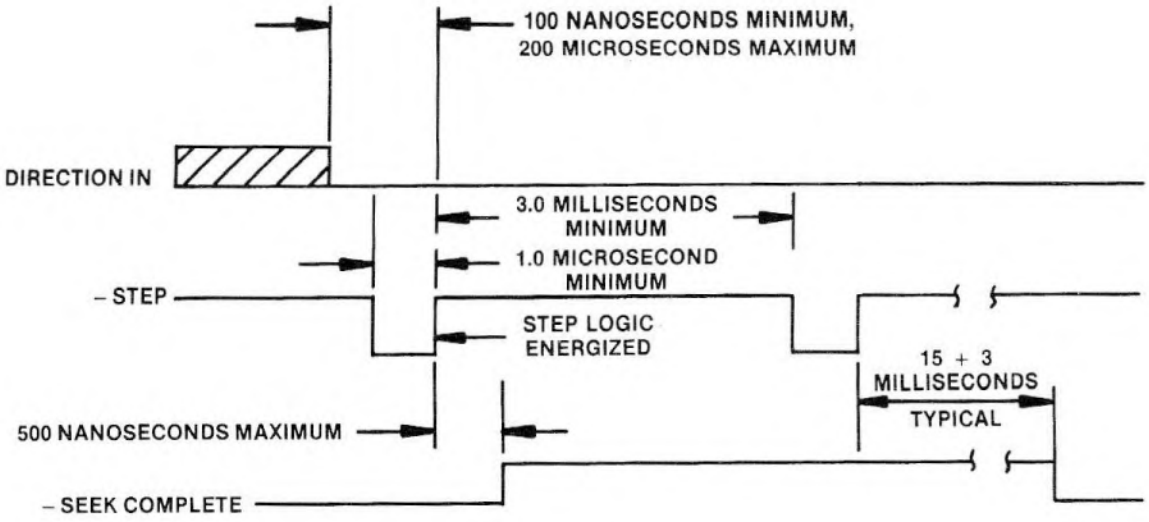


FIGURE 3-8
STEP MODE TIMING

BUFFERED SEEK

The buffered seek uses an onboard microprocessor that calculates the most efficient seek algorithm for the user. The user need only issue step pulses in accordance with the timing shown (see Figure 3-9). Step pulses are issued in a 1:1 ratio to the cylinders moved. If more pulses are issued than there are cylinders left to move, the heads soft stop at the last cylinder.

The pulse repetition rate must not be less than five microseconds. The duty cycle may be varied, provided the one microsecond minimums are met (see Figure 3-9).

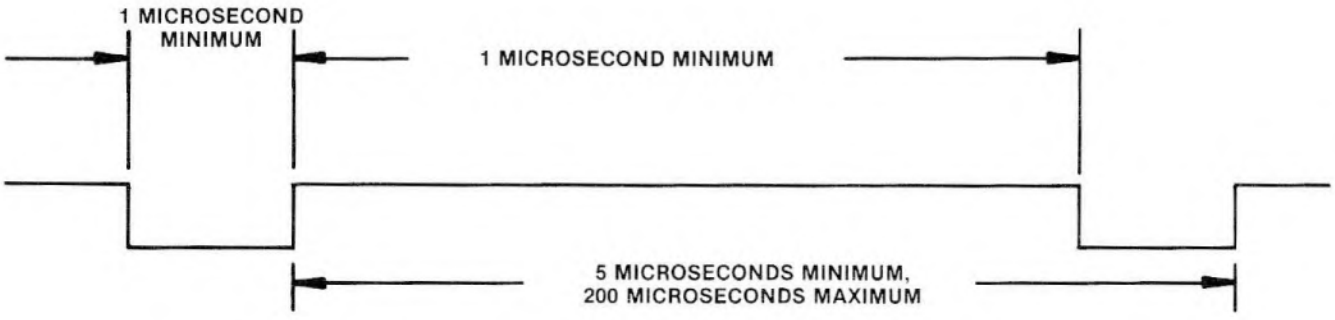


FIGURE 3-9
BUFFERED SEEK STEP PULSES

DIRECTION IN

This signal defines the direction of motion of the read/write head when the Step line is pulsed. An open circuit or logical false defines the direction as "out". If a pulse is applied to the Step line, the read/write heads move away from the center of the disk. If this line is true, the direction is defined as "in", and the read/write heads move in toward the center of the disk.

Seek Complete must be true prior to changing directions and the application of additional step pulses.

REDUCED WRITE CURRENT

The Reduced Write Current input line is terminated, but is not used in the TM252 drive. The microprocessor automatically switches write current.

DRIVE SELECT 0 THROUGH DRIVE SELECT 3

These control signals enable the selected drive's input receivers and output drivers. When logically false, the output drivers are open circuits and the input receivers do not acknowledge signals presented to them.

Selecting the appropriate jumper block at W9 through W12 determines which select line activates the drive.

NOTE

Only one drive may be selected at a time.

OUTPUT CONTROL SIGNALS

The output control signals are driven with an open collector output stage capable of sinking a maximum of 40 milliamperes in a true state, with a maximum voltage of 0.4 volt measured at the driver. When the line driver is in the false state, the driver transistor is off, and the collector cutoff is a maximum of 250 microamperes.

All J1 output lines are enabled by the respective Drive Select lines.

SEEK COMPLETE

The Seek Complete signal goes true when the read/write heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when Seek Complete is false.

Seek Complete goes false:

1. When a recalibration sequence is initiated by the microprocessor at power on because the read/write heads are not over Track 0.
2. 500 nanoseconds, maximum, after the trailing edge of a step pulse or a series of step pulses.
3. When power is momentarily lost, Seek Complete is false when power is restored and remains false until an automatic recalibration is completed.

TRACK 0

The Track 0 signal indicates a true state only when the drive's read/write heads are positioned at Track 0, the outermost data track.

FAULT

The Fault signal is used to indicate a condition exists in the drive that could cause improper writing on the disk. When this line is true, further writing is inhibited, as are other drive functions, until the condition is corrected.

This condition is caused by either the +12 volt or +5 volt supply dropping below the specified limits, and on power up until a successful recalibration sequence is completed.

INDEX

The Index signal is provided once each revolution, 16.7 milliseconds nominal, to indicate the beginning of the track. Normally, this signal is false and makes the transition to true to indicate Index. Only the transition from logical false to logical true is valid.

READY

When true, the Ready signal, together with Seek Complete, indicates that the drive is ready to read, write or seek, and the I/O signals are valid. When this line is false, all controller-initiated functions are inhibited.

The typical time after power on for Ready to be true is fifteen seconds. Track 0, Seek Complete, and Ready come true sequentially during power on.

SELECT STATUS

A Status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The Drive Selected line is driven by a TTL open collector drive (see Figure 3-7). This signal goes active only when the drive is programmed as Drive X, X = 0, 1, 2, or 3, by programming the shunt on the drive, and the Drive Select X line at J1/P1 is activated by the host system.

DATA TRANSFER SIGNALS

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the J2/P2 connector on all drives.

Signal level are defined by RS-422A. Two pairs of balanced lines are used for the transfer of data: MFM Write Data and MFM Read Data. Figure 3-10 illustrates the driver/receiver combination used with the drive for data transfer signals.

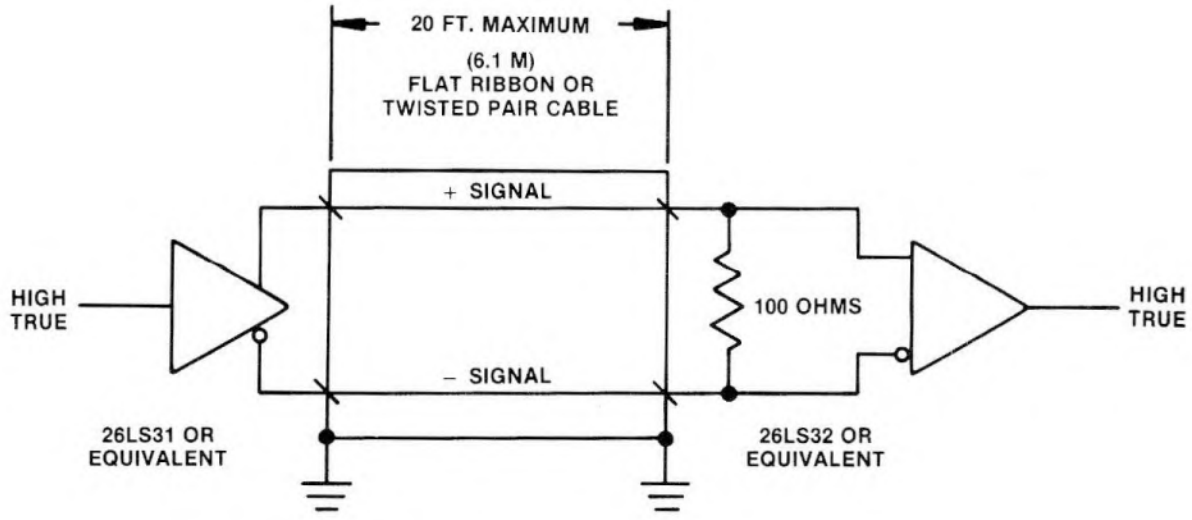


FIGURE 3-10
DATA TRANSFER LINE DRIVER RECEIVER

MFM WRITE DATA

This is a differential pair of lines that define the flux transition to be written on the track. The transition of the +MFM Write Data line going more positive than the −MFM Write Data line causes a flux reversal on the track if Write Gate is active. This signal must be driven to an inactive state, +MFM Write Data more negative than −MFM Write Data, by the host system when in a read mode.

The delay from the leading edge of Write Gate to the Write Data pulse is 400 nanoseconds, maximum.

Host controllers may implement write precompensation circuits that recognize worst case patterns and adjust the write data waveform. Although a value cannot be specified for write precompensation, Tandon suggests a value of 12 nanoseconds for systems using MFM double density recording format starting at cyclinder 128.

MFM READ DATA

The data recovered by reading a prerecorded track is transmitted to the host system via the differential pair of MFM Read Data lines. The transition of the +MFM Read Data line going more positive than the −MFM Read Data line represents a flux reversal on the track of the selected head.

3.6 DRIVE ADDRESS AND OPTION SELECTION

The drive address and option selection is determined by the programmable jumper blocks located on the logic circuit board. If jumper configurations are changed, power should be cycled off and on, so that the microprocessor can recognize the new configuration.

The option programming guide is contained in Table 3-3.

3.7 SHIPPING PACK AND HANDLING

Figures 3-11 through 3-13 provide basic information on recommended design guidelines for packaging systems.

From various drop tests conducted, it has been established that drives subjected to shock loads in excess of forty G's may be damaged and consequently not meet published performance specifications for data reliability, margins, and function.

In order to avoid media or head damage, it is recommended that:

1. Drive mounting designs incorporate some type of shock dampening consideration.
2. Shipping cartons protect the drive within the system to withstand forty G's.
3. Individual drives are handled carefully, e.g., receiving and in-process personnel are property trained, surface mats are used on working surfaces to prevent the possibility of "handling shock," and padding is placed on racks and carts.

Please emphasize the critical aspects of handling these drives to all concerned people. In addition, Tandon provides technical assistance on packing and handling to customers upon request.

Table 3-3
OPTION PROGRAMMING GUIDE

Option Jumper	Function	Factory Programmed, User Accessible	Usage
W15	Drive Select	I	Omit W15 for drive-to-controller lines, enabled when drive not selected.
W16	Index	I	Omit W16 for index-to-controller line, enabled when drive not selected.
RTW7	Read Terminator	I	Install only at the end drive for daisy chain data.
WTW8	Write Terminator	I	Install in all drives for radial data.
S4W9	Drive Select 4	O	Install one of four plugs only. Plug corresponds to drive address
S3W10	Drive Select 3	O	
S2W11	Drive Select 2	O	
S1W12	Drive Select 1	I	
U19	Terminator Pack	I	Install at the end drive only for daisy chain control lines.

NOTES:

O = Omit
I = Install

SECTION 4

TROUBLESHOOTING GUIDE AND REPLACEMENT PROCEDURE

INTRODUCTION

This section is designed to help locate and correct failures related to the drive. Table 4-2 is a troubleshooting guide outlining the problem, its possible cause, and the recommended action. This section also contains parts removal, replacement, and adjustment procedures.

In all cases, the power supply voltages should be checked before proceeding.

4.1 TROUBLESHOOTING GUIDE

TEST EQUIPMENT

The following test equipment, or its equivalent, is recommended:

1. Oscilloscope, Tektronix 465 -- vertical and horizontal sensitivity plus three percent specified accuracy -- with three 10X probes, each with individual ground leads.
2. Counter Timer, Monsanto Model 100B.
3. Digital Voltmeter (DVM), John Fluke Model 800A.

TEST POINTS

Table 4-1 contains each test point by function name. All test points referred to are on the logic board. Figure 4-1 illustrates their location.

TABLE 4-1
TEST POINTS

Test Point	Signal
TP 1, 5, 6	Logic Ground
TP 4	Index
TP 2	Pulse Read Data
TP 7	- Analog Read Data
TP 8	+ Analog Read Data

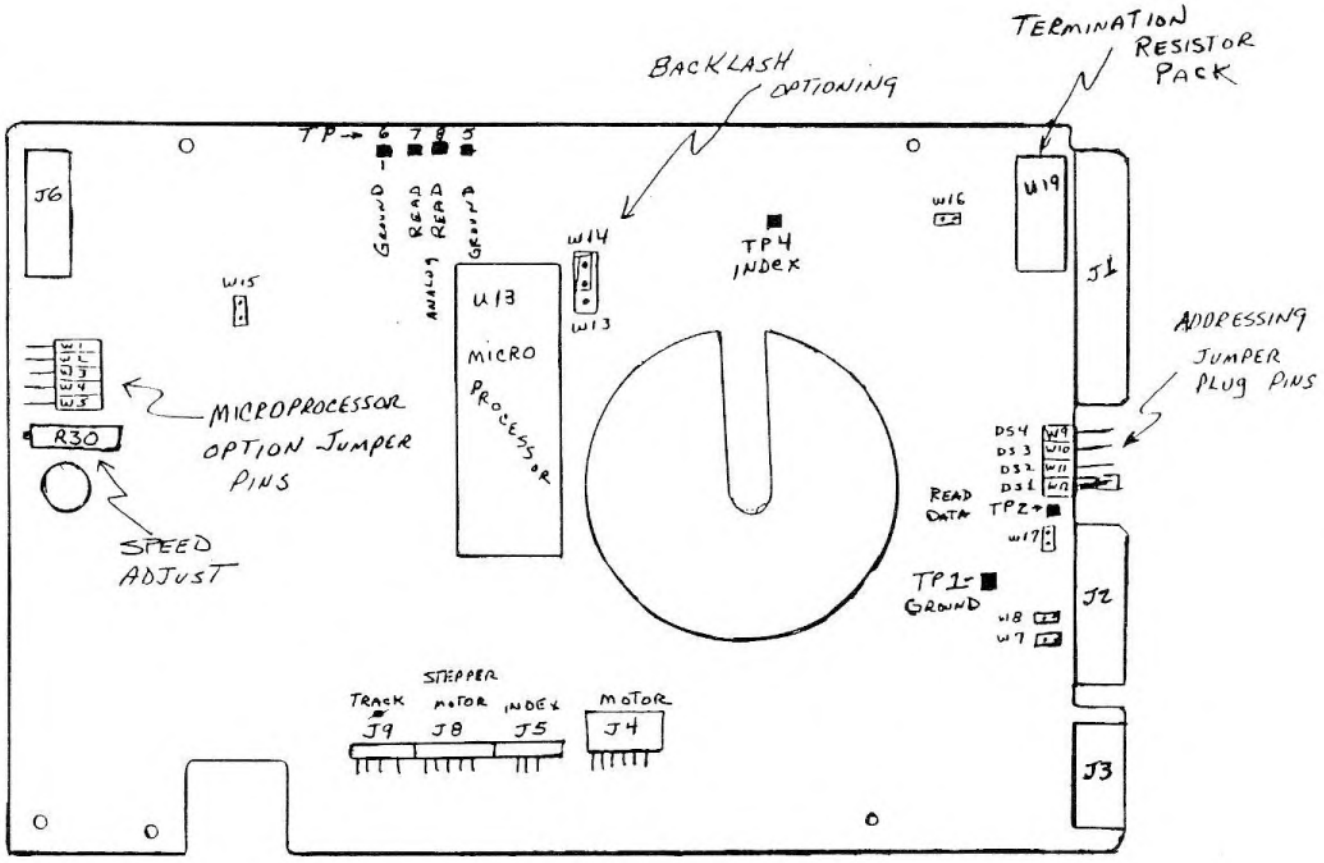


FIGURE 4-1
LOGIC CIRCUIT BOARD

TABLE 4-2
TROUBLESHOOTING GUIDE

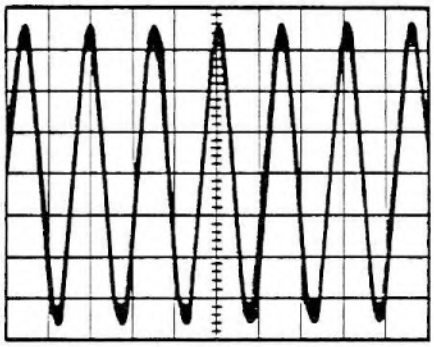
Problem	Possible Cause	Recommended Action
No activity lamp.	Not selected.	Check for correct drive select jumper.
	Lamp not plugged in.	Check Connector P-7, if used.
	Lamp faulty.	Replace lamp.
	Logic board faulty.	Replace logic board.
No index.	Not selected.	Check drive select jumper.
	Index sensor not plugged in.	Check Connector P-5.
	Index sensor misadjusted.	Readjust Index sensor.
	Index sensor faulty.	Replace sensor.
	Logic board faulty.	Replace logic board.
No Track 0	Not selected.	Check drive select jumper.
	Track 0 sensor not plugged in.	Check Connector P-9.
	Track 0 sensor misadjusted.	Readjust Track 0 sensor.
	Track 0 sensor faulty	Replace Track 0 sensor.
	Logic board faulty.	Replace logic board.
Drive not ready.	Not selected.	Check drive select jumper.
	No index.	See "No index."
	No Track 0.	See "No Track 0."
	Motor not up to speed or not turning.	See "Motor not up to speed, not turning."
	Drive does not seek. Drive does not restore.	See "Drive does not seek or restore."

TABLE 4-2 (CONTINUED)
TROUBLESHOOTING GUIDE

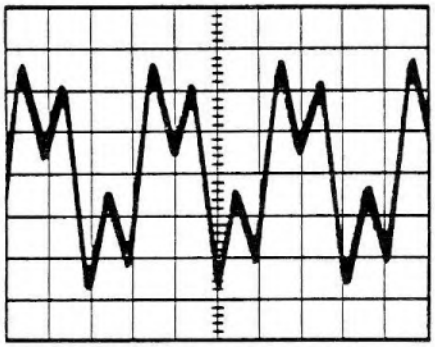
Problem	Possible Cause	Recommended Action
Drive does not seek or restore.	Drive not selected.	Check drive select jumper.
	Stepper motor not plugged in.	Check Connector P-8.
	Logic board faulty.	Replace logic board.
	Spindle motor speed misadjusted.	Readjust spindle motor's speed.
	Stepper motor faulty.	Return to factory for repair.
	Foreign object interfering with positioning arm or damper.	Remove foreign object.
Motor not up to speed, not turning	Spindle motor not plugged in.	Check Connector P-4.
	Faulty logic board - spindle motor circuit	Replace logic board.
	Motor not up to speed.	Adjust spindle speed.
	Motor faulty.	Return to factory for Repair.
Does not read.	Not selected.	Check drive select jumper.
	Heads not selected.	Check head select interface lines.
	Head cable not plugged in.	Check Connector P-6.
	Logic board faulty (see Figure 4-2).	Replace logic board.
	Defective head.	Return to factory for repair.
Does not read.	Improper position.	See "Drive does not seek or restore."
	Drive not ready.	See "Drive not ready."

TABLE 4-2 (CONTINUED)
TROUBLESHOOTING GUIDE

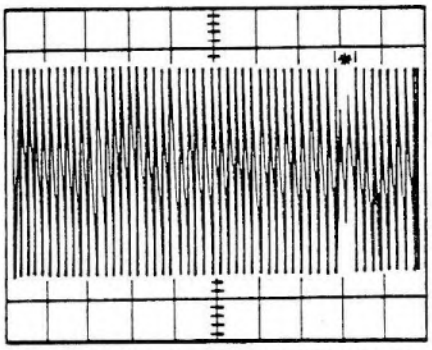
Problem	Possible Cause	Recommended Action
Does not write.	Not Write Gate for writing.	Check Write Gate interface line.
	Not selected.	Check drive select jumper.
	Heads not selected.	See "Does not read."
	Head cable not plugged in.	Check Connector P-6.
	Logic board faulty.	Replace logic board.
	Defective head.	Return to factory for repair.
	Drive not ready.	See "Drive not ready."



ALL ZERO PATTERN



ALTERNATING ONES AND ZEROS



*BIT DROPOUT CAUSED BY MEDIA DEFECT

FIGURE 4-2
READ DATA WAVEFORMS 7 TPR + AND 8 TPR -

4.2 REPLACEMENT PROCEDURES

LOGIC CIRCUIT BOARD ASSEMBLY

Removal

To remove the Logic Circuit Board:

1. Remove the four screws that attach the circuit board to the chassis.
2. Remove J6 via the hole in the circuit board.
3. Remove the Connectors J4, J5, J7, and J8 from the circuit board.
4. Slide the circuit board toward the side of the frame, and lift up on the free side of it.

Replacement

To replace the Logic Circuit Board Assembly, reverse Steps 1 through 4.

Speed Adjustment

To adjust the spindle speed using a digital counter:

1. Attach probe to TP 4.
2. Attach probe ground to frame.
3. Adjust speed control, R30, for a time period of 16.666 milliseconds, $\pm$ 1%.

NOTE

Counter may read between 16.833 and 16.650 milliseconds.

FRONT PANEL L.E.D. ASSEMBLY

Removal

To remove the Front Panel L.E.D. Assembly:

1. Remove the Logic Circuit Board.
2. Remove the L.E.D. Assembly by pressing the center of the Front Panel L.E.D. Assembly with a blunt tool.

NOTE

Press from the inside to the outside of the panel.

3. Remove the square retainer from the assembly.

Replacement

To replace this assembly, reverse Steps 1 through 3.

INDEX ASSEMBLY

Removal

To remove the Index Assembly:

1. Remove the Logic Circuit Board.
2. Loosen the lock nut on the Index Assembly bracket.
3. Unscrew the Index Assembly, and remove.

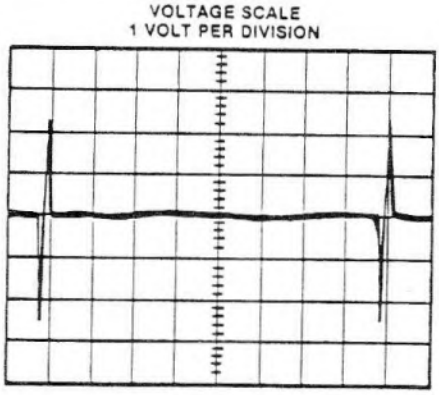
Replacement

To replace the Index Assembly, reverse Steps 1 through 3.

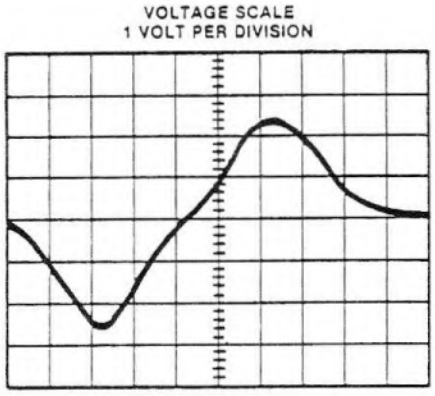
Adjustment

To adjust the Index Assembly:

1. Loosen the 3/8-inch locking nut.
2. Adjust the Index Assembly between 0.006 to 0.008 inches from the motor rotor.
3. Use a 100 megahertz or greater bandwidth oscilloscope.
4. Verify the A. C. signal as seen at U7, Pin 14, is greater than one volt peak to peak (see Figure 4-3).
5. There must not be more than 100 millivolts peak ripple on the base line.



TIME SCALE: 2 MILLISECONDS PER DIVISION
LOCATION U7-13



TIME SCALE: 50 MICROSECONDS PER DIVISION
LOCATION U7-13

FIGURE 4-3
INDEX SENSOR

FRONT PANEL

Removal

To remove the front panel

1. Pull front panel away from frame by lifting up one edge.
2. Remove the snap-on front panel from the drive frame.
3. Disconnect the L.E.D. assembly from the Logic Circuit Board.

Replacement

To replace the front panel, connect the L.E.D. to the Logic Circuit Board and snap on the panel over the drive frame.

FRAME ASSEMBLY

Removal

To remove the Frame Assembly:

1. Remove the Logic Circuit Board.
2. Remove the three frame nuts and the six washers.
3. Remove the Frame Assembly.

Replacement

To replace the Frame Assembly, reverse Steps 1 through 3.

TRACK 0 SENSOR ASSEMBLY

CAUTION

Do not move the positioning mechanism or Track 0 stop.

Removal

To remove the Track 0 Sensor Assembly:

1. Remove the Logic Circuit Board.
2. Loosen the screws on the Track 0 Sensor Assembly mount.
3. Swing the mount clear, and remove the screw that holds the Track 0 Sensor Assembly.

Replacement

To replace the Track 0 Sensor Assembly, reverse Steps 1 through 3.

Adjustment

To adjust the Track 0 Sensor Assembly:

1. Loosen the screws.
2. Adjust the sensor so that it is 2.5 $\pm$ 1 volt at U3, Pin 3, while stepping out from Track 5 to Track 0, and the positioner is on Track 2 plus or minus one track.
3. Verify that U3, Pin 2, changes logic level at Track 2, plus or minus one track (see Figure 4-4).

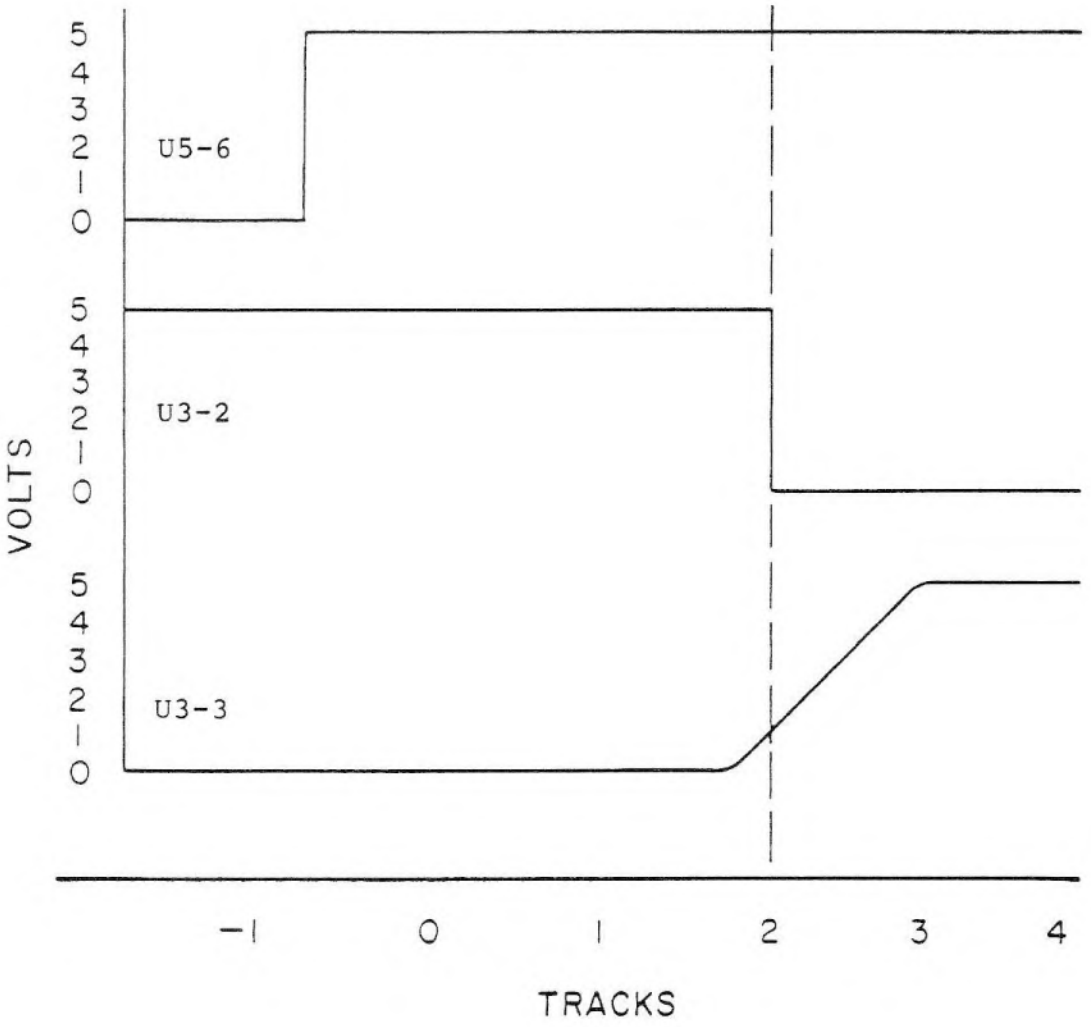
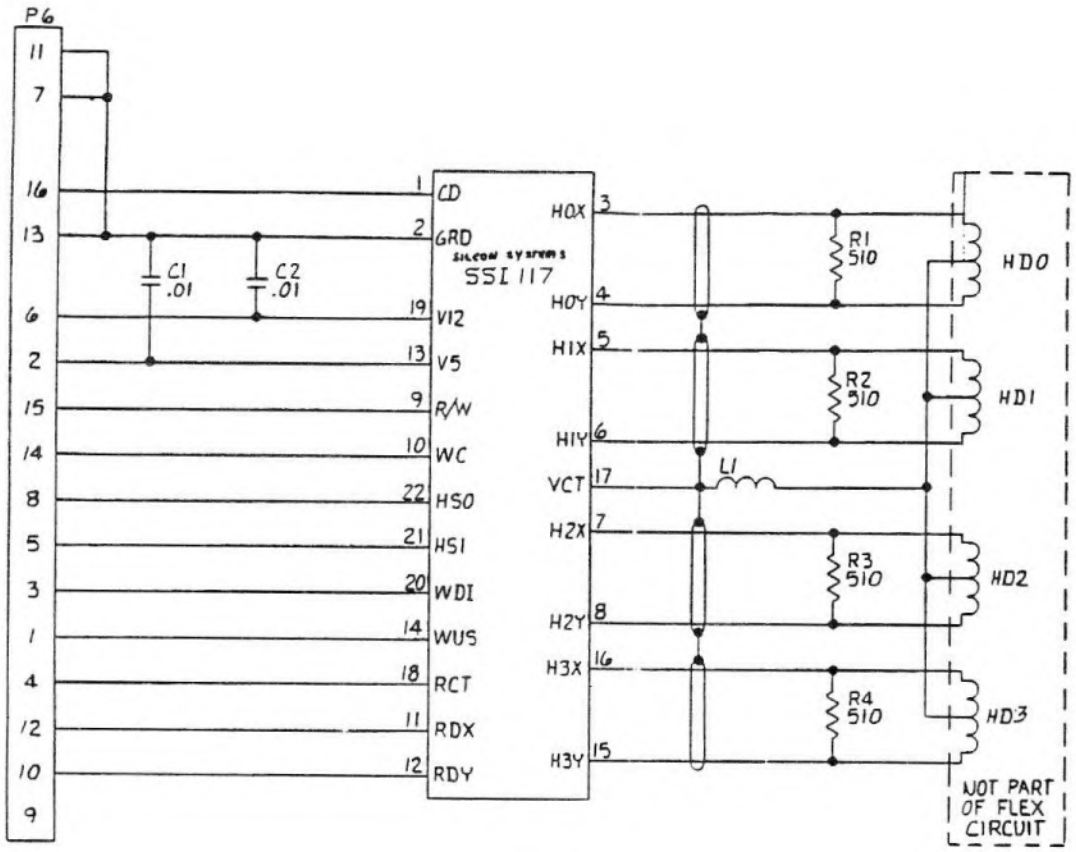


FIGURE 4-4
TRACK 0 ADJUSTMENT

RECOMMENDED SPARE PARTS - TM252

TRACK 0 ASSEMBLY	-	210939-001
INDEX SENSOR	-	187010-003
LOGIC BOARD	-	187490-001
BEZEL ASSEMBLY (including L.E.D.)	-	187574-001
LED ASSEMBLY	-	187571-001



WUS - UN-SAFE WRITE
WDI - WRITE DATA IN
WC - WRITE CURRENT
HS0 - HEAD SELECT 0
HS1 - HEAD SELECT 1
RCT - REDUCE CURRENT
R/W - READ/WRITE
RDX - READ DATA "X"
RDY - READ DATA "Y"
V5 - VOLTAGE +5 VDC
V12 - VOLTAGE +12 VDC
CD - CARRIER DETECT
VCT - VOLTAGE CENTER TAP

Tandon
CORPORATE OFFICES
20320 PRAIRIE STREET
CHATSWORTH, CA 91311

TEL. NO.: (818) 993-6644
TELEX NO.: 194794
TWX NO.: 910-494-1721

P/N 179050-001B (T5008B 11-84)

MAILING ADDRESS: P.O. BOX 2107, CHATSWORTH, CA 91311

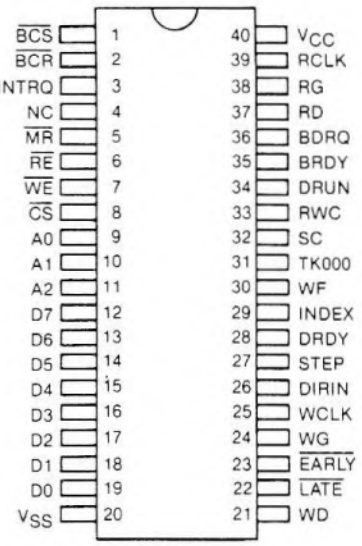
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FINAL

WD1010-05 Winchester Disk Controllers

FEATURES

- ST506/SA1000 COMPATIBLE
- MULTIPLE SECTOR READ/WRITE
- UP TO 5MBITS/SEC DATA RATE
- UNLIMITED SECTOR INTERLEAVE
- AUTOMATIC FORMATTING
- CRC/ECC CAPABILITY WITH EXTERNAL ECC GENERATOR/CHECKER
- PROGRAMMABLE RETRIES
- VARIABLE SECTOR SIZE
- SINGLE +5V SUPPLY



PIN DESIGNATION

DESCRIPTION

The WS1010-05 is a MOS/LSI device which performs the functions of a Winchester Disk Controller/Formatter. It is compatible with the Seagate ST506 and the Shugart Associates SA1000 drives, as well as all other 5¼" and 8" products utilizing the same type of interface. On the host side, an 8-bit bi-directional bus accepts all commands, data, and status bytes. The Western Digital WD1000 series of board level controllers are software compatible with the WD1010-05.

Operating from a single 5 volt supply, the WD1010-05 is implemented in NMOS silicon gate technology and is available in a 40 pin dual-in-line package.

ARCHITECTURE

The WD1010-05 Winchester Disk Controller provides the necessary link between an 8-bit, parallel processor and a Winchester disk drive. The WD1010-05 may be programmed to either automatically retry errors, or to terminate the command. The internal architecture of the WD1010-05 is shown in Figure 1. Its major functional blocks are:

PLA Controller

The PLA interprets commands and provides all control functions. It is synchronized with WCLK.

Magnitude Comparator

A 10 bit magnitude comparator is used for calculation of drive step, direction, present and desired cylinder position.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
1	$\overline{BCS}$	$\overline{BUFFER}$ $\overline{CHIP}$ $\overline{SELECT}$	Active low output used to enable reading or writing of the external sector buffer.
2	$\overline{BCR}$	$\overline{BUFFER}$ $\overline{COUNTER}$ $\overline{RESET}$	Active low output that is strobed by the WD1010-05 prior to read/write operations. This pin is strobed whenever $\overline{BCS}$ changes state.
3	INTRQ	INTERRUPT REQUEST	INTRQ is an output asserted upon completion of a command and de-asserted when the Status Register is read or a new command is written into the Command Register. This signal can be programmed to occur with BDRQ and DRQ during Read Command.
4	NC	NO CONNECT	
5	$\overline{MR}$	$\overline{MASTER}$ $\overline{RESET}$	A logic low in this input will initialize all internal logic.
6	$\overline{RE}$	$\overline{READ}$ $\overline{ENABLE}$	Tristate bi-directional line used as an input for reading the task register and an output when the WD1010-05 is reading the buffer.
7	$\overline{WE}$	$\overline{WRITE}$ $\overline{ENABLE}$	Tristate bi-directional line used as an input for writing into the task register and as an output when the WD1010-05 is writing to the buffer.
8	$\overline{CS}$	$\overline{CHIP}$ $\overline{SELECT}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
9 10 11	A0 A1 A2	ADDRESS 0- ADDRESS 2	These three inputs select the register to receive/transmit data on D0-D7.
12 thru 19	D7 thru D0	DATA 7 thru DATA 0	8-bit tri-state bi-directional bus used for transfer of commands, status, and data.
20	V_{SS}	GROUND	Ground
21	WD	WRITE DATA	This output contains the MFM clock and data pulses to be written on the disk.
22 23	$\overline{LATE}$ $\overline{EARLY}$	$\overline{LATE}$ $\overline{EARLY}$	Precompensation outputs used to delay the WD pulses externally.
24	WG	WRITE GATE	This output is set to a logic high before writing is to be performed on the disk.
25	WCLK	WRITE CLOCK	4.34 or 5.0 MHz clock input used to derive all internal write timing.
26	DIRIN	DIRECTION IN	This output determines the direction the stepping motor will move the heads. High = in, Low = out.
27	STEP	STEP PULSE	This output generates a pulse for stepping the drive motor.
28	DRDY	DRIVE READY	This input must be at a logic high in order for commands to execute.
29	INDEX	INDEX PULSE	A rising edge on this input informs the WD1010-05 when the index hole has been encountered.
30	WF	WRITE FAULT	An error input to the WD1010-05 which indicates a fault condition at the drive.
31	TK000	TRACK 000	An input to the WD1010-05 which indicates positioning over track 000.

PIN DESCRIPTION (Continued)

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
32	SC	SEEK COMPLETE	A rising edge on this input informs the WD1010-05 when head settling time has expired. In the Format Command it is used to extend the gap.
33	RWC	REDUCED WRITE CURRENT	This output can be programmed to reduce write current on a selected starting cylinder.
34	DRUN	DATA RUN	This input informs the WD1010-05 when a field of one's or zeroes have been detected.
35	BRDY	BUFFER READY	This rising edge is activated input is used to inform the controller that the sector buffer is full or empty.
36	BDRQ	BUFFER DATA REQUEST	BDRA and DRQ (Bit 3 Status Register) are asserted when the Buffer is to be read from or written to, by the Host. BDRQ can be used by a DMA controller or by the Host during Programmed I/O. DRQ must be polled by the Host if used during programmed I/O.
37	RD	READ DATA	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
38	RG	READ GATE	This output is set to a logic high when data is being inspected from the disk.
39	RCLK	READ CLOCK	A nominal square wave clock input derived from the external data recovery circuits.
40	V_{CC}	+5 VOLT	+5V

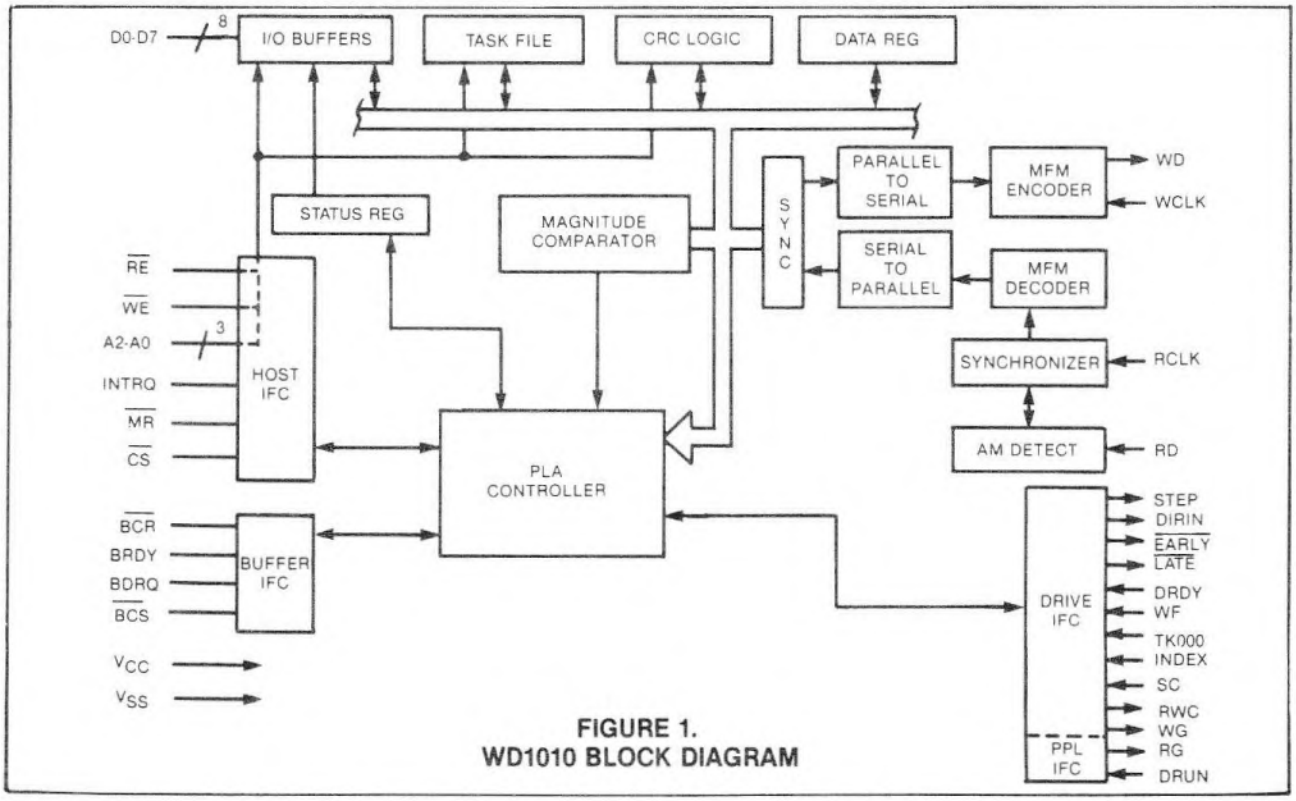


FIGURE 1.
WD1010 BLOCK DIAGRAM

CRC Logic
Generates and checks the cyclic redundancy check characters appended to the ID and data fields. The polynomial is X16 + X12 + X5 + 1.

MFM Encode/Decode
Encodes and decodes MFM data to be written/read from the drive. The MFM encoder operates from WCLK; a clock having a frequency equivalent to the bit rate. The MFM decode operates from RCLK; a bit rate clock generated from the external data separator. RCLK and WCLK need not be synchronized.

AM Detect
The address mark detector checks the incoming data stream for a unique missing clock pattern (Data = A1 hex, Clock = 0A hex) used in each ID and data field.

Host/Buffer IFC
This logic contains all of the necessary circuitry to communicate with the 8-bit host processor.

Drive IFC
This logic controls and monitors all lines from the drive, with the exception of read and write data.

DRIVE INTERFACE

The drive side of the WD1010-05 controller requires three sections of external logic. These are buffers/receivers, data separator, and write precompensation. Figure 2 illustrates a drive side interface.

The buffer/receivers condition the control lines to be driven down the cable to the drive. The control lines are typically single-ended, resistor terminated TTL levels. The data lines to and from the drive also require buffering, but are differential RS-422 levels. The interface specification to the drive can be found in the manufacturers' OEM manual. The WD1010-05 supplies TTL compatible signals, and will interface to most buffer/driver devices.

The data recovery circuits consist of a phase-lock loop data separator and associated components. The WD1010-05 interacts with the data separator through the DRUN and RG signals. The block diagram of the

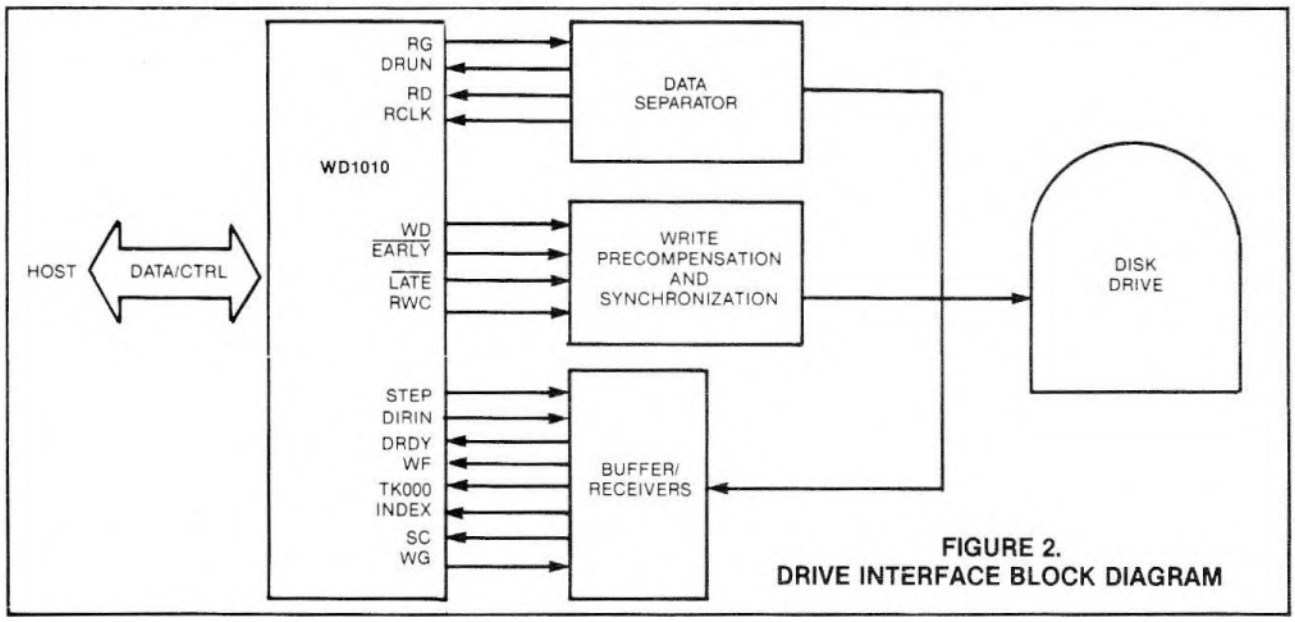


FIGURE 2.
DRIVE INTERFACE BLOCK DIAGRAM

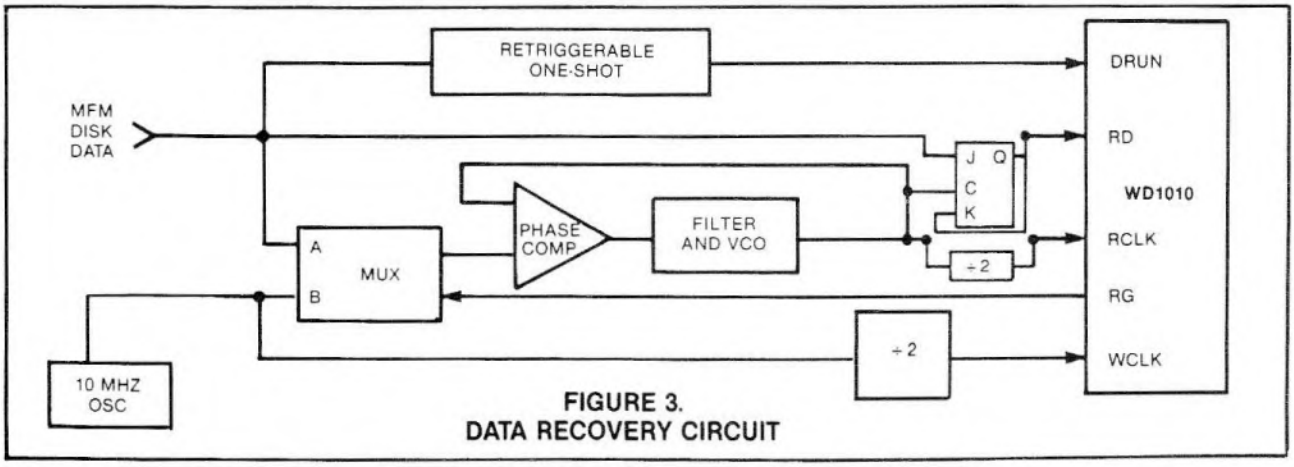


FIGURE 3.
DATA RECOVERY CIRCUIT

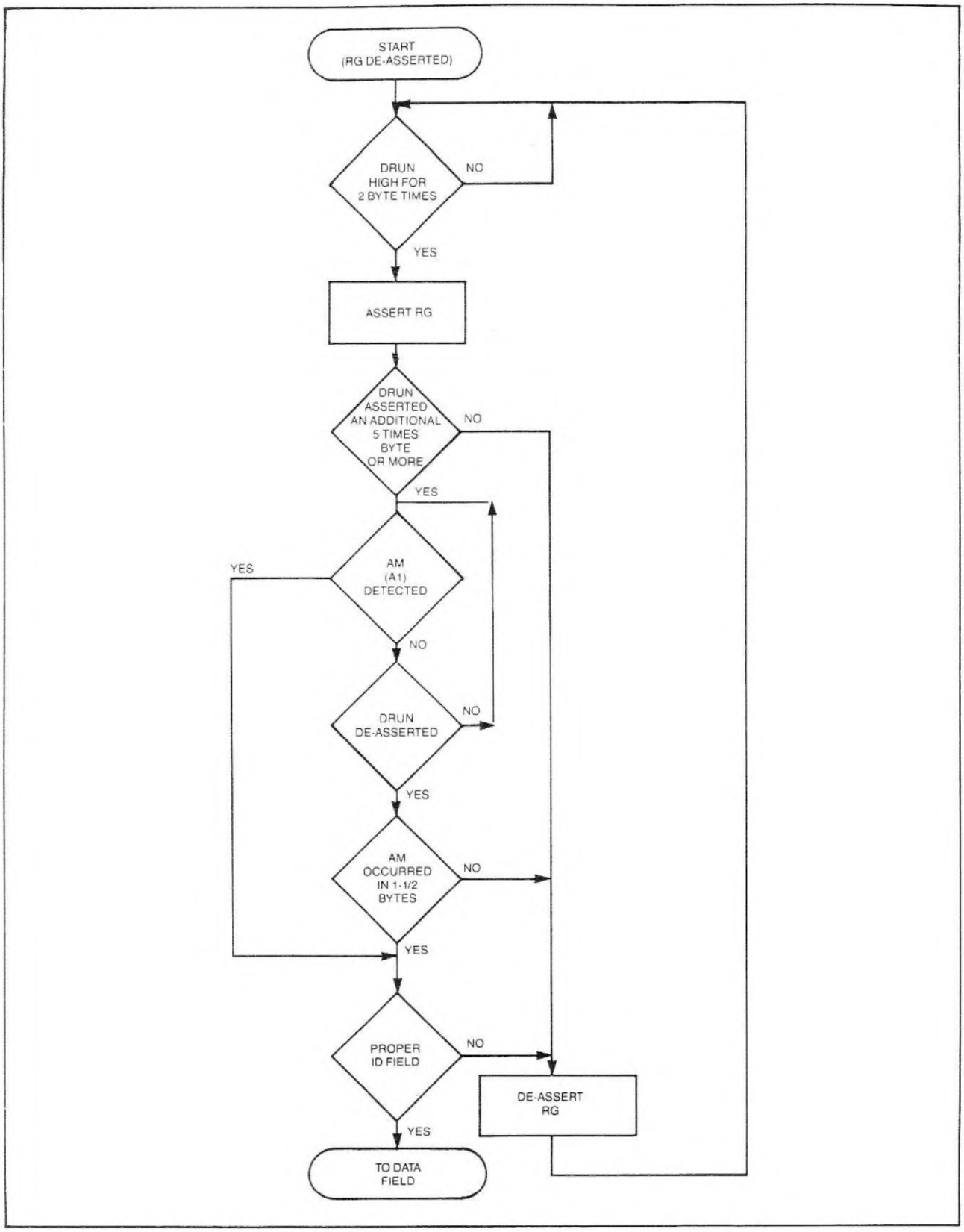


FIGURE 4. PLL CONTROL SEQUENCE FOR ID FIELD

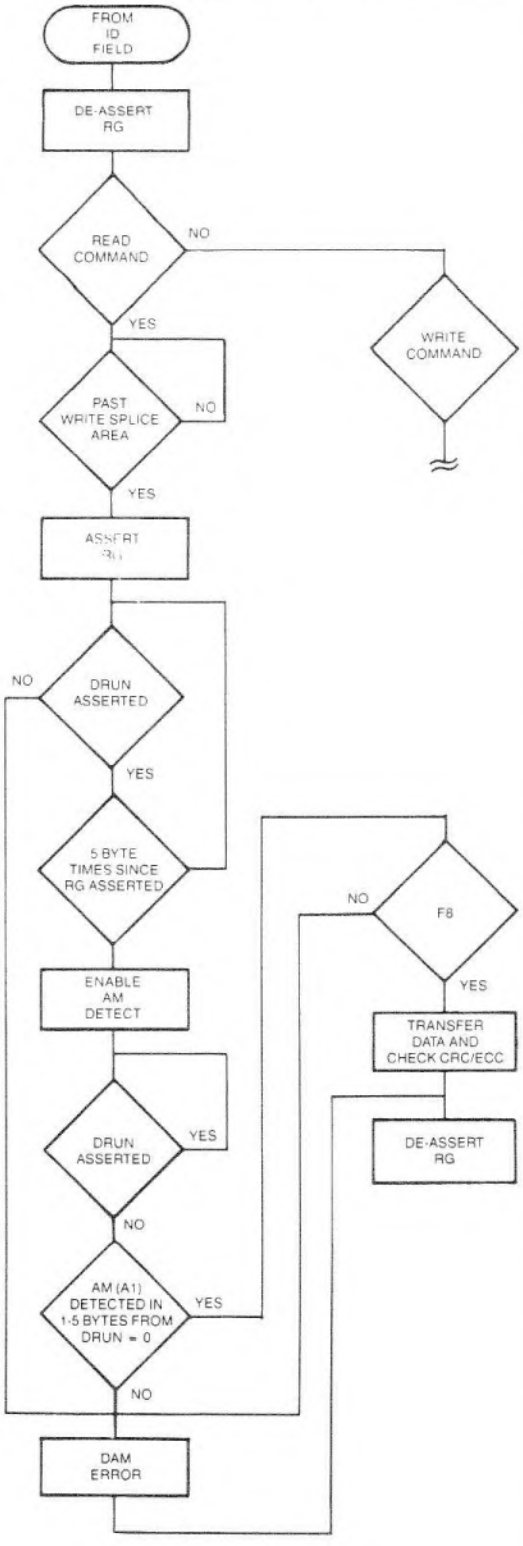


FIGURE 4. (CONT.)
PPL CONTROL SEQUENCE FOR DATA FIELD

data separator circuit is shown in Figure 3. Read data from the drive is presented to the RD input of the WD1010-05, the reference multiplexor, and a retriggerable one shot. The read gate output will be low when the WD1010-05 is not inspecting data. The PLL at this time should remain locked to the reference clock.

When any Read/Write command is initiated and a search for address marks begins, the DRUN input is examined. The DRUN one-shot is set for slightly greater than one bit time, allowing it to retrigger constantly on a field of ones and zeros. An internal counter times out to see that DRUN is high for 2 byte times. Read gate is set by the WD1010-05, switching the data separator to lock onto the incoming data stream. If DRUN falls prior to 7 bytes times RG is lowered and the process is repeated. Read gate will remain active high until a non-zero, non-address mark byte is detected. It then will lower read gate for 2 byte times (to allow the PLL to lock back on the reference clock) and start the DRUN search over again. If an address mark is detected, read gate will be held high and the command will continue searching for the proper ID field. This sequence is shown in the flow chart of Figure 4.

The write precompensation logic is controlled by the signals RWC, $\overline{\text{Early}}$ and $\overline{\text{Late}}$. The cylinder in which the RWC line becomes active is controlled by a register in the Task File. It can be used to turn on the precomp circuitry on a predetermined cylinder. If the write precomp register value is FF, then RWC will always be low.

The signals $\overline{\text{Early}}$ and $\overline{\text{Late}}$ are used to tell the precomp how much delay is required on the write data pulse about to be sent. The amount of delay is determined externally through a digital delay line or equivalent circuitry. Since the signal $\overline{\text{Early}}$ occurs after the fact, write data should be delayed one interval when both $\overline{\text{Early}}$ and $\overline{\text{Late}}$ are deasserted; two intervals when $\overline{\text{Late}}$ is asserted; and no delay when $\overline{\text{Early}}$ is asserted. An interval, for example, is 12-15 ns. on the ST506. $\overline{\text{Early}}$ or $\overline{\text{Late}}$ will be active slightly ahead of the write data pulse; $\overline{\text{Early}}$ and $\overline{\text{Late}}$ will never be asserted at the same time. The $\overline{\text{Early}}$ $\overline{\text{Late}}$ signals function independently of the content of the RWC register.

Examples for all three of the above circuits can be found in the WD1010 Application Note.

HOST INTERFACE

The primary interface between the host processor and the WD1010-05 is through an 8-bit bidirectional bus. This bus is used to transmit/receive data to both the WD1010-05 and a sector buffer. The sector buffer is constructed with either FIFO memory or static RAM and a counter. Since the WD1010-05 will make the bus active when accessing the sector buffer, a transceiver must be used to isolate the host during this time. Figure 5 shows a typical connection to a sector buffer implemented with RAM memory. Whenever the WD1010-05 is not using the sector buffer, the $\overline{\text{BCS}}$ is deasserted. This allows the host to access the WD1010's Task File, and to set up parameters prior to issuing a command. It also allows the host to access the RAM buffer. A

decoder is used to generate a chip select when A_0-A_2 are '000'; an unused address in the WD1010-05. A binary counter is enabled whenever $\overline{RE}$ or $\overline{WE}$ goes active and incremented on the trailing edge of the chip select. This allows the host to access sequential bytes within the RAM. The decoder also generates another chip select when A_0-$A_2 \neq$ '000'; allowing access to the WD1010-05's internal registers while keeping the RAM tri-stated.

During write sector commands, the processor sets up data in the Task File and issues the command. The WD1010 then generates a status to inform the host it may load the buffer with the data to be written. When the counter reaches its maximum count, the BRDY signal is made active (by the "carry" out of the counter), informing the WD1010-05 that the buffer is full. (BRDY is a rising edge activated signal). The $\overline{BCS}$ is then asserted, disconnecting the host through the transceivers, and the $\overline{RE}$ and $\overline{WE}$ lines become outputs from the WD1010-05 to allow it access to the buffer. When the WD1010-05 is done using the buffer, it disables $\overline{BCS}$ which again allows host access to this local bus. The read sector commands operate in a similar manner, except the buffer is loaded by the WD1010-05 instead of the host.

Another control signal called BDRQ can be connected to a DMA controller in the Host, or can be polled by the Host for programmed I/O. For further explanation, refer to the description of the individual commands and the A.C. Timing Specifications. In a read command; an interrupt may be specified to occur either at the end of the command or when BDRQ is activated. The INTRQ is cleared either by reading the status register or by writing a new command in the command register.

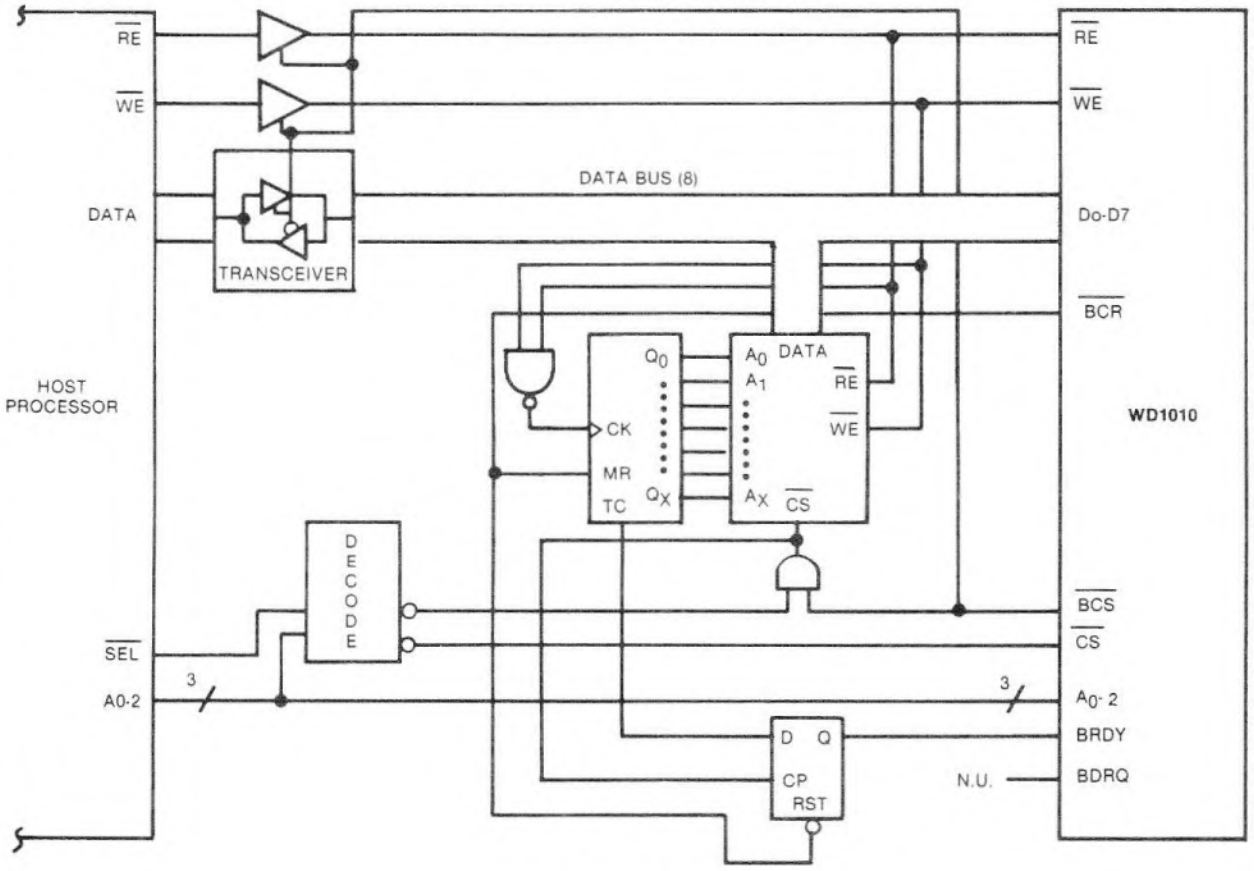


FIGURE 5.
HOST INTERFACE

TASK FILE

The Task File is a bank of nine registers used to hold parameter information pertaining to each command. These registers and their addresses are:

A_2	A_1	A_0	READ	WRITE
0	0	0	(Bus Tri-Stated)	(Bus Tri-Stated)
0	0	1	Error Flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Low	Cylinder Low
1	0	1	Cylinder High	Cylinder High
1	1	0	SDH	SDH
1	1	1	Status Register	Command Register

NOTE: Registers are **not** cleared by master reset ($\overline{MR}$).

ERROR REGISTER

This read-only register contains specific error status after the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	0
BB	CRC	—	ID	—	AC	TK	DM

Bit 7 — Bad Block Detect
This bit is set when an ID field has been encountered that contains a bad block mark. Used for bad sector mapping.

Bit 6 — CRC Data Field
This bit is set when a CRC error occurs in the data field. With Retry enabled, ten more attempts are made to read the sector correctly. If none of these attempts are successful, the Error Status is set also (bit 0 in the Status Register). If one of the attempts is successful, this bit remains set to inform the Host that a marginal condition exists. However, the Error Status bit is not set. Even if errors exist, the data can be read.

Bit 5 — Reserved
Not used; forced to a zero.

Bit 4 — ID Not Found
This bit is set to indicate that the correct cylinder, head, sector number or sector size parameter could not be found, or that a CRC error occurred on the ID field. This bit is set on the first failure and remains set even if the error is recovered on a Retry. When recovery is unsuccessful, the Error Status bit is set also (bit 0 in the Status Register).

Bit 3 — Reserved
Not used; forced to a zero.

Bit 2 — Aborted Command
This bit is set if a command was issued while the DRDY is de-asserted or the WF is asserted. The aborted command bit will also be set if an undefined command code is written into the command register, but an implied seek will be executed.

Bit 1 — Track Zero Error
This bit is set only by the restore command. It indicates that the TK000 has not gone active after the issuance of 1024 stepping pulses.

Bit 0 — Data Address Mark Not Found
This bit is set during a read sector command if the data address mark is not found after the proper sector ID is read.

WRITE PRECOMP CYLINDER

This register is used to define the cylinder number where the RWC is to be asserted:

7	6	5	4	3	2	1	0
CYLINDER NUMBER ÷ 4							

The value 00-FF loaded into this register is internally multiplied by 4 to specify the actual cylinder where RWC is asserted. Thus, a value of 01 hex will cause RWC to activate on cylinder 4; 02 hex on cylinder 8, and so on. Switching points are then 0, 4, 8, . . . The RWC will be asserted when the present cylinder is equal to 4 times or more than the value in this register. For example, the ST506 requires precomp on cylinder 128 (80 hex) and above. Therefore, the write precomp cylinder register should be loaded with 32 (20 hex).

A value of FF hex will always cause RWC to be low, no matter what the cylinder number values are.

SECTOR COUNT

This register holds the number of sectors that are to be transferred to the buffer.

7	6	5	4	3	2	1	0
# OF SECTORS							

This register is used during a multiple sector R/W command. The written value is decremented after each sector is transferred to the sector buffer. A zero represents a 256 sector transfer, a 1 = one sector transfer, etc. This register is a "don't care" when single sector commands are specified.

SECTOR NUMBER

This register holds the sector number of a desired sector:

7	6	5	4	3	2	1	0
SECTOR NUMBER							

During a multiple sector command, this register specifies the first sector in the transfer. It is internally incremented after each transfer of data to the sector buffer. The sector number register may contain any value from 0 to 255.

CYLINDER NUMBER LOW

This register holds the least significant 8-bits of the desired cylinder number.

7	6	5	4	3	2	1	0
LS BYTE OF CYLINDER NUMBER							

It is used in conjunction with the cylinder number high register to specify a range of 0 to 1023.

CYLINDER NUMBER HIGH

This register defines the two most significant bits of the cylinder number desired:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	(9)	(8)

Internal to the WD1010-05, is another pair of registers that hold the actual position number where the R/W heads are located. The cylinder number high and low registers can be considered the cylinder destination for seeks and other commands. After these commands are executed, the internal cylinder position registers' contents are equal to the cylinder high/low registers. If a drive number change is detected on a new command, the WD1010-05 automatically reads an ID field to update its internal cylinder position registers. This affects all commands except a Restore.

SDH BYTE

This register contains the desired sector size, drive number, and head number parameters. The format is:

7	6	5	4	3	2	1	0
EXT	SIZE		DRIVE		HEAD		

6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL 1
0	1	DSEL 2
1	0	DSEL 3
1	1	DSEL 4

2	1	0	HEAD #
0	0	0	HSEL 0
0	0	1	HSEL 1
0	1	0	HSEL 2
0	1	1	HSEL 3
1	0	0	HSEL 4
1	0	1	HSEL 5
1	1	0	HSEL 6
1	1	1	HSEL 7

Both head number and sector size is compared against the disks' ID field. Head select and drive select lines are not available as outputs from the WD1010-05, and must be generated externally. Figure 6 shows the logic to implement these select lines.

Bit 7, the extension bit, is used to extend the data field by seven bytes when using ECC codes. CRC is not appended to the end of the data field when EXT = 1; the data field becomes "sector size + 7" bytes long. CRC is checked on the ID field regardless of the state of the extension bit. Note that the sector size bits are written to the ID during a format command. The SDH byte written into the ID field is different that the SDH register contents. The recorded SDH byte does not have the drive number written but does have bad block mark written. The format is:

BAD BLOCK	SIZE		0	0	HEAD #		
7	6	5	4	3	2	1	0

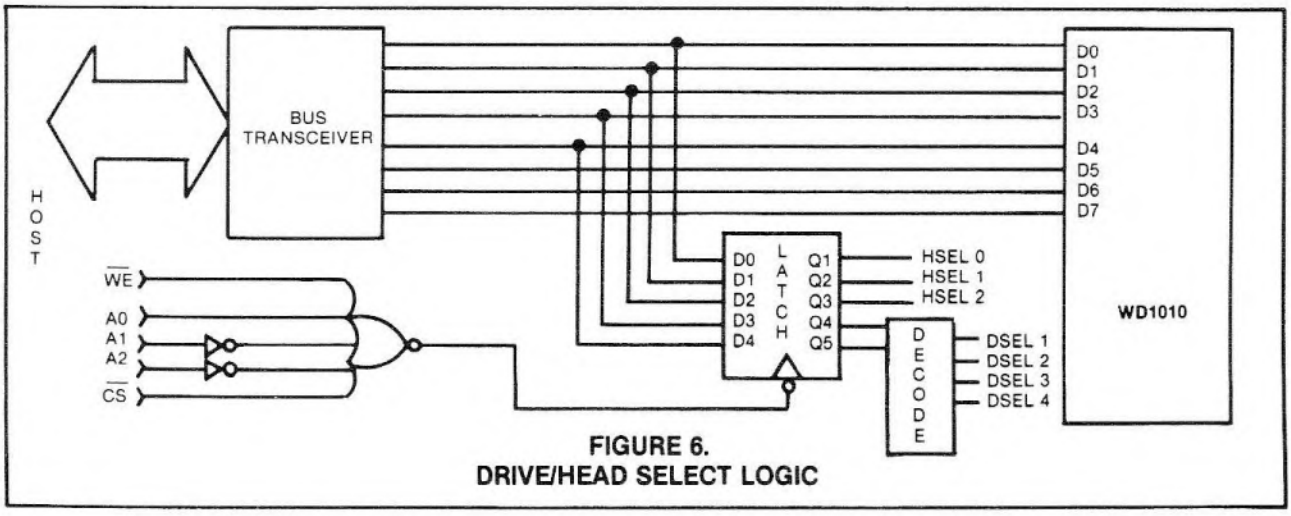


FIGURE 6.
DRIVE/HEAD SELECT LOGIC

STATUS REGISTER

The status register is a read-only register which informs the host of certain events performed by the WD1010 as well as reporting status from the drive control lines. The term INTRQ, if set, will be cleared when the status register is read. The format is:

7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	—	CIP	ERR

Bit 7— Busy
This bit is set whenever the WD1010-05 is accessing the disk. Commands should not be loaded into the command register while busy is set. Busy is made active when a command is written into the WD1010-05 and is deactivated at the end of all commands except the read sector. While executing a read sector command, busy is deactivated after the sector buffer has been filled. When the BUSY bit is set, no other bits in either the status or other registers are valid.

Bit 6 — Ready
This bit reflects the state of DRDY.

Bit 5 — Write Fault
This bit reflects the state of the WF. Whenever the WF bit goes high, an interrupt will be generated.

Bit 4 — Seek Complete
This bit reflects the state of the SC. When a seek has been initiated by a command, it will pause until the seek is completed.

Bit 3 — Data Request
This bit reflects the state of the BDRQ. It is set when the sector buffer should be loaded with data or read by the host, depending upon the command. DRQ/BDRQ remains high until BRDY is sensed, indicating the operation is completed. The BRDQ signal can be used in DMA interfacing or Programmed I/O, while the DRQ bit can be used only for programmed I/O transfers.

Bit 2 — Reserved
Not used. This bit is always forced to a zero.

Bit 1 — Command in Progress
When this bit is set, a command is being executed and a new command should not be loaded until reset. Although a command may be executing, the sector buffer is still available for access by the host. When the WD1010 is not busy (bit 7 = 0) the status register may be read. If other registers are read while CIP, the status register contents are returned.

Bit 0 — Error
This bit indicates that a non-recoverable error has occurred. When the Host reads the status and finds this bit set, it must then read the Error Register to determine the type of error. This bit is reset when a new command is written into the command register.

COMMAND REGISTER

This write-only register is loaded with desired command:

7	6	5	4	3	2	1	0
		C	O	M	M	A	N	D			

The commands begins to execute immediately upon loading. This register should not be loaded while the Busy or CIP bits are set in the status register. The INTRQ, if set, will be cleared by a write to the command register.

INSTRUCTION SET

The WD1010 will execute six commands. Prior to loading the command register, the host must first set up the task file with the proper information needed for the command. Except for the command byte, the other registers may be loaded in any order. Any subsequent writes to the command register will be ignored until execution is completed indicated by the resetting of the CIP bit in the status register.

COMMAND SUMMARY

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R_3	R_2	R_1	R_0
SEEK	0	1	1	1	R_3	R_2	R_1	R_0
READ SECTOR	0	0	1	0	I	M	0	T
WRITE SECTOR	0	0	1	1	0	M	0	T
SCAN ID	0	1	0	0	0	0	0	T
WRITE FORMAT	0	1	0	1	0	0	0	0

R_3-R_0 Rate Field

For 5 MHz WCLK:
R_3-R_0 = 0000 — ≈35 μs.
0001 — .5 ms.
0010 — 1.0 ms.
0011 — 1.5 ms.
0100 — 2.0 ms.
0101 — 2.5 ms.
0110 — 3.0 ms.
0111 — 3.5 ms.
1000 — 4.0 ms.
1001 — 4.5 ms.
1010 — 5.0 ms.
1011 — 5.5 ms.
1100 — 6.0 ms.
1101 — 6.5 ms.
1110 — 7.0 ms.
1111 — 7.5 ms.

Bit 0, ("T") Read Sector, Write Sector Commands

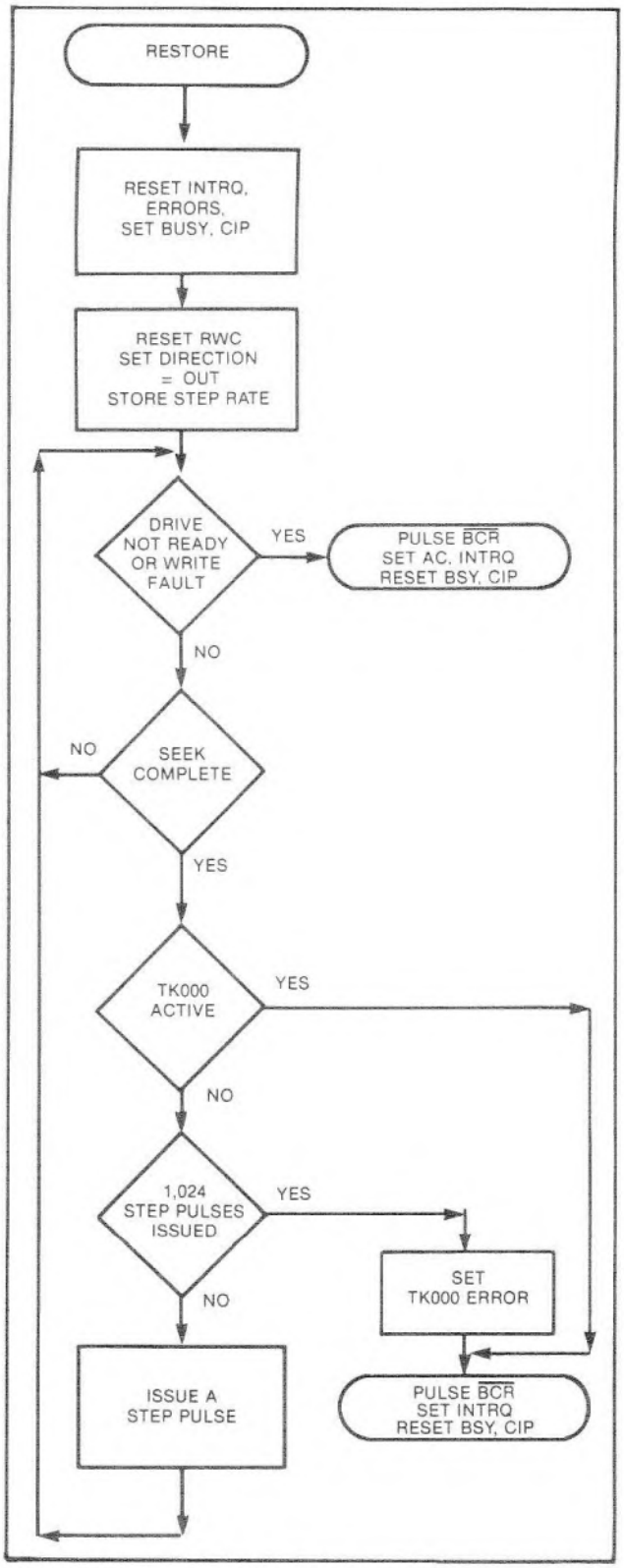
T = 0 Enable retries
T = 1 Disable retries

M = Multiple Sector Flag

M = 0 Transfer 1 sector
M = 1 Transfer multiple sectors

I = Interrupt Enable

I = 0, Interrupt at BDRQ time
I = 1, Interrupt at end of command



RESTORE COMMAND

The restore command is usually used on a power-up condition. The actual stepping rate used for the restore is determined by Seek Complete time. A step pulse is issued and the WD1010-05 waits for a rising edge on the seek complete line before issuing the next pulse. If 10 index pulses are received without a rising edge of seek complete, the WD1010 will switch to sensing the level of the SC line. If after 1,024 stepping pulses, the TK000 lines does not go active, the WD1010-05 will set the Track Zero error bit in the error register and terminate with an INTRQ. An interrupt will also occur if the write fault goes active or the DRDY goes inactive during execution.

The rate field specified (R_3-R_0) is stored in an internal register for future use in commands with implied seeks.

SEEK COMMAND

Since except for the SCAN ID all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The actual step rate used is taken from the rate field, which is also stored in an internal register for future use. If DRDY goes inactive or WF goes active, the command is terminated and an INTRQ is generated.

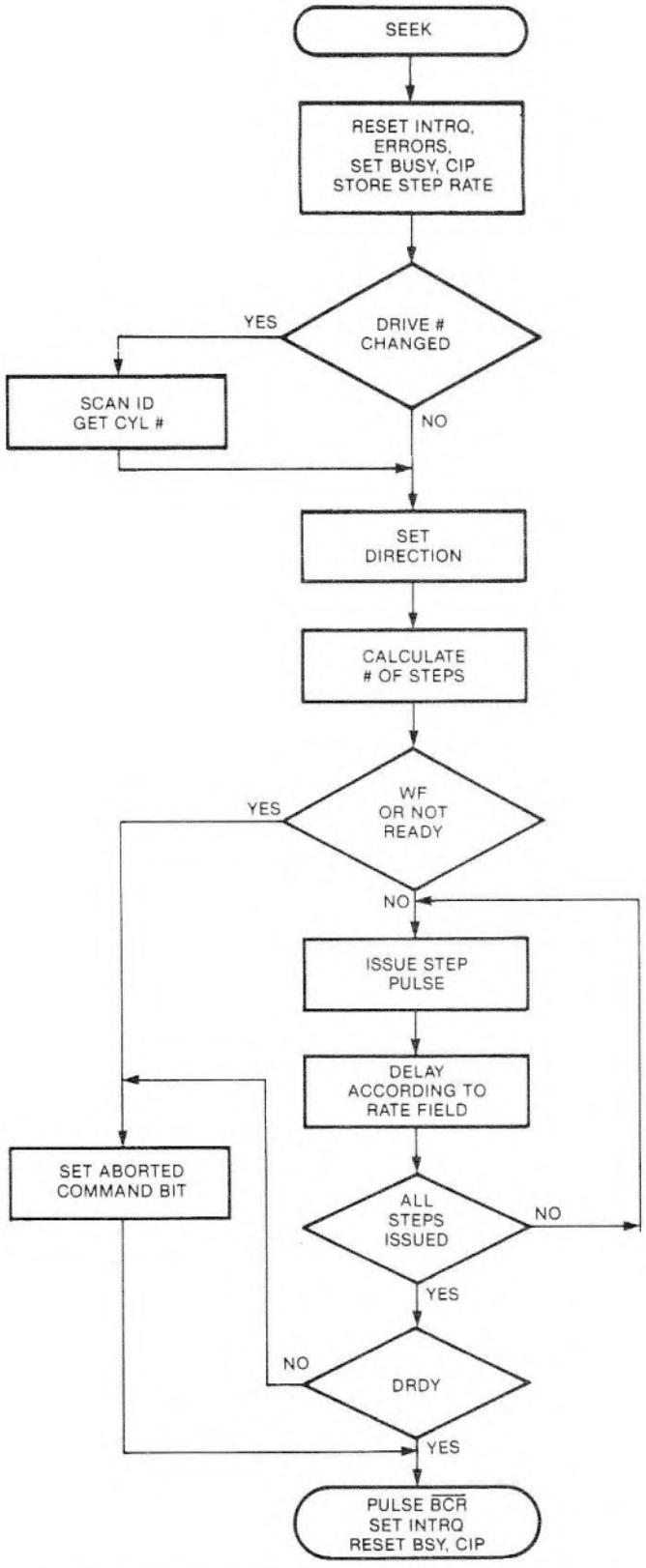
The direction and number of step pulses needed are calculated by comparing the contents of the cylinder register high/low to the cylinder position number stored internally. After all steps have been issued, the internal cylinder position register is updated and the command is terminated. Seek complete is not checked at the beginning or end of the command.

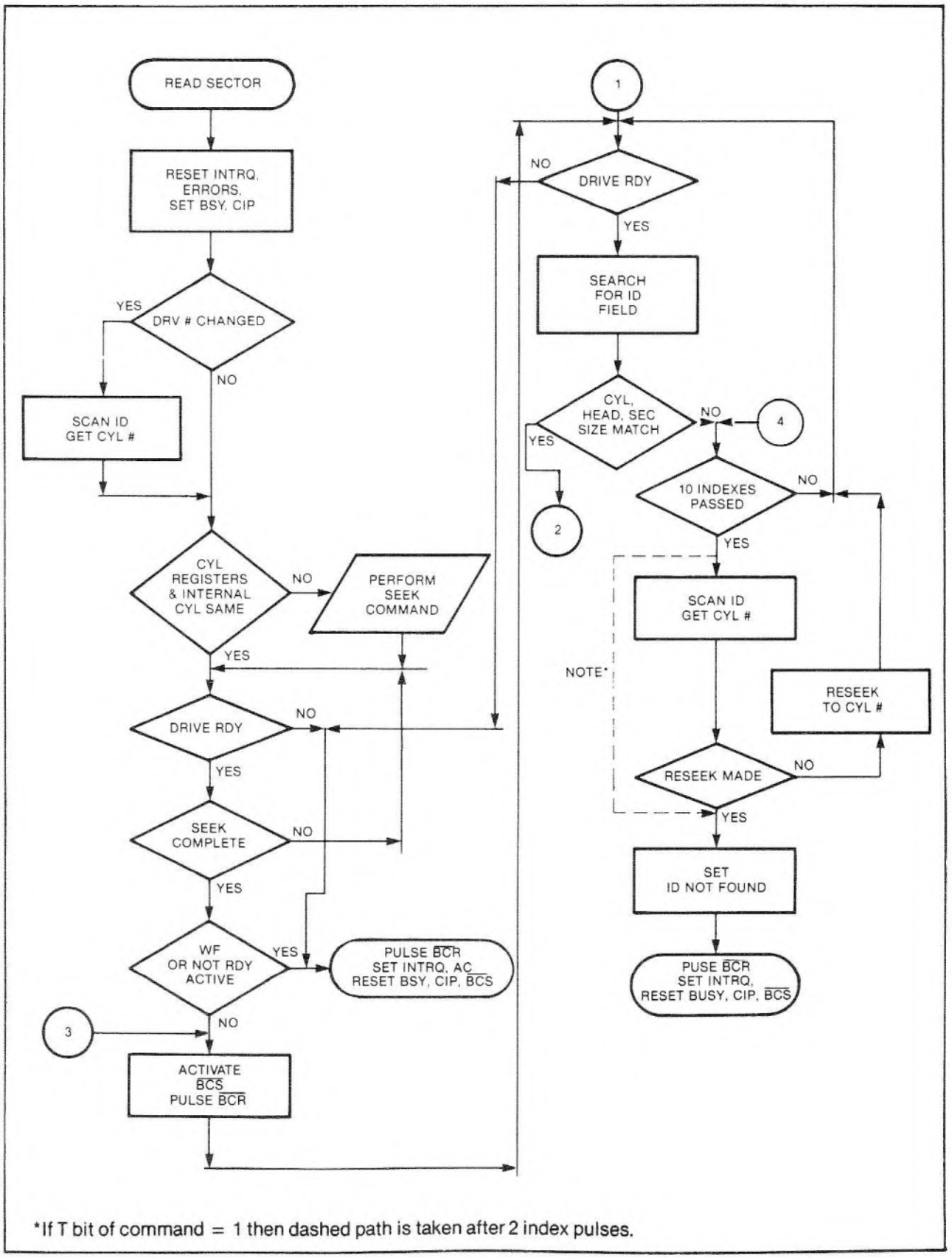
If an implied seek was performed, the WD1010-05 will wait until a rising edge of SC is received. If 10 revolutions occur before the rising edge of SC, the WD1010 will switch to level sensing of SC.

READ SECTOR

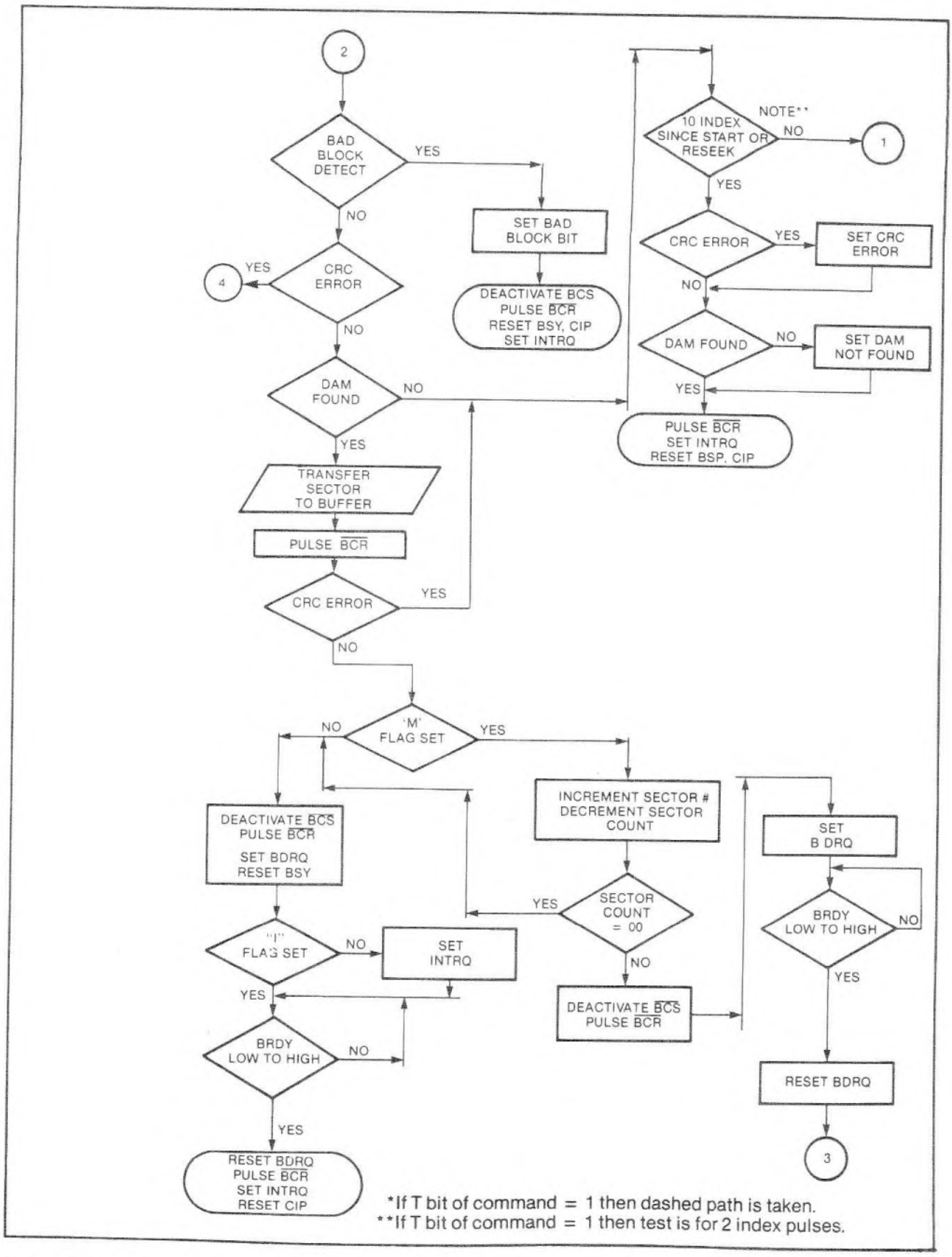
The read sector command is used to transfer one or more sectors of data from the disk to the sector buffer. Upon receipt of this command, the WD1010-05 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps calculation is performed and seek takes place. If an implied seek was performed, the WD1010-05 will search until a rising edge of seek complete is received. Write Fault and DRDY lines are checked throughout the command.

After seek complete is found to be true (with or without an implied seek), the search for an ID field occurs. The WD1010-05 must find an ID with the correct cylinder, head, sector size, and CRC within 10 revolutions if T bit of command is zero, and within 2 revolutions if T = 1; else the appropriate error bits will be set and the command terminated if T = 1. Both the Read and Write sector commands feature a "simulated completion" to ease programming. DRQ/BDRQ will be generated upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command. If T = 0, an automatic scan ID is performed to obtain cylinder position information and then, if necessary, a seek is performed. The search for the correct ID field is continued for 10 more disk rotations.

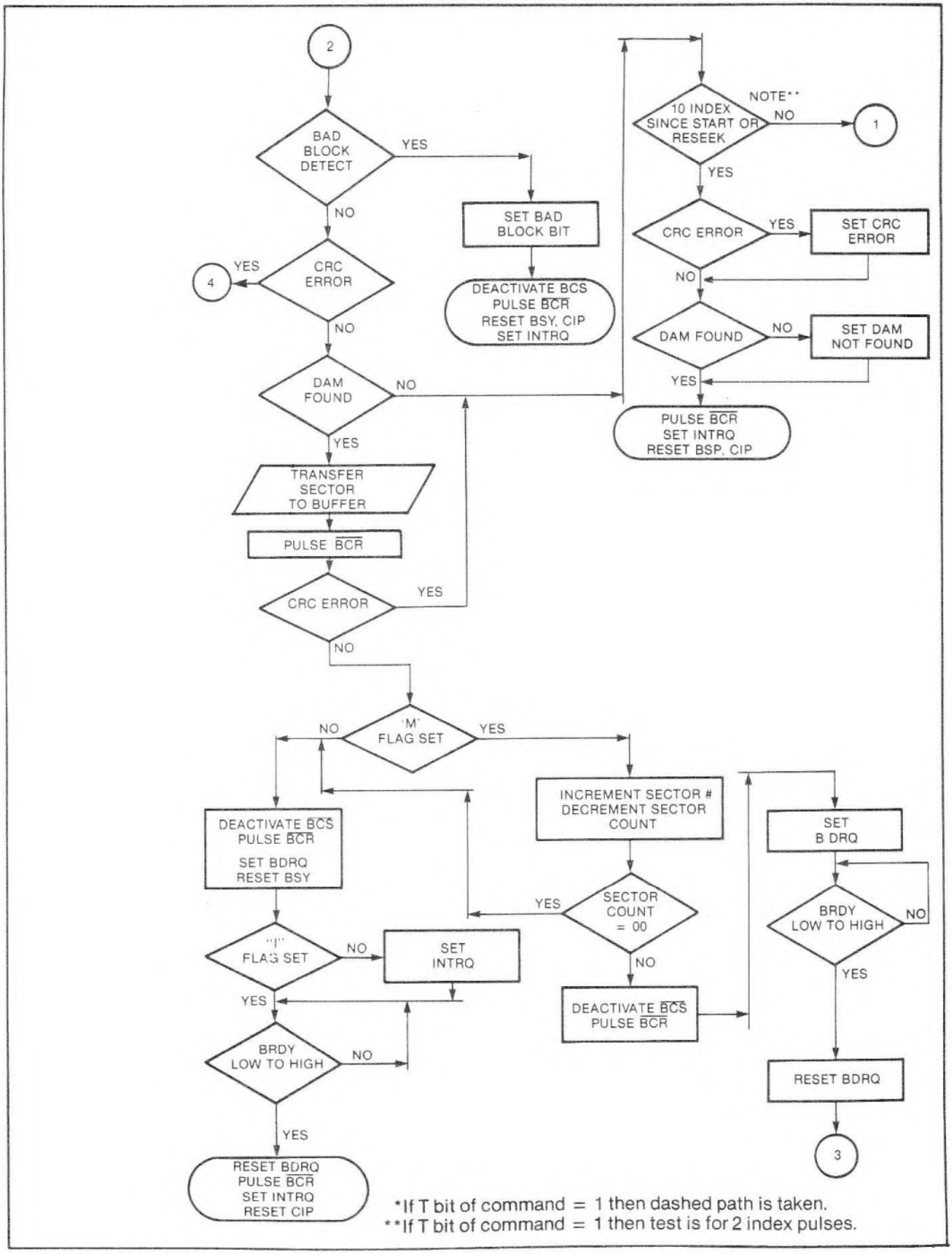

SEEK
RESET INTRQ, ERRORS, SET BUSY, CIP STORE STEP RATE
DRIVE # CHANGED
YES
NO
SCAN ID GET CYL #
SET DIRECTION
CALCULATE # OF STEPS
WF OR NOT READY
YES
NO
ISSUE STEP PULSE
DELAY ACCORDING TO RATE FIELD
SET ABORTED COMMAND BIT
ALL STEPS ISSUED
NO
YES
DRDY
NO
YES
PULSE BCR SET INTRQ RESET BSY, CIP



*If T bit of command = 1 then dashed path is taken after 2 index pulses.



*If T bit of command = 1 then dashed path is taken.
**If T bit of command = 1 then test is for 2 index pulses.



*If T bit of command = 1 then dashed path is taken.
**If T bit of command = 1 then test is for 2 index pulses.

When the data address mark is found, the WD1010-05 is ready to transfer data to the buffer. After the sector data has been transferred, the I flag is checked. If the I flag is 0, the INTRQ is made active coincident with BDRQ, indicating a transfer of data is required by the host. If I = 1, the INTRQ will occur at the end of the command (i.e., after the buffer is unloaded by the host).

An optional M flag may be set for multiple sector transfers. When M = 0, one sector is transferred and the sector count register is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD1010-05 decrements the sector count register and increments the sector number register. The next logical sector will be transferred, regardless of the interleave. Sectors are numbered at format time by a byte in the ID field.

For the WD1010 to make multiple sector transfers to the buffer, the BRDY line must be toggled low to high for each sector. The sector transfers will continue until the sector count register equals zero. If the sector count register is non-zero (indicating more sectors are to be transferred but the buffer is full), BDRQ will be made active and the host must unload the buffer. Once this occurs, the buffer will again be free to accept the next sector in this multiple sector read command.

When M = 0 (Single Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(5)	1010:	Sets BDRQ = 1; sets DRQ flag.
(6)	1010:	If I bit = 1 then (9).
(7)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$).
(8)	1010:	Waits for BRDY then sets INTRQ = 1; End.
(9)	1010:	Sets INTRQ = 1.
(10)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$); End.

When M = 1 (Multiple Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes $\overline{BCR}$; set $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Decrements sector count register; increments sector number register.
(5)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(6)	1010:	Sets BDRQ = 1; DRQ flag = 1.
(7)	Host:	Reads out content of buffer (by $\overline{RE}$ strobes).
(8)	Buffer:	Indicates data has been transferred by asserting BRDY.
(9)	1010:	When BRDY is asserted, go to (11) if sector count = 0.
(10)	1010:	Go to Step (2).
(11)	1010:	Activates INTRQ.

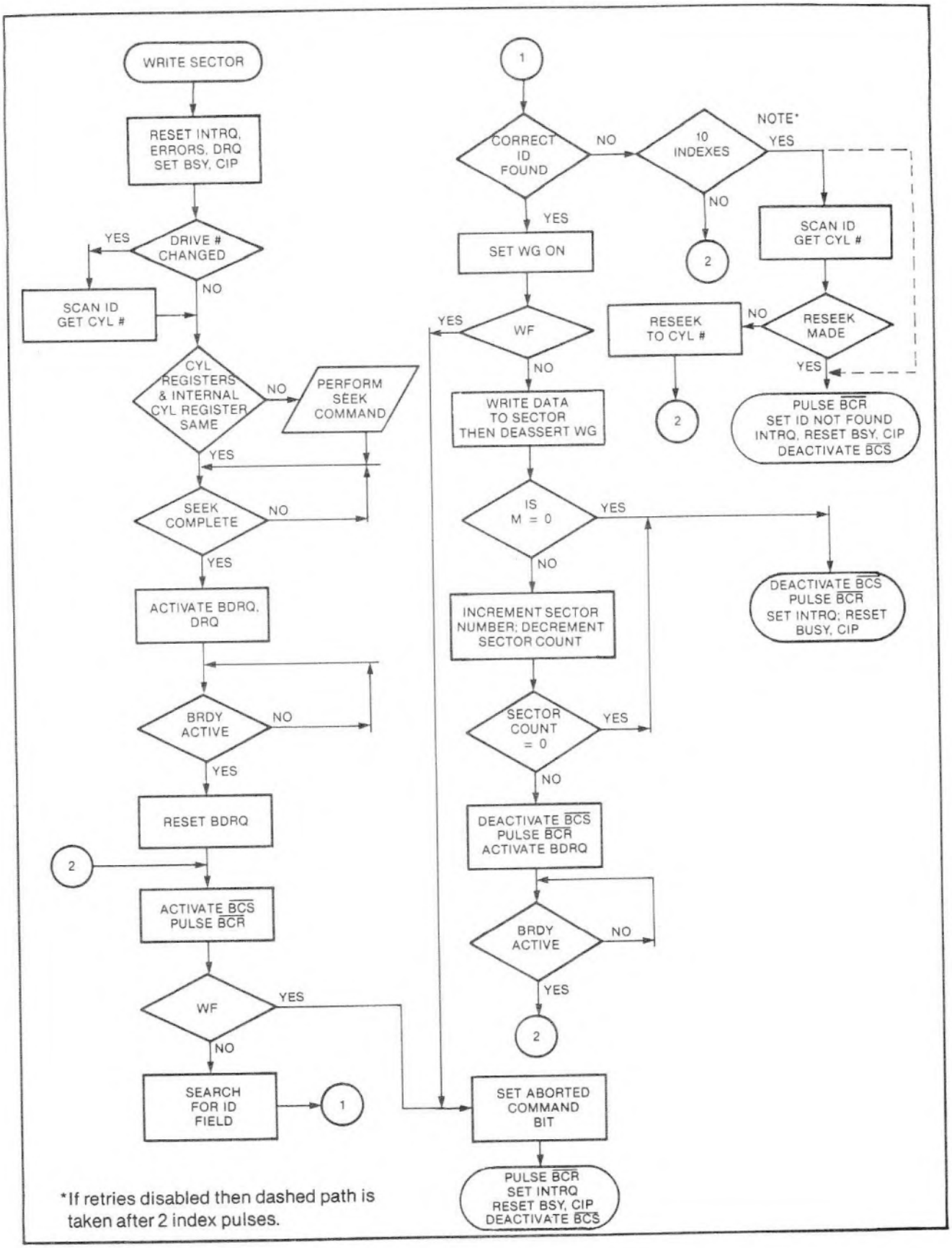
WRITE SECTOR

The write sector command is used to write one or more sectors of data to the disk. Upon receipt of this command, the WD1010-05 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps are calculated and a seek command takes place. Write fault and DRDY lines are checked throughout the command.

After Seek complete is found to be true (with or without an implied seek), the BDRQ signal is made active and the host proceeds to load the buffer. When the WD1010-05 senses the BRDY line going high, the ID field with the specified cylinder, head, and sector size is searched for. Once found, the write gate signal is raised and the data is written to the disk. It is necessary to resynchronize the write data due to the fact that a bit cell can extend from 295ns to 315ns during a write cycle. If retries are disabled and if the ID field cannot be found within 2 revolutions, the ID not found bit is set and the command is terminated.

If retries are enabled, and the ID field cannot be found within 10 revolutions, an automatic scan ID and seek commands are performed. The ID Not Found error bit is set if the ID field is not found after 10 more revolutions.

During a multiple sector write operation (M flag = 1), the sector number is incremented and the sector count register is decremented. If the BRDY line is asserted after the first sector is read out of the buffer, the WD1010-05 will continue to read data out of the buffer for the next sector. If BRDY is inactive, the WD1010-05 will raise BRDQ and wait for the host to place more data in the buffer.


WRITE SECTOR
RESET INTRQ, ERRORS, DRQ SET BSY, CIP
DRIVE # CHANGED
YES
NO
SCAN ID GET CYL #
CYL REGISTERS & INTERNAL CYL REGISTER SAME
NO
PERFORM SEEK COMMAND
YES
SEEK COMPLETE
NO
YES
ACTIVATE BDRQ, DRQ
BRDY ACTIVE
NO
YES
RESET BDRQ
2
ACTIVATE BCS PULSE BCR
WF
YES
NO
SEARCH FOR ID FIELD
1
1
CORRECT ID FOUND
NO
10 INDEXES
NOTE*
YES
NO
SCAN ID GET CYL #
2
YES
SET WG ON
WF
YES
NO
RESEEK TO CYL #
NO
RESEEK MADE
YES
2
PULSE BCR SET ID NOT FOUND INTRQ, RESET BSY, CIP DEACTIVATE BCS
WRITE DATA TO SECTOR THEN DEASSERT WG
IS M = 0
YES
NO
DEACTIVATE BCS PULSE BCR SET INTRQ; RESET BUSY, CIP
INCREMENT SECTOR NUMBER; DECREMENT SECTOR COUNT
SECTOR COUNT = 0
YES
NO
DEACTIVATE BCS PULSE BCR ACTIVATE BDRQ
BRDY ACTIVE
NO
YES
2
SET ABORTED COMMAND BIT
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
*If retries disabled then dashed path is taken after 2 index pulses.

In summary then, the write sector operation is as follows:

(1)	Host:	Sets up parameters; issues write sector command.
(2)	1010:	Sets BDRQ = 1, DRQ flag = 1.
(3)	Host:	Loads buffer with data (by $\overline{WE}$ strobes).
(4)	1010:	Waits for BRDY = low to high.
(5)	1010:	Finds specified ID field, write out sector.
(6)	1010:	If M = 0, then interrupt; End.
(7)	1010:	Increments sector number, decrements sector count.
(8)	1010:	If sector count = 0, then interrupt; End.
(9)	1010:	Go to (2).

SCAN ID

The scan ID command is used to update the head, sector size, sector number and cylinder registers.

The ready and write fault lines are checked throughout the command. When the first ID field is encountered, the ID information is loaded into the SDH, cylinder, and sector number registers. The internal cylinder position register is also updated. If a bad block is detected, the bad block bit will also be set. CRC is checked and if an error is found, the WD1010-05 will retry up to 10 revolutions to find an error-free ID field. There is no implied seek with this command and the buffer is left undisturbed.

FORMAT

The format command is used to format one track using the task file and the sector buffer. During this command, the sector buffer is used for additional parameter information instead of sector data. Shown in Figure 7 is the contents of the sector buffer for a 32 sector track format with an interleave factor of two. Each sector requires a two byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. A 00 is normal; a 80 hex indicates a bad block mark for that sector. In the example of Figure 7, sector 04 will get a bad block mark recorded.

The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded in any interleave factor desired. The remaining memory in the sector buffer may be filled with any value; its purpose is only to generate a BRDY to tell the WD1010-05 to begin formatting the track.

An implied seek is also in effect on this command. As in other commands, if the drive number has changed, an ID field will be scanned for cylinder position information before the implied seek is performed. If no ID field can be read (because the track had been erased or because an incompatible format had been used), an IDNF error will result and the Format command will be aborted. This can be avoided by issuing a Restore command before formatting.

The sector count register is used to hold the total number of sectors to be formatted, while the sector number register holds the number of bytes minus 3 to be used for Gap 1 and Gap 3; for instance, if the sector count register value is 2 and the sector number register value is 0, then 2 sectors are written and 3 bytes of 4E hex are written for Gap 1 and Gap 3. The data fields are filled with FF hex, and CRC is automatically generated and appended. The sector extension bit of the SDH register should not be set. After the last sector is written, 4E hex is filled until index.

The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave factor. The interleave factor is only important when 1:1

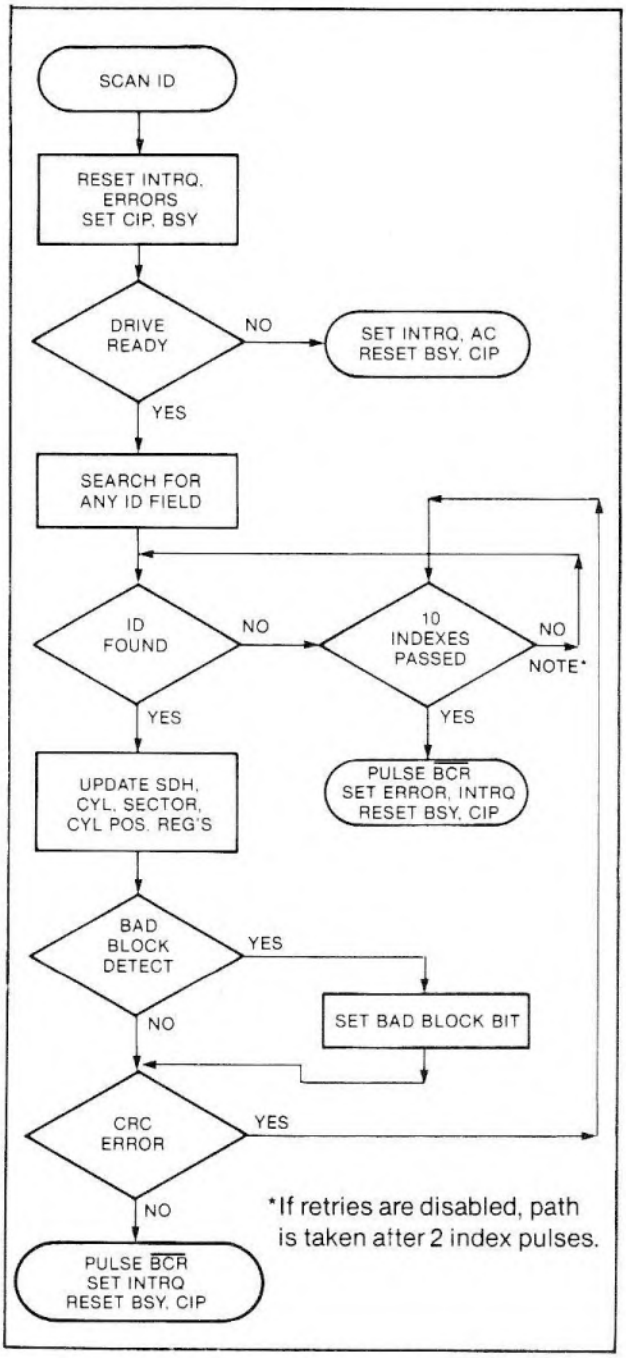
	DATA							
ADDR	0	1	2	3	4	5	6	7
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
:				:				
:				:				
F0	FF	FF	FF	FF	FF	FF	FF	FF

FIGURE 7.
FORMAT COMMAND BUFFER CONTENTS

interleave is used. The formula for determining the minimum Gap 3 value is:

Gap 3 = 2*M*S + K + E
M = motor speed variation (e.g. .03 for ± 3%)
S = sector length in bytes
K = 25 for interleave factor of 1
K = 0 for any other interleave factor
E = 7 if the sector is to be extended

Like all commands, a write fault or not ready condition will terminate the command. Figure 8 shows the format that the WD1010-05 will write on the Disk.



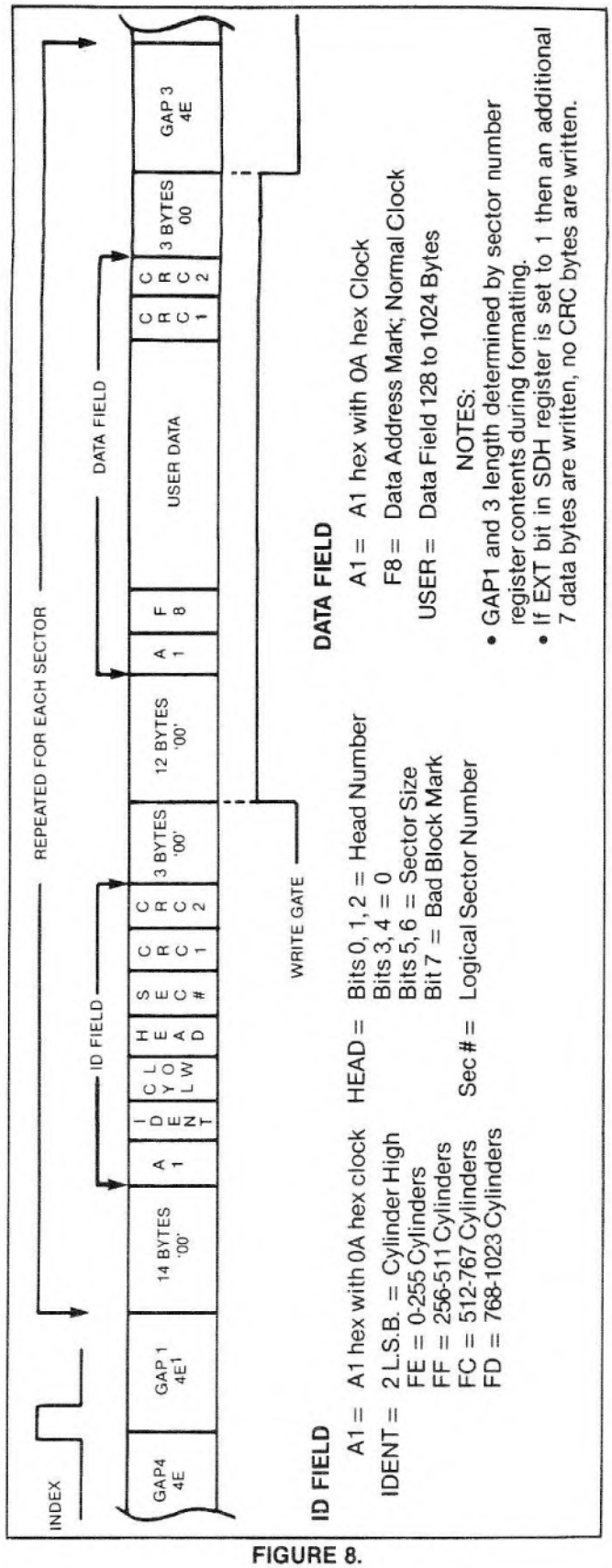
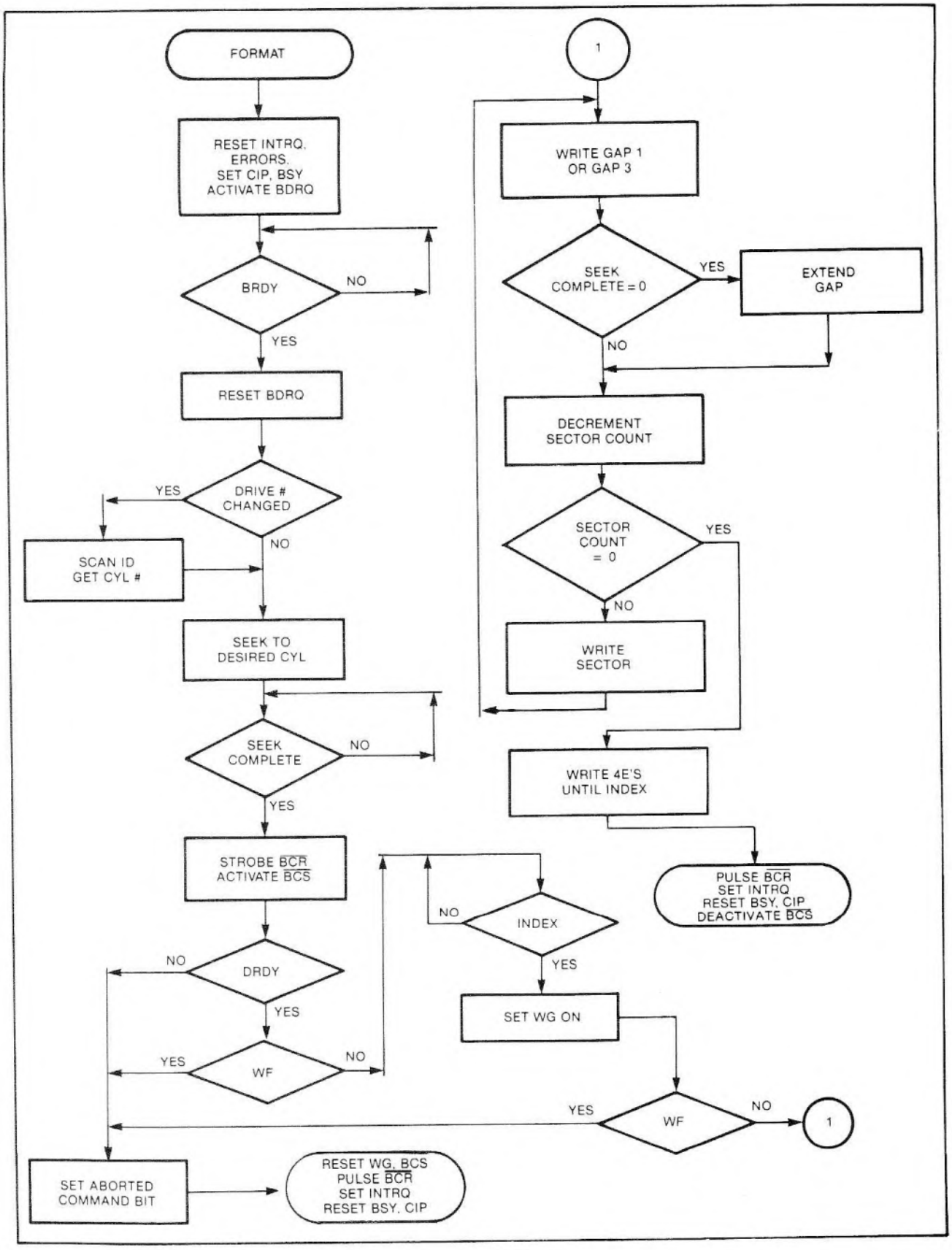


FIGURE 8. FORMAT


FORMAT
RESET INTRQ, ERRORS, SET CIP, BSY ACTIVATE BDRQ
BRDY
NO
YES
RESET BDRQ
DRIVE # CHANGED
YES
NO
SCAN ID GET CYL #
SEEK TO DESIRED CYL
SEEK COMPLETE
NO
YES
STROBE BCR ACTIVATE BCS
DRDY
NO
YES
WF
YES
NO
SET ABORTED COMMAND BIT
RESET WG, BCS PULSE BCR SET INTRQ RESET BSY, CIP
1
WRITE GAP 1 OR GAP 3
SEEK COMPLETE = 0
YES
EXTEND GAP
NO
DECREMENT SECTOR COUNT
SECTOR COUNT = 0
YES
NO
WRITE SECTOR
WRITE 4E'S UNTIL INDEX
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
INDEX
NO
YES
SET WG ON
WF
YES
NO
1

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

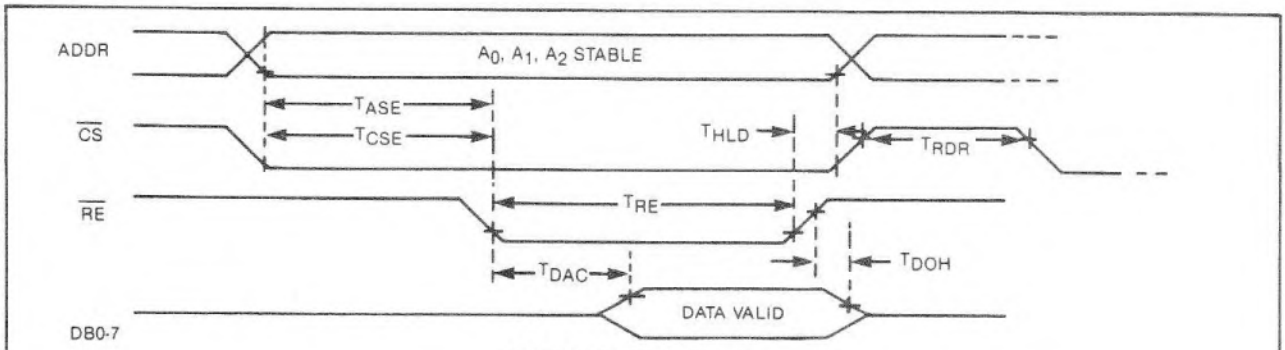
V_{CC} with respect to V_{SS} (Ground) . . . . . +7V
Max Voltage on any Pin with respect to V_{SS} . . . . . −0.5V to +7V
Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . −55°C to +125°C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		± 10	μA	V_{IN} = .4 to V_{CC}
I_{OL}	Output Leakage (Tristate & Open Drain)		± 10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = −100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6 mA
V_{OL}	Output Low Voltage (Pins 21-23)		0.45	V	IO = 4.8 mA See Note 10
I_{CC}	Supply Current		200	mA	All Outputs Open
	For Pins 25, 34, 37, 39:				
V_{IH}	Input High Voltage	4.6		V	
V_{IL}	Input Low Voltage		0.5	V	
TRS	Rise and Fall Time		30	ns	.9V to 4.2V points
C_{IN}	Input Capacitance		15	pF	

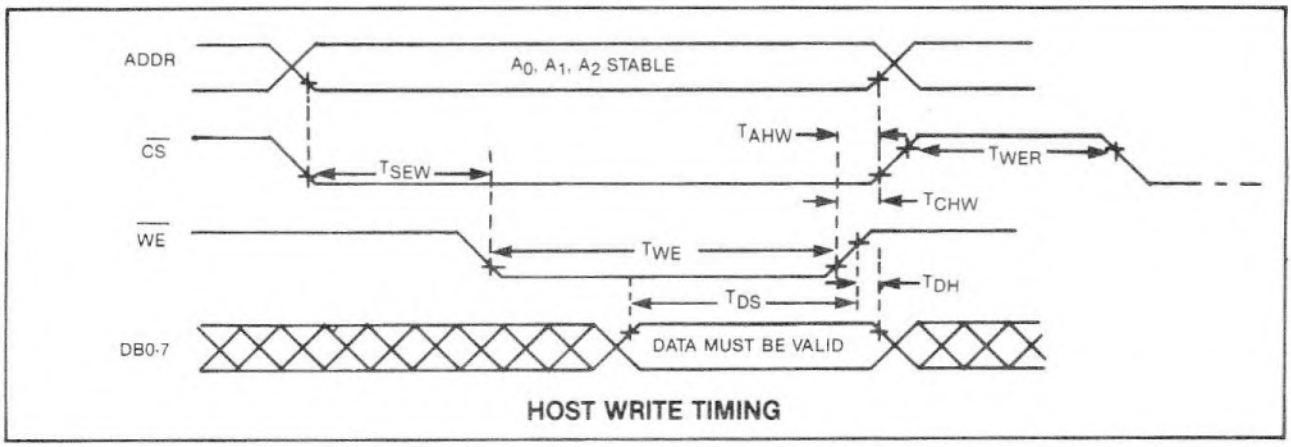
AC Timing Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V



HOST READ TIMING

HOST READ TIMING WD1010-05 WC = 5 MHZ

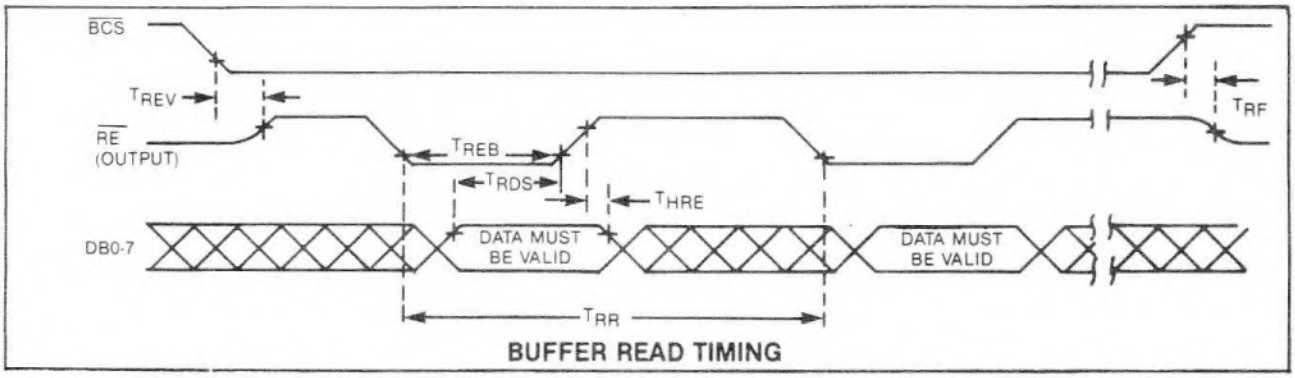
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{ASE}	ADDR Setup to $\overline{RE}$	100		ns	
T_{DAC}	Data Valid from $\overline{RE}$		375	ns	
T_{RE}	Read Enable Pulse Width	.4	10	μs	
T_{DOH}	Data Hold from $\overline{RE}$	20	200	ns	
T_{HLD}	ADDR, $\overline{CS}$, Hold from $\overline{RE}$	0		ns	
T_{RDR}	Read Recovery Time	300		ns	
T_{CSE}	$\overline{CS}$ Setup To $\overline{RE}$	0		ns	See Note 8



HOST WRITE TIMING

HOST WRITE TIMING WD1010-05

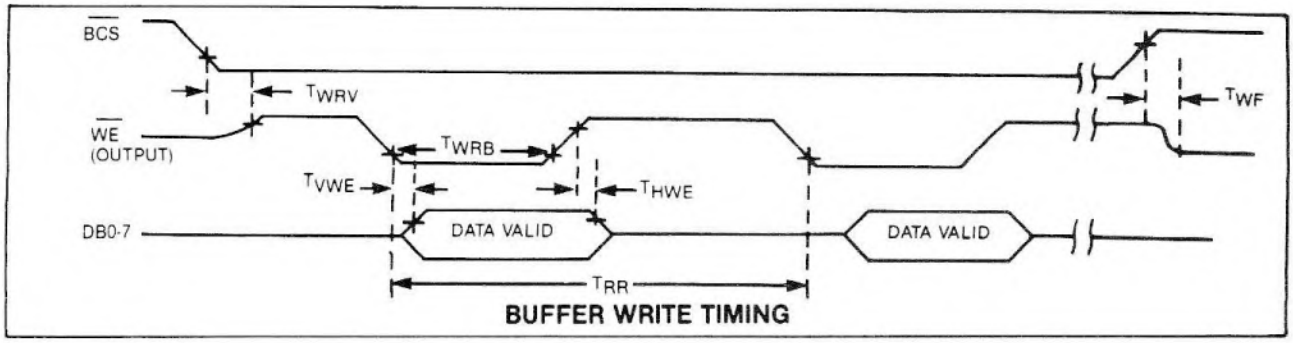
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{SEW}	ADDR, $\overline{CS}$ Setup to $\overline{WE}$	0	10	µs	
T_{DS}	Data Bus Setup to $\overline{WE}$	.2	10	µs	
T_{WE}	Write Enable Pulse Width	.2	10	µs	
T_{DH}	Data Bus Hold from $\overline{WE}$	10		ns	
T_{AHW}	ADDR Hold from $\overline{WE}$	30		ns	
T_{WER}	Write Recovery Time	1.0		µs	See Note 1
T_{CHW}	$\overline{CS}$ Hold Time from $\overline{WE}$	0			See Note 9



BUFFER READ TIMING

BUFFER READ TIMING (WRITE SECTOR CMD) WD1010-05 WC = 5 MHZ

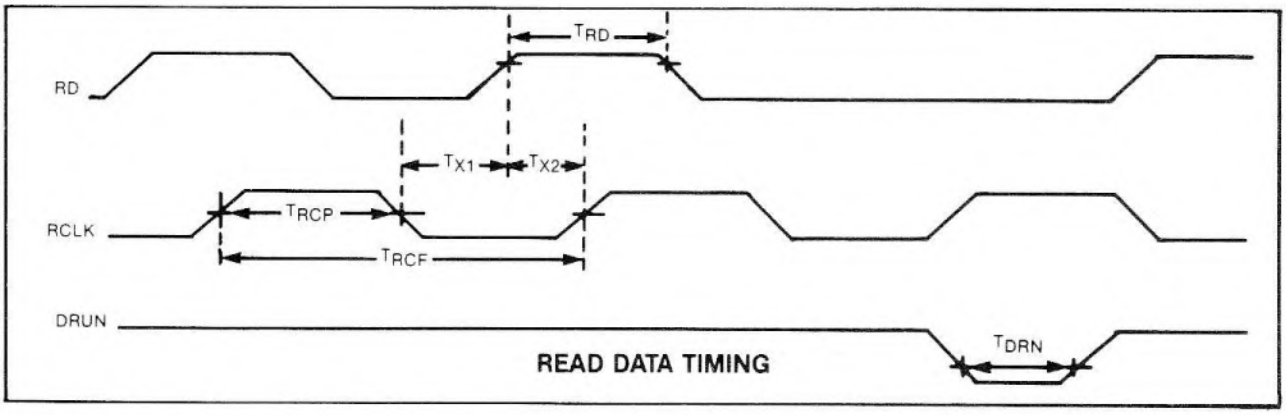
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	15		100	ns	C_L = 50 pf
T_{REB}	$\overline{RE}$ Output Pulse Width	300	400	500	ns	See Note 4
T_{RDS}	Data Setup to $\overline{RE}$	140			ns	
T_{RR}	$\overline{RE}$ Repetition Rate	1.2	1.6	2.0	µs	
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	ns	C_L = 50 pf
T_{HRE}	Data Hold from $\overline{RE}$	0			ns	



BUFFER WRITE TIMING

BUFFER WRITE TIMING (READ SECTOR CMD) WD1010-05 WC = 5 MHZ

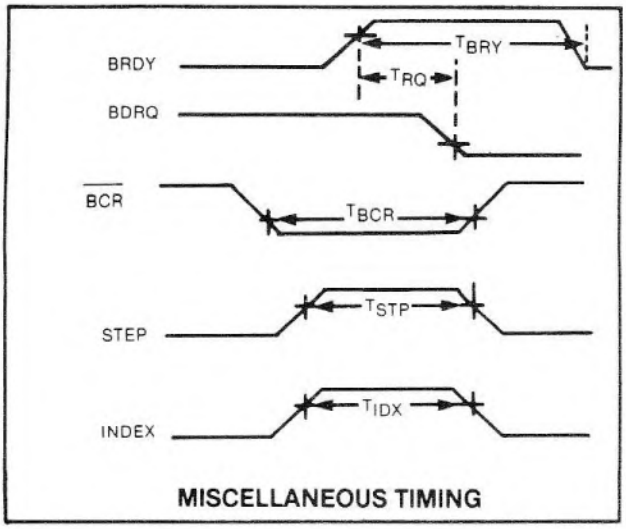
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	15		100	ns	C_L = 50 pf
T_{WRB}	$\overline{WE}$ Output Pulse Width	300	400	500	ns	See Note 4
T_{VWE}	Data Valid from $\overline{WE}$			150	ns	
T_{HWE}	Data Hold from $\overline{WE}$	60			ns	
T_{RR}	$\overline{WE}$ Repetition Rate	1.2	1.6	2.0	μs	See Note 2
T_{WF}	$\overline{WE}$ Float from $\overline{BCS}$	15		100	ns	C_L = 50 pf



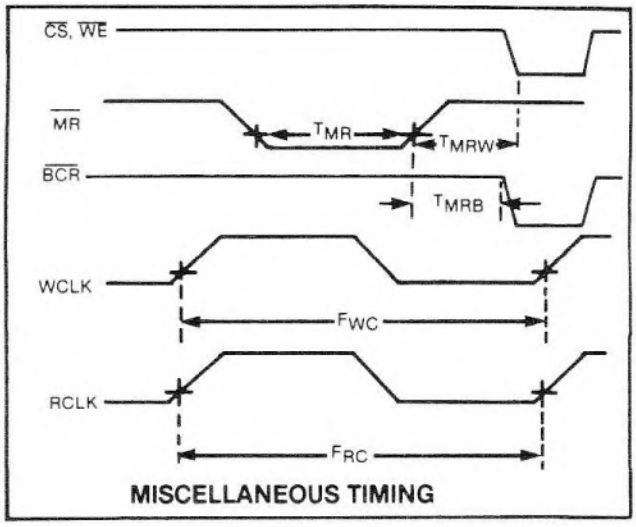
READ DATA TIMING

READ DATA TIMING WD1010-05 WC = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RCP}	RCLK Pulse Width	95		2000	ns	50% Duty Cycle
T_{X1}	RD from RCLK Transition	0		T_{RCP}	ns	
T_{X2}	RD to RCLK Transition	20		T_{RCP}	ns	
T_{RD}	RD Pulse Width	40		T_{RCP}	ns	
T_{DRN}	DRUN Pulse Width	30			ns	
T_{RCF}	RCLK Frequency	.250		5.25	MHZ	See Note 6



MISCELLANEOUS TIMING



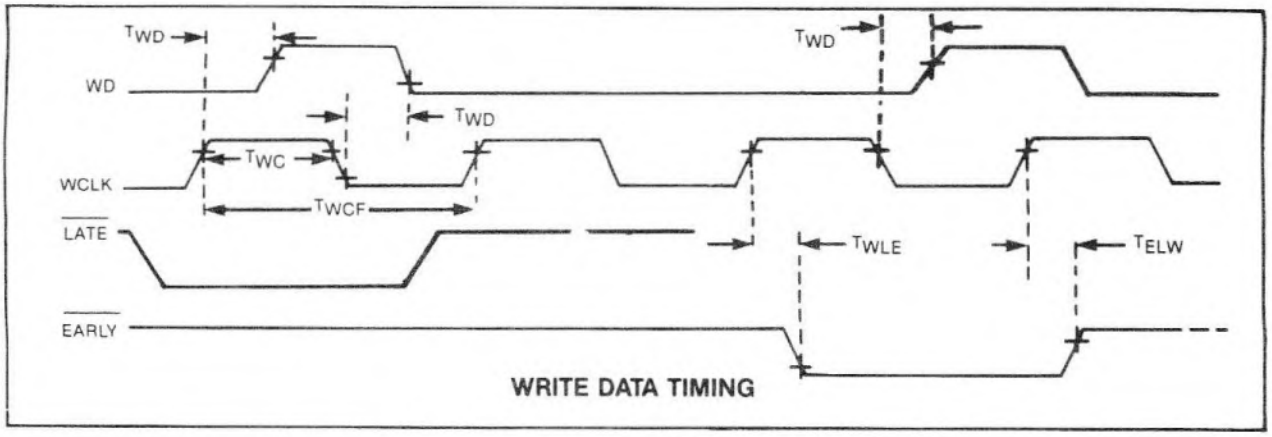
MISCELLANEOUS TIMING

MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RQ}	BDRQ Reset from BRDY	40		200	ns	
T_{BCR}	Buffer Counter Reset Pulse Width	1.4	1.6	1.8	μs	See Note 2
T_{STP}	Step Pulse Width	8.3	8.4	8.7	μs	See Note 2
T_{IDX}	Index Pulse Width	500			ns	
T_{MR}	Master Reset Pulse Width	24			WC	See Note 3
F_{WC}(-05)	Write Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle,
F_{RC}(-05)	Read Clock Frequency	.25	5.0	5.25	MHz	See Note 6
T_{BRY}	BRDY Pulse Width	800			ns	See Note 5
T_{MRB}	$\overline{MR}$ Trailing To $\overline{BCR}$	1.6	3.2	6.4	μs	See Note 2
T_{MRW}	$\overline{MR}$ Trailing To Host Write	6.4			μs	See Note 2

NOTES:
1. AC timing measured at V_{OH} = 2.0V, V_{OL} = 0.8V, C_L = 50 pf.
2. Based on WCLK = 5.0 MHz.
3. 24 WCLK periods (4.8 μsec at 5.0 MHz).
4. 2 WCLK ± 100 ns.
5. To drive a DMA controller, BRDY must be >4 μs or a spurious BDRQ pulse may exist for up to 4 μs after rising edge of BRDY.
6. T_{RCF} = T_{WCF} ± 15%.
7. 2 WCLK ± 50 ns.
8. $\overline{RE}$ may precede $\overline{CS}$ if $\overline{CS}$ plus $\overline{RE}$ meets the T_{RE} width.
9. $\overline{WE}$ may precede $\overline{CS}$ if $\overline{CS}$ plus $\overline{RE}$ meets the TWE width.
10. Pins 21-23 should be loaded with a 1K pullup resistor.

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WRITE DATA TIMING

WRITE DATA TIMING WD1010-05 WC = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WC}	WCLK Pulse Width	95		2000	ns	
T_{WD}	Prepagation Delay WCLK to WD	10		65	ns	
T_{WLE}	WCLK to Leading Early/Late	10		65	ns	
T_{ELW}	WCLK to Trailing Early/Late	10		65	ns	
T_{WCF}	WCLK Frequency	.250		5.25	MHZ	See Note 6

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FLEXIBLE CONTROLLER MATES WITH POPULAR WINCHESTER DRIVES

To take advantage of the growing demand for Seagate Technology-type 5¼-in. Winchester disk drives in personal computers, electronic work stations, and small-business systems, designers need an appropriate controller that is inexpensive. In fact, today's designs must implement the control link between a host CPU and a disk drive at far lower cost than the drive itself. That requires a single-chip controller rather than discrete, gate-array-intensive circuits that take up valuable board space in ever smaller computer equipment.

Such a device is now available in the form of an LSI single-chip Winchester controller-formatter. The chip incorporates 80% of the circuitry required for Winchester control, eliminating between 50 and 75 SSI and MSI devices used in earlier designs.

A controller that claims Seagate compatibility must be sufficiently flexible to meet not only the company's original ST506 specifications, but also the various deviations from them. The basic specifications include a data rate of 5.0 Mbits/s and open-collector outputs and differential signal inputs for the separate control and data interface cables. The recording format is modified frequency modulation (MFM), but more importantly, the structure of the format defines both specific address-mark bytes and ID fields. These are fixed specifications, but manufacturers of Seagate-type drives sometimes make other changes. For example, the track density on high-capacity drives may be greater than that in the original ST506 specifications. Also, the number of sectors and bytes per sector on each cylinder can vary according to the application. In each case, a compatible controller must be able to handle the original specifications plus the deviations.

The ST506 interface is a spinoff of the Shugart Associates SA1000 drive, first introduced in 1979. Two important differences between the interfaces are the data rates and a timing-clock differential signal on the SA1000. The latter operates at 4.34 Mbits/s vs 5 Mbits/s for the ST506, but the remaining signals have enough similarity to permit a single controller design to run either an 8-in. SA1000 drive or the 5¼-in. ST506 drive. The advantage of the WD1010 Winchester controller-formatter is that it works with either and with other manufacturers' variations as well.

Operation of the drive begins when a host processor initiates a command after first loading a set of internal task registers called the task file. Information such as cylinder, sector, and head number is written to these registers, which are selected by address lines. The memory-mapped register scheme allows individual accesses to each register. Thus the host need not waste valuable time reading all the registers to obtain a specific parameter.

The WD1010, which comes in a 40-pin DIP, is run by an internal microcontroller — a PLA (programmable logic array) serving as a state machine (Fig. 1). This logic controls the flow of data throughout the chip, recognizes and processes commands, and formats the data.

WRITING AND READING DATA

During a write operation, parallel data is read from the data bus and written to a specific sector. But first the cylinder and sector must be located on the requested disk drive. The WD1010's micro-controller accesses its internal cylinder-position data and compares it with the requested cylinder number. If necessary, a seek is performed automatically to position the head assembly over the desired cylinder.

If the drive requested is changed before a seek command is executed, the WD1010 enables its read logic and searches for an ID field on the currently selected drive. Then it reads the cylinder number from the new ID field and determines whether to seek in or out to find the requested cylinder. This so-called implied seek is a feature of all commands (see "Macro Commands Provide Multiple Options").

After the WD1010 finds an ID field that matches the cylinder, head, sector, sector size and CRC (cyclic redundancy check) value, it writes a field of 0s and a new address mark — later these two fields will be used for synchronization during a read operation. The chip then reads parallel data in from the data bus, serializes it, and converts it into the MFM format. Next, a new CRC value is calculated for the incoming data and is appended to the end of the data field (after the last byte). If the original command specified multiple sectors, the next logical sector must be searched for and the process repeated. After the last sector is written, the WD1010 gives the bus back to the host and waits for the next command.

Although the chip does not generate an error correction signal, an optional command bit can be set to disable cyclic redundancy checks of the data field. The sector is extended by seven bytes to allow the host to write its 56-bit error detection and correction code. Later, during a read operation, these seven bytes are transferred back to the host to permit it to identify a syndrome and correct any errors that were encountered. For systems that require such operations, the WD1014 error detection and correction and

WD1015 buffer controller chips are available.

Reading is similar to writing except that data is sent out on the data bus and written into the sector buffer at the host. MFM data is entered on the RD pin along with a synchronous clock (RCLK) generated from an external data separator (Figure 2).

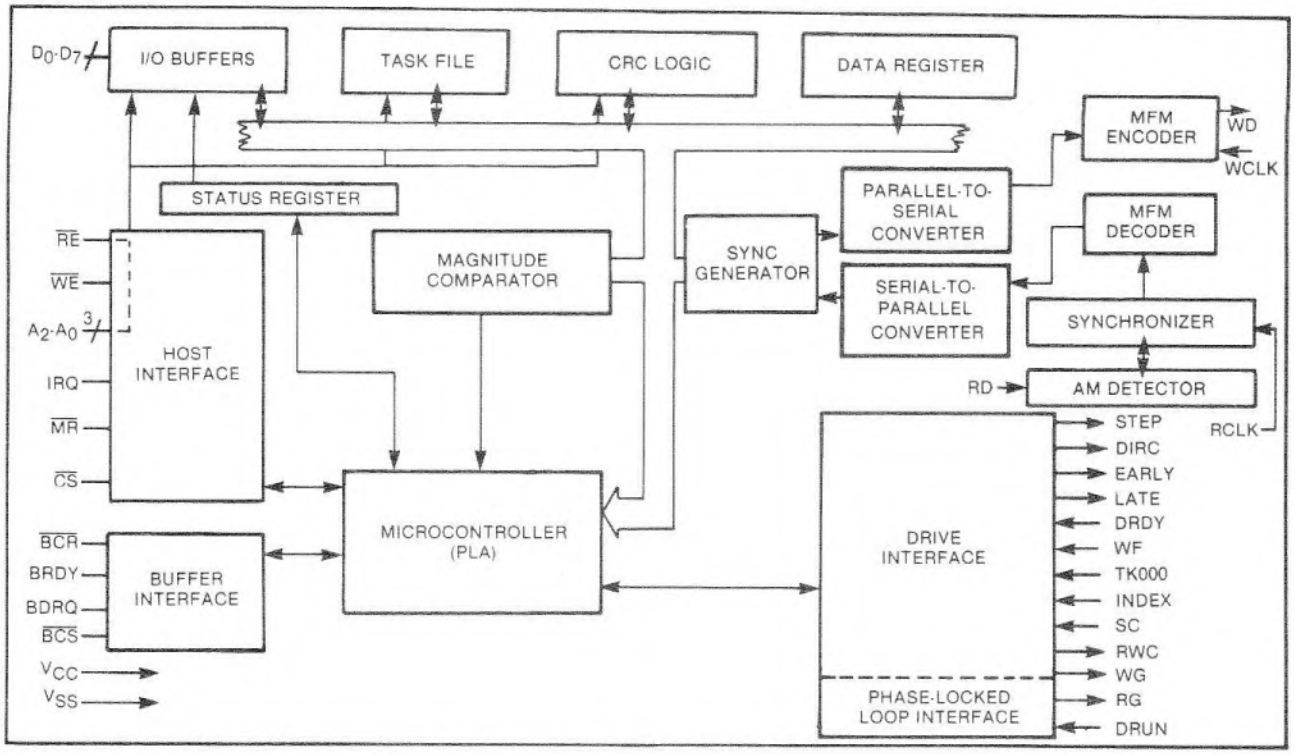


Figure 1.

The architecture of the WD1010 Winchester controller-formatter chip is designed to reduce a host processor's overhead burden. An internal microcontroller (PLA) manages data flow, incoming commands, and formatting.

Since the data rate is relatively high, the data separator must instruct the controller to lock on to the incoming data stream only during a field of 1s and 0s. A Data Run (DRUN) signal to the WD1010 indicates such an occurrence. When DRUN is active, the WD1010 counts off 16 bits — 2 byte times — sets the Read Gate (RG) signal, and starts to search the data stream for an address mark.

IMPLEMENTING THE PRECOMPENSATION ALGORITHM				
ALREADY SENT		SENDING	TO BE SENT	SHIFT REQUIRED
X	1	1	0	Early
X	0	1	1	Late
0	0	0	1	Early
1	0	0	0	Late

NOTE: All other patterns produce no shift.

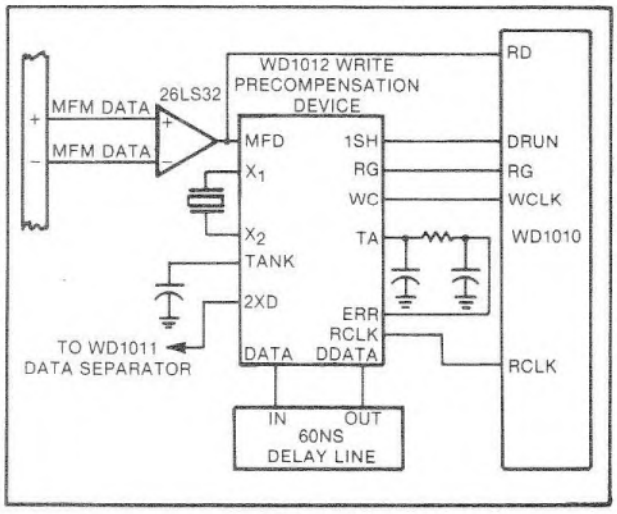


Figure 2.

A separate IC — the WD1012 — performs the data separation for the WD1010. The data separator sends a DRUN signal to the controller when it encounters a data field (1s and 0s).

An address mark is a unique pattern of clock and data bits that does not appear in any place that normal MFM data appears. If an address mark is not detected within nine bytes or if a non-0 pattern is detected within nine bytes, RG is turned off and the search repeated. Since data fields within sectors can contain 0s or all 1s, the DRUN algorithm is also triggered in these cases. But the address mark will not be detected, preventing erroneous data from being transferred.

After the ID field is compared and verified, a search begins for the address mark. Resynchronization occurs and the data is transferred to an internal MFM-to-NRZ converter. Data is then shifted through a double-buffered shift register and placed on the data bus for loading to the buffer. Either the cyclic redundancy code at the end of the data field is checked or the error detection and correction bytes are transferred in parallel to the host, depending on which option is used. Then the host processor can read the data from its local buffer.

Like all magnetic recording media, Winchester disks are not immune to the effects of bit shifts at high recording densities. The WD1010 uses an algorithm that informs external delay circuits when to shift outgoing data. A register within the task file specifies which cylinder receives reduced write current and if precompensation is needed. Typically, both occur on the same cylinder about half way down the disk surface.

The WD1010's precompensation signals are called $\overline{\text{Early}}$ and $\overline{\text{Late}}$. Depending on the bit pattern leaving the device, data will be shifted early, late, or not at all. A WD1011 data separator implements the precompensation delay network (Figure 3).

Since the $\overline{\text{Early}}$ signal and the current data (or clock) bits leaving the WD1010 have already occurred, the WD1011 performs no delay function on $\overline{\text{Early}}$. If both $\overline{\text{Early}}$ and $\overline{\text{Late}}$ are inactive, the WD1011 inserts a 12-ns delay; if only $\overline{\text{Late}}$ is active, it inserts a 24-ns delay. The result is a ± 12-ns shift of the data from its nominal position. An inactive Reduced Write Current (RWC) signal from the WD1010 disables the WD1011. The WD1010 then furnishes precompensation signals independent of current cylinder position.

INTERFACING WITH CABLES AND BUSES

The remaining function on the drive side is to provide sufficient buffers to drive the cables between the chip and the interface connectors. Single-ended open-collector signals are used for the control cable, and differential receiver-drivers are used for the data cable (Figure 4). Each line must have such buffers, since the controller is designed to drive one TTL load on all inputs and outputs.

At a 5-Mbit/s data transfer rate to the host interface, a byte of data must be read every 1.6 μs — in 8-bit parallel form. Few microprocessors can access a port and check status within this period. Consequently, a design objective of the WD1010 is compatibility with a programmed I/O environment, as well as the support of off-line error detection and correction. Moreover, the chip can transfer multiple sectors on one command. To achieve such performance within the constraints of a 40-pin package, the WD1010 relies on a unique approach to the traditional peripheral interface.

Three modes of communication can exist at the host interface: between the host and the WD1010, between the host and the buffer, and between the WD1010 and the buffer. For host-WD1010 commun-

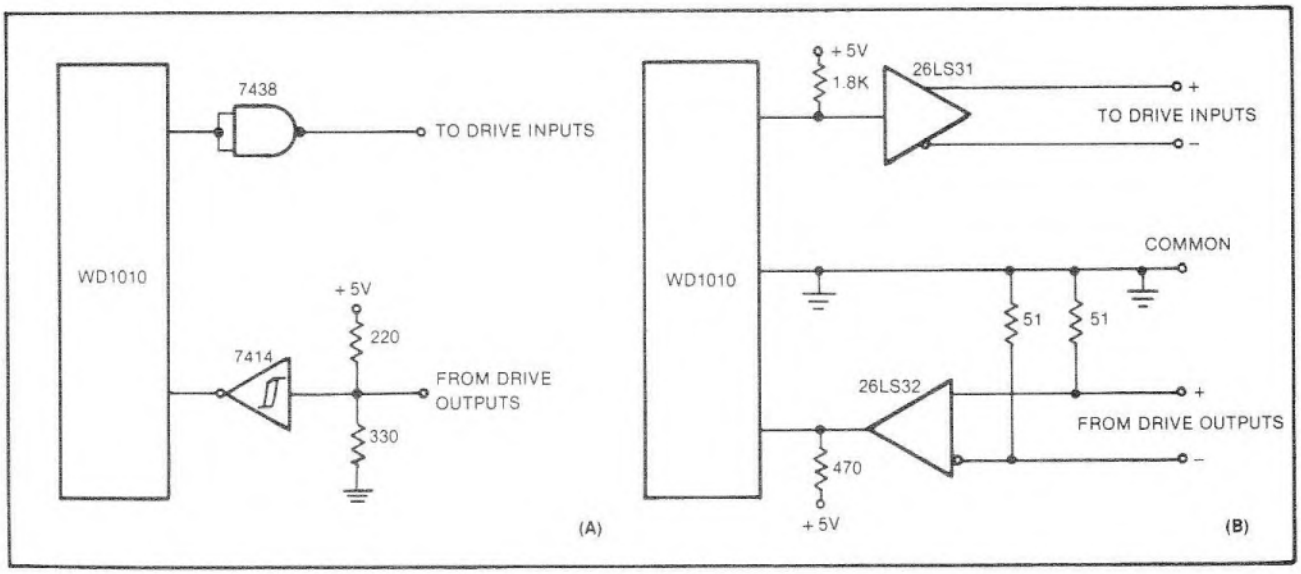


Figure 3.
Buffering circuits from the WD1010 to the control cable (A) and the data cable (B) must be used because the controller has a rather limited drive capability (one TTL load each on inputs and outputs).

ication the chip, like many microprocessors, talks over an 8-bit bidirectional bus, plus Read, Write and chip select lines (Figure 5). Three address lines access registers within the chip.

In host-buffer or WD1010-buffer communications (Figure 6), when the chip reads or writes to the buffer, the Buffer Chip Select ($\overline{BSC}$) line is pulled low. This signal should be used to disconnect the host data

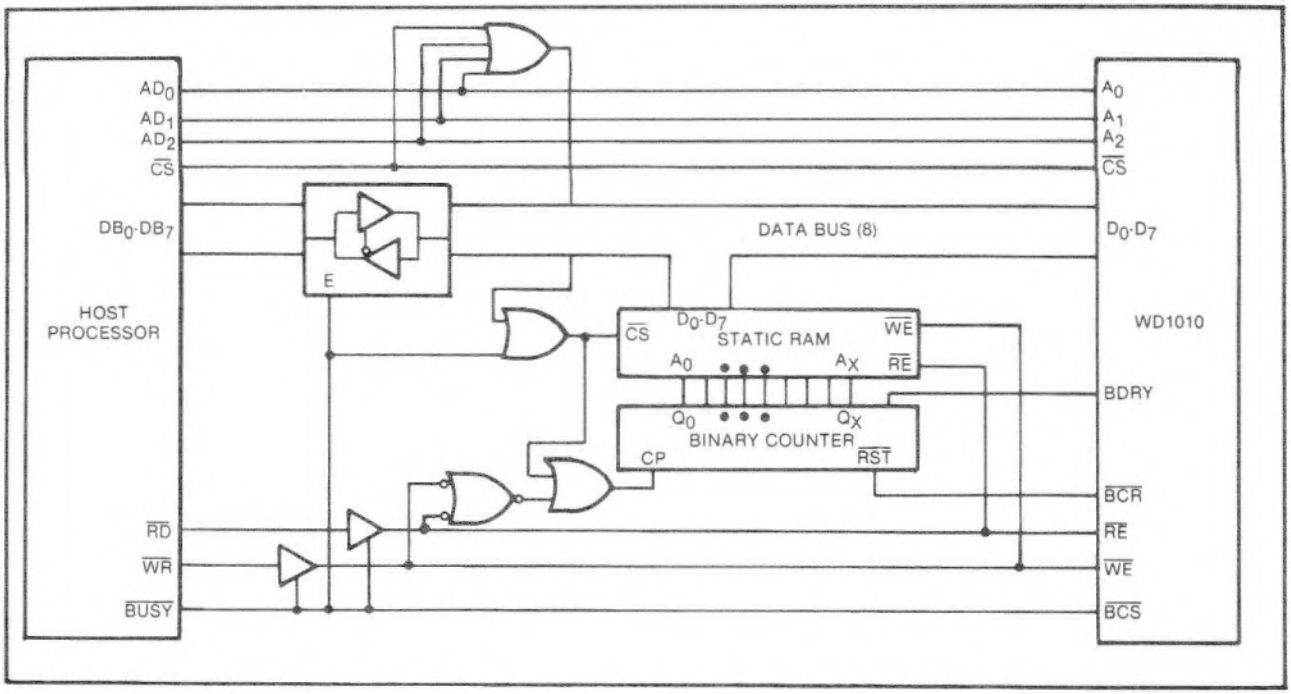


Figure 4.

Communications between a host and the WD1010 can be effected with the static RAM and binary counter circuitry shown here. These devices form a sector buffer that stores data sent from the host or the controller. This hardware handles both read and write operations on multiple sectors.

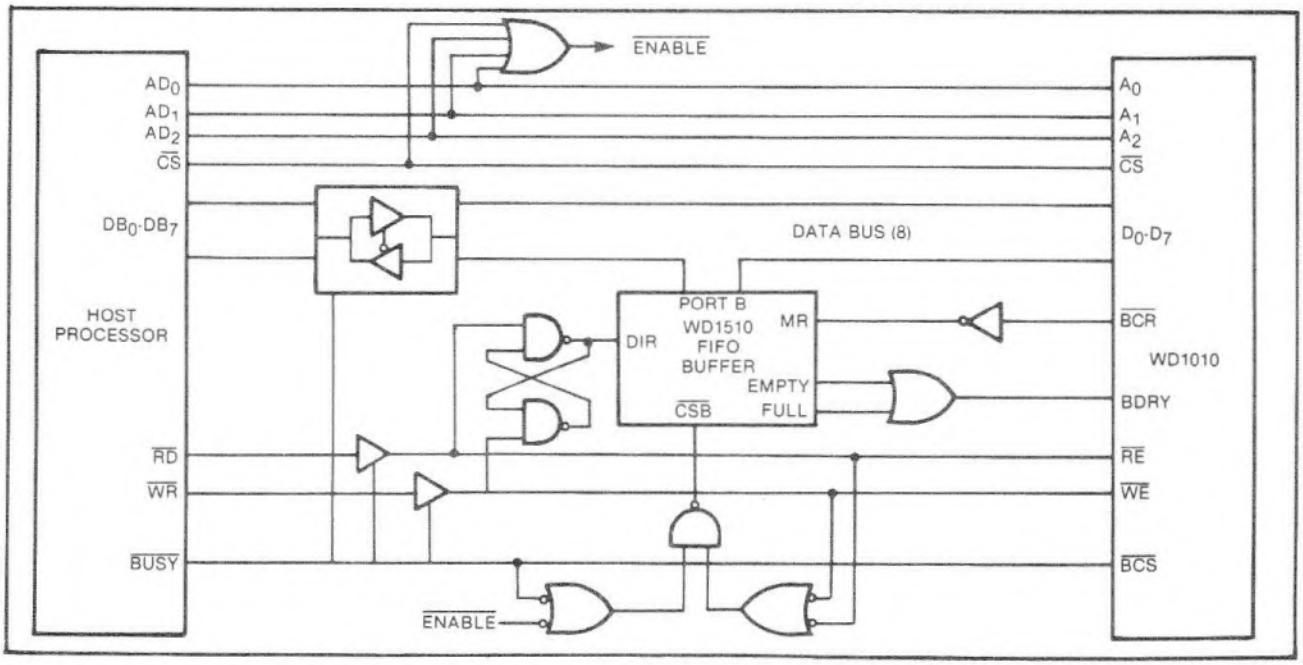


Figure 5.

A variation on the circuit of Figure 6 uses a WD1510 FIFO buffer to replace the counter-RAM circuitry. The scheme works well at high throughout rates since the buffer need not be filled to transfer data supplied by the WD1010 to the host.

bus and Read and Write lines from the WD1010. The Read ($\overline{RE}$) and Write ($\overline{WR}$) lines become outputs from the WD1010 and are strobed as each byte is placed on the bus.

The sector buffer in Figure 6 is implemented with a binary counter and a static RAM. With each $\overline{RE}$ or $\overline{WE}$ strobe, the counter is incremented so that the following byte can be read from or written to the next sequential location in the RAM. After all memory locations are written to, a carry signal from the counter goes to the Buffer Ready (BRDY) line of the WD1010. This signal informs the controller that the counter has rolled over and that the buffer is either full or empty, depending on the command.

During multiple-sector transfers, the RAM can be as large as the available sectors on each cylinder. The controller continues to load the RAM with data when a sector is being read. When no more memory is available. BRDY signals the WD1010. The command will then pause, wait for the host to dump the memory, and then begin filling the RAM again. This scheme permits both read and write operations on multiple sectors.

Signals for host and buffer control include the Buffer Counter Reset ($\overline{BCR}$) line, which is pulsed when $\overline{BCS}$ makes an active transition. $\overline{BCR}$ resets the binary counter before a read or write operation. Since address location 000 does not exist in the WD1010, a decoder can be used to make this address location enable the RAM and simulate a data register. For DMA applications, the Buffer Data Request (BRDQ) line is activated when data is available for host use.

Numerous other methods can be used with these same control signals. For example, a first-in, first-out buffer (Figure 7) can replace the counter-RAM. In this scheme, the host can dump data before the WD1010 fills the buffer. With sufficient throughput, the FIFO buffer need not have the storage capacity of an entire sector if the host can empty it quickly enough with a burst mode. In that case, the BRDY signal becomes the OR function of the Empty and Full signals from the FIFO buffer.

MACRO COMMANDS PROVIDE MULTIPLE OPTIONS

Each of the WD1010 Winchester controller-formatter's six macro commands contains several option flags. These flags allow the selection of stepping rates, multiple-sector transfers, and interrupt timing. The WD1010's task file contains additional options that are programmed before the command is actually issued. The operations of each command are as follows:

Restore causes the read/write head assembly to move to track 000. The stepping rate is determined by the state of Seek Complete (pin 32), which is activated by the drive to indicate its readiness. The stepping rate specified in the Restore command is not actually used but retained internally for an implied seek later on.

Activation of a Seek causes a seek operation for any desired cylinder. The selected cylinder is loaded into the cylinder register. Then the controller decides which way to seek and how many steps to use. The Seek Complete line is not checked, making possible overlapping seek operations on several drives.

The actual transfer of data from the WD1010 to sector buffer is performed under the Read Sector command. This command also causes a search for the specified cylinder, drive, head, and sector. Multiple sectors are specified and enabled through the sector count register. If the multiple-option flag is set, the number of sectors specified are transferred to the buffer.

Data in the sector buffer is written on the disk under the Write Sector command. Like the Read Sector command, it specifies and enables multiple drives through the sector count register.

Both the Read and Write Sector commands will retry up to eight times before automatically performing a restore operation. After a restoration, the controller seeks out the marginal sector and tries to determine whether an error condition was caused by a mispositioning of the head or a problem in the actuator.

The Format command is used to initialize a track with ID fields, gaps, and all information necessary for subsequent read and write operations. The sector buffer plays a unique role in this command, since it provides information on error mapping and inter-leaving rather than data from a sector. The order in which each sector is to be recorded is specified in the buffer, together with information indicating whether a sector contains a bad block or an error flag. Gap sizes, number of sectors, and other information are specified in the task file to allow further control over the format. By incrementing the cylinder number register, an entire surface can be formatted by accessing just two registers.

THER WD1010'S MACRO COMMANDS

	CODE							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Restore	0	0	0	1	R_3	R_2	R_1	R_0
Seek	0	1	1	1	R_3	R_2	R_1	R_0
Read Sector	0	0	1	0	1	M	0	0
Write Sector	0	0	1	1	0	M	0	0
Scan ID	0	1	0	0	0	0	0	0
Write Format	0	1	0	1	0	0	0	0

M = Multiple Sector Flag

M = 0 — transfer 1 sector
M = 1 — transfer multiple sectors

I = Interrupt Enable

I = 0 — Interrupt at BDRQ time
I = 1 — Interrupt at end of command

A MULTIPLE-DRIVE SYSTEM

For multiple drive-head configurations, the WD1010's sector-drive-head (SDH) register is decoded at address 110 to produce individual, latched drive-selection signals whenever the host writes to this address location. Binary head selection does not require a separate decoder, since one is located at the drive.

When the WD1010 senses a change in drive number, it automatically reads a cylinder. This takes place before the execution of the current command. The chip records the new cylinder number it has read and stores it internally as a reference for future seek operations on the current drive.

After the execution of any command, the WD1010 informs the host processor of any errors encountered during execution. On-board status and error registers report error conditions and signal status from the drive. To eliminate tedious error detection procedures, the host processor need only check the error bit in the status register to determine whether any bits are set in the error register.

Bit 0 of the status register is set if any of 5 bits in the 8-bit error register are set — bit 0 establishes the logical OR of the status register. Other error indicators include a Bad Block Detect bit, which is activated when an ID field contains a bad block mark, and an ID Not Found bit, which is set when the desired cylinder, head, sector, or size parameter is not found after 16 revolutions of the disk. The latter is also set if the data address mark of the data field is incorrect when a read is executed.

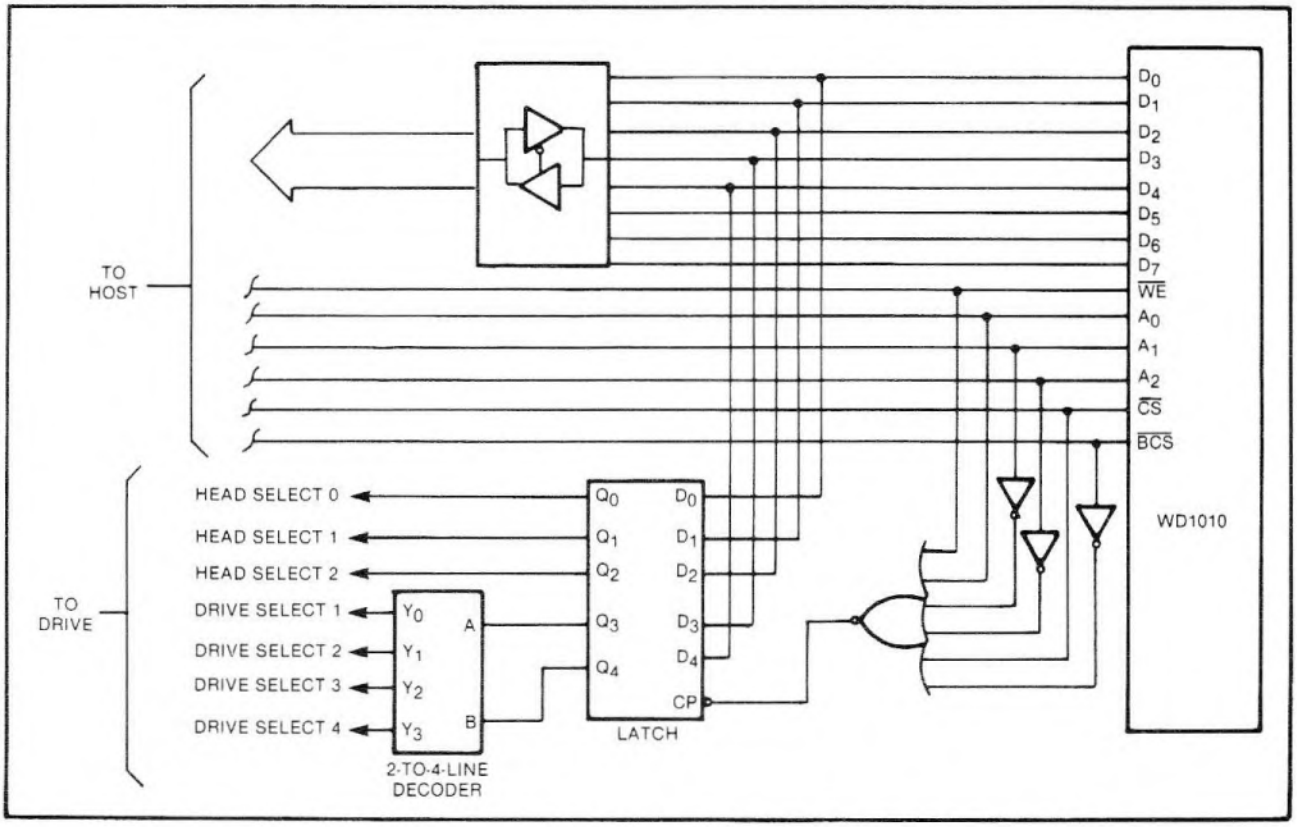


Figure 6.
Four Winchester drives can be controlled by the WD1010 using an external latch and a 2-to-4-line decoder. If the drive being accessed changes, the controller performs an automatic read operation. It records the cylinder number of the read for future seeks.

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WD1002S-WX2

Winchester

Disk Controller

OEM Manual

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SECTION I
INTRODUCTION

1.1 DOCUMENT SCOPE

This document provides the user with the information required to design related software drivers and interface connections for efficient use of the WD1002S-WX2 Winchester Disk Controller Board. It is to the user's advantage to become familiar with the following related documents:

WD11C00-17 Logic Array . . . . . Data Sheet
WD10C20 Winchester Data Separator and
Write Precompensation Device . . . . . Data Sheet
WD1010-05 Winchester Disk
Controller . . . . . Data Sheet
WD1010 Winchester Disk
Controller . . . . . Application Note
WD1015 Buffer Manager Control
Processor . . . . . Data Sheet
ST-506 Micro Winchester Disk
Interface ST506
Seagate Technology
Scotts Valley, Cal.

1.2 DESCRIPTION

The WD1002S-WX2 is a stand-alone, general purpose Winchester Disk Controller. The WD1002S-WX2 interfaces up to two Winchester Disk drives and a Host Processor, e.g. an IBM XT.

The Winchester interface conforms to the Seagate Technology ST506 interface. All necessary receivers and drivers are included on the board, allowing direct connection to the disk drive(s).

A separate computer access port enables communications between the Host and disk controller. An 8-bit bi-directional bus and appropriate control signals comprise this port. Disk read or write data, status information, and command parameters are transferred via this bus. An on-board data buffer allows bus transfers to be executed independently of the drive's data transfer.

The WD1002S-WX2 is based on a proprietary chip set consisting of the WD11C00-17, WD1010A-05, WD10C20, and WD1015.

1.3 FEATURES

- 8-BIT BI-DIRECTIONAL BUS HOST INTERFACE
- IBM XT WINCHESTER CONTROLLER EMULATION, IBM PC HOST INTERFACE
- WD10C20 WINCHESTER DATA SEPARATOR AND WRITE PRECOMPENSATION DEVICE
- WD11C00-17 LOGIC ARRAY
- DATA RATES UP TO 5 MBITS/SEC
- CONTROLS UP TO 2 DRIVES USING SEAGATE TECHNOLOGY ST506
- SUPPORTS DRIVES OF ANY CONFIGURATION UP TO 1024 CYLINDERS AND 16 R/W HEADS WITH THE WD1015-24 OR 8 R/W HEADS WITH THE WD1015-14
- THE CONTROLLED DRIVES NEED NOT BE OF THE SAME CAPACITY OR CONFIGURATION
- ERROR CORRECTION ON DATA FIELD ERRORS, CRC ID FIELD VERIFICATION
- 32 BIT ECC POLYNOMIAL FOR ERROR DETECTION AND CORRECTION
- READ AND WRITE LONG COMMANDS FOR CHECKING ERROR CORRECTION CIRCUITRY
- SELECTABLE AUTOMATIC RETRIES ON ALL ERRORS
- AUTOMATIC RESTORE AND RE-SEEK ON ALL SEEK ERRORS
- AUTOMATIC FORMATTING
- 512 BYTES PER SECTOR
- SECTOR INTERLEAVE CAPABILITY
- MULTIPLE SECTOR READS AND WRITES
- OVERLAPPED SEEK CAPABILITY ON BUFFERED-STEP DRIVES
- SUPPORTS IMPLIED SEEKS ON ALL COMMANDS
- INTERNAL DIAGNOSTICS
- DMA TRANSFER CAPABILITY
- SUPPORTS INTERRUPTS, INTERRUPT REQUESTS, AND DMA REQUEST SHARING
- INCLUDES SOCKET FOR USER SUPPLIED 2716, 2732, OR 2764 ROM
- BIOS AVAILABLE

1.4 OPERATION

This section provides an operational overview of the WD1002S-WX2 Winchester Disk Controller. For a detailed explanation, refer to Section 6 (Theory of Operation). As illustrated in Figure 1-1, the WD1002S-WX2 consists of the following components:

Bi-directional Control/Data Bus
Address Decoding Logic
Configuration Switches
Basic Input/Output System (BIOS) ROM
WD11C00-17
WD10C20
Sector Buffer RAM
WD1010A-05
WD1015
Reset Logic

1.4.1 BI-DIRECTIONAL CONTROL/DATA BUS

The 8-bit, bi-directional bus transmits addresses, commands, data, and status information. This bus links the WD1002S-WX2 to the Host. Specifically, this bus transmits data between the Host and Sector Buffer RAM.

1.4.2 ADDRESS DECODING LOGIC

The puspose of this logic is to decode a valid device address from the Host.

1.4.3 CONFIGURATION JUMPERS

These jumpers configure the WD1002S-WX2 for different disk drive capacities.

1.4.4 BIOS ROM

The Host, after powering up, interrogates its ports to determine what devices are connected. The Host uses information supplied by the BIOS ROM to perform an install operation. Then, during normal operation, the BIOS operates much like a driver that is resident in the Host's memory space. The BIOS ROM is addressed at Host memory locations C8000-C8FFF. The BIOS is addressed by the A0 through A19 bus. Outputs to the Host are via the Intraboard Command/Status bus (BD0 through BD7) and Host Interface Data/Command bus (D0 through D7).

1.4.5 WD11C00-17

The WD11C00-17 incorporates several functions in a single package. Implementation of these functions occurs by combining random logic and specialized circuits. The WD11C00-17 contains the following circuits:

Status ports
Read and write ports
Sector Buffer RAM addressing and control
ECC
Reset timing

The WD11C00-17 connects directly to the Host Interface Data/Command and Intraboard Command/Data (AD0-AD7) buses.

1.4.6 WD10C20

The WD10C20 performs phase-locked loop data synchronization on read data from the Winchester drives. This device also conditions write data to be recorded on the disk. The WD10C20 includes both frequency and phase detection. Zero phase error start-up circuitry eliminates problems due to asymmetry. The WD10C20 requires no adjustments and contains all data synchronization and write precompensation circuitry in a single device.

1.4.7 SECTOR BUFFER RAM

The Sector Buffer RAM is a 2K x 8 RAM. The Sector Buffer allows Host data transfers independent of the actual drive data transfer rate. The Sector Buffer temporarily stores the following information:

Sector data during Read and Write Commands
Disk format information during a Format Command
Drive characteristics during a Set Parameters Command

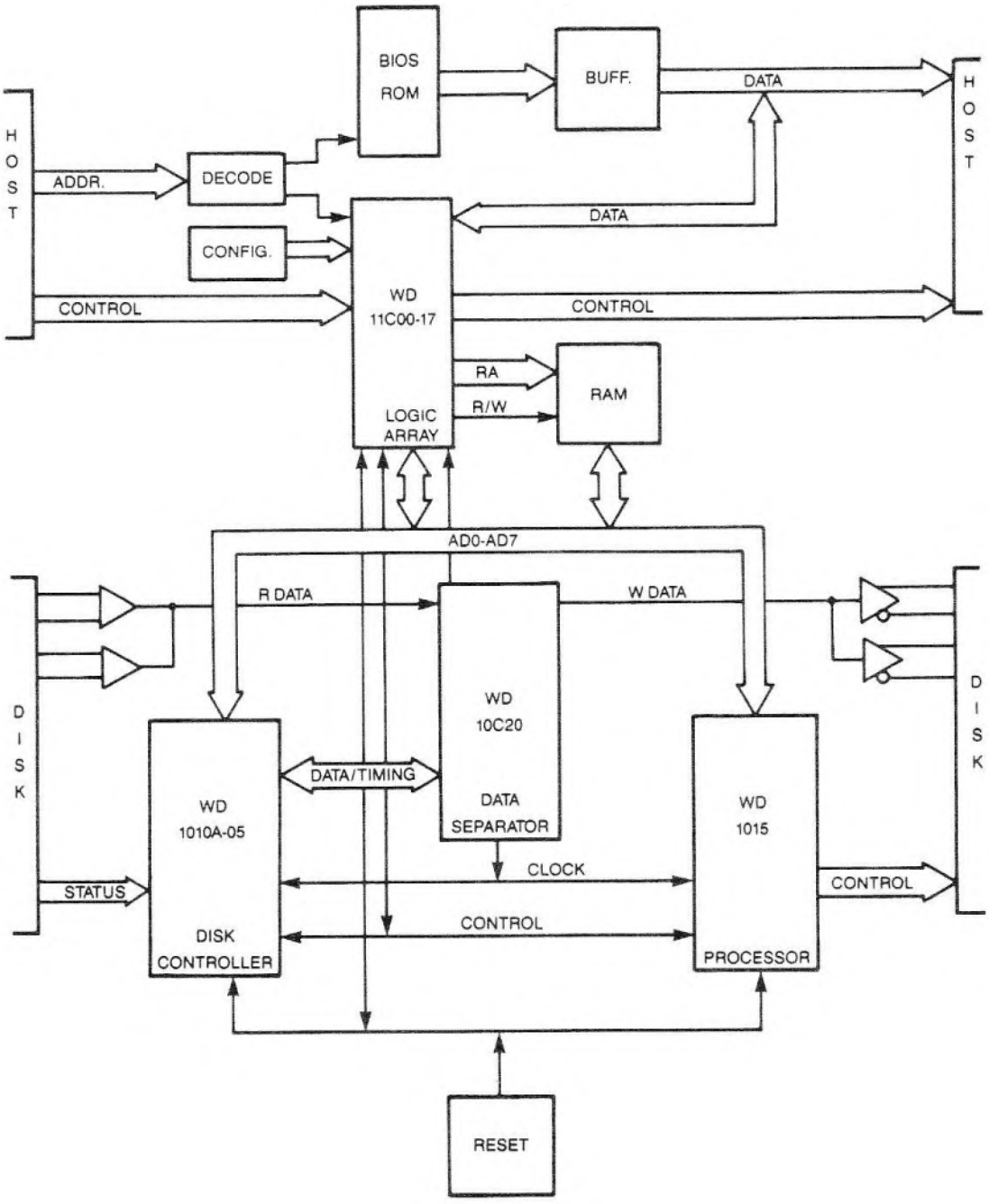


FIGURE 1-1. WD1002S-WX2 FUNCTIONAL BLOCK DIAGRAM

1.4.8 WD1010A-05

The primary function of the WD1010A-05 is to control data transfers between the disk and the Sector Buffer. Data transfers take place after the WD1015 Buffer Manager Control Processor positions the selected head over the desired track. The WD1010A-05 receives the parameters and commands from the WD1015 via the AD0 through AD7 bus. The WD1010A-05 interprets the parameter or command, determines which sectors are involved, and whether a read, write, or format function is required.

1.4.9 WD1015

The WD1015 manages and controls all commands and communications between the Host and WD1010A-05. The WD1015 controls ECC and CRC functions.

There are two versions of the WD1015. Table 1-1 describes the differences between the two versions of the WD1015. The acronym WD1015 refers to both versions. When a specific reference is made to a specific version, the appropriate acronym is used.

TABLE 1-1. WD1015 DESCRIPTION

FUNCTION	WD1015-14	WD1015-24	REMARKS
Execution of automatic self-test after Reset command or power-up	Yes	No	
Supports 16 heads	No	Yes	The WD1015-14 supports up to eight heads. The WD1015-14 uses the REDUCED WRITE CURRENT ($\overline{\text{RWC}}$) signal. The WD1015-24 supports up to 16 heads. The WD1015-24 uses the $\overline{\text{RWC}}$ pin on J1 as HEAD SELECT 3 ($\overline{\text{HS3}}$). Refer to Sections 3 and 7 for further details.
3.5 seconds time-out on single track steps	No	Yes	3.5 seconds time-out allows removable/servo drives time to create servo map. WD1015-14 allows 1 second.
Bit 4 of opcode in Command Control	Valid	Don't care	Refer to Section 5 for further details.
Step rates			Refer to Section 5 for further details.
Format Bad Track			Refer to Section 5 for further details.

1.4.10 RESET LOGIC

The Reset Logic initializes the internal circuitry of the WD1002S-WX2 during the power-up process or a low voltage condition. The Reset Logic also disables the $\overline{\text{WRITE GATE}}$ signal. Disabling $\overline{\text{WRITE GATE}}$ prevents writing spurious data to the disk drive during power up, power down or a low voltage condition.

SECTION II
SPECIFICATIONS

2.1 GENERAL

This section contains the overall specifications for the WD1002S-WX2 Winchester Disk Controller.

2.2 ELECTRICAL

2.2.1 HOST INTERFACE

Type	IBM PC
Max Cable Length	Connects directly to Host motherboard with a 62 pin card edge connector

2.2.2 DRIVE INTERFACE

Encoding Method	MFM
Cylinders per Drive	Up to 1024
Sectors per Track	17
Bytes per Sector	512
Heads	8 with WD1015-14 16 with WD1015-24
Drive Selects	2
Stepping Rates	70µsec, 200µsec, 3msec (WD1015-14) 18 µsec, 30 µsec, 45µsec, 60µsec, 75µsec, 210µsec, 3msec (WD1015-24)
Data Transfer Rate	5Mbits/sec (ST506)
Write Precomp Time	12nsec
Sectoring	Soft
CRC Polynomial	$X^{16} + X^{12} + X^5 + 1$
ECC Polynomial	$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$
Reciprocal ECC Polynomial	$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^6 + X^4 + 1$
Miscorrection Prob.	5 bit correction = < 1.6 E-5
Non-detection Prob.	< 2.3 E-10
Correction Span	Up to 11-bit burst
Max Cable Length:	
Control (Total Daisy Chain)	3 meters (10 ft.)
Data (Radial-each)	3 meters (10 ft.)

2.2.3 WD10C20

Acquisition Time	< or = 12.8µs
Capture Range	± 2.2% to 1ns after 12.8µs acquisition
Bit Jitter Tolerance	± -34ns (min. of 40 db after acquisition)
Asymmetry Tolerance	34ns (write precompensation turned off; as measured over constant RCLK pattern)

2.2.4 POWER

Voltage	5V ±5%
Current	0.8 amps max.
Ripple	0.1 volts max., 25 mV typical
Voltage	+12V ±10%
Current	10 mA. max.

2.3 PHYSICAL

Form factor	IBM PC
Length	20.6 centimeters (8.1 inches)
Width	9.78 centimeters (3.85 inches)
Height (max. including board, components & leads)	1.27 centimeters (0.50 inches)

2.4 ENVIRONMENTAL

Ambient Temperature	0°C (32°F) to 55°C (131°F)
Relative Humidity	10% to 95% non-condensing
Altitude	0 to 3000 meters (10,000 ft.)
Air Flow	100 lin ft/min. at 0.5" from component surfaces.
MTBF	10,000 POH
MTTR	30 Minutes

SECTION III
INTERFACE CONNECTIONS

3.1 ORGANIZATION

The WD1002S-WX2 has four on-board connectors for user application.

P1 Host interface: 62 pin IBM PC compatible card edge connector.

J1 Drive control: 34 pin dual row header connector daisy-chained to two drives. The control signals at the second drive from the WD1002S-WX2 (no more than a total length of 3 meters or 10 feet) are terminated with a 220 ohm resistor to +5V and a 330 ohm resistor to ground.

J2, J3 Drive data: 20 pin dual row header connectors, radially connected each to its own drive.

3.2 HOST INTERFACE

Connector P1 pins A1 through A31 are on the component side of the board and B1 through B31 are on the artwork side. Table 3-1 describes the Host interface connector (P1) pin assignments and functions.

TABLE 3-1. HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
A1		Not Connected		
A2 thru A9	D7 thru D0	DATA 7 thru DATA 0	I/O	8-Bit, tri-state, bi-directional bus. It is used to transmit data between the Host and Sector Buffer, the Command Block to the WD1015, status and drive configuration to the Host. The BIOS transmits parameter information and commands to the Host via this bus.
A10		Not Connected		
A11	AEN	ADDRESS ENABLE	I	AEN is asserted during a DMA mode of operation making the I/O ports 320 hex thru 323 hex inaccessible to the Host. Data transfers and intra-bus control is initiated by asserting $\overline{\text{DACK3}}$. The BIOS ROM can still be addressed via A0-A19.
A12 thru A31	A19 thru A0	ADDRESS BUS A19 thru A0	I	A0 thru A9 are used during programmed I/O mode of operation to address ports 320 hex thru 323 hex. They are inhibited during DMA by AEN. A0 thru A19 addresses the BIOS ROM regardless of the state of AEN.
B1	GND	GROUND		
B2	RST	RESET	I	When asserted, RST places the WD1002S-WX2 into its initial power-up state.
B3	+5VDC	+5VDC		+5VDC
B4	IRQ2	INTERRUPT REQUEST LEVEL 2	O	The WD1002S-WX2 asserts IRQ2 to interrupt the Host upon the completion of a command. Use of IRQ2 is jumper selectable. Use of IRQ5 is standard. Refer to Section 7 for further details on jumper selectable options.
B5 thru B8		Not Connected		
B9	+12VDC	+12VDC		+12VDC
B10	GND	GROUND		
B11		Not Connected		

TABLE 3-1. HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION (CONT'D.)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
B12	$\overline{\text{MEMR}}$	$\overline{\text{MEMORY READ}}$	I	The Host, to read the BIOS ROM places the address on A0 thru A19, asserts $\overline{\text{MEMR}}$ and receives the data via D0 thru D7 data bus.
B13	$\overline{\text{IOW}}$	$\overline{\text{I/O WRITE}}$	I	The Host or DMA controller asserts $\overline{\text{IOW}}$ when a data byte is to be written to the WD1002S-WX2.
B14	$\overline{\text{IOR}}$	$\overline{\text{I/O READ}}$	I	The Host or DMA controller asserts $\overline{\text{IOR}}$ when a data or status byte is to be read from the WD1002S-WX2.
B15	$\overline{\text{DACK3}}$	$\overline{\text{DMA ACKNOWLEDGE CHANNEL 3}}$	I	The DMA controller asserts $\overline{\text{DACK3}}$ in response to DRQ3 sent by the WD1002S-WX2. $\overline{\text{DACK3}}$ enables DMA data transfer, bypassing port 320 which was disabled by AEN.
B16	DRQ3	DMA REQUEST CHANNEL 3	O	WD1002S-WX2 asserts DRQ3 to inform the DMA controller that data is available for transfer.
B17 thru B22		Not Connected		
B23	IRQ5	INTERRUPT REQUEST LEVEL 5	O	The WD1002S-WX2 asserts IRQ5 to interrupt the Host upon the completion of a command.
B24 thru B28		Not Connected		
B29	+5VDC	+5VDC		+5VDC
B30		Not Connected		
B31	GND	GROUND		

3.3 DRIVE INTERFACE

3.3.1 DRIVE CONTROL

Control signals are common to all drives and are daisy-chained to the drives from a single connector, J1. To terminate the control signals properly, the last drive in the daisy-chain must have a 220/330 ohm resistor pack installed. Table 3-2 describes the drive control connector (J1) pin assignments and functions.

TABLE 3-2. DRIVE CONTROL CONNECTOR (J1) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
1	2	$\overline{\text{RWC/HS3}}$	$\overline{\text{REDUCE WRITE CURRENT/HEAD SELECT 3}}$	O	The WD1015-14 allows this pin to be used as the $\overline{\text{RWC}}$ pin. The WD1015-24 uses this pin as $\overline{\text{HS3}}$. Refer to Section 7 for further details. $\overline{\text{RWC}}$ is used by the drive to reduce the write current on the inner cylinders. This lessens the bit shift caused by the greater bit density on these cylinders. $\overline{\text{RWC}}$ is asserted when the specified cylinder is reached. $\overline{\text{HS3}}$ is one of four Head Select signals decoded by the drive to select one of 16 R/W heads.
3	4	$\overline{\text{HS2}}$	$\overline{\text{HEAD SELECT 2}}$	O	$\overline{\text{HS2}}$ is one of three (or four) Head Select signals decoded by the drive to select one of eight (or 16) R/W heads.
5	6	$\overline{\text{WG}}$	$\overline{\text{WRITE GATE}}$	O	$\overline{\text{WG}}$ is asserted when valid data is to be written. It is used by the drive to enable the write current to the head. WD1002S-WX2 de-asserts this signal when a $\overline{\text{WF}}$ is detected. Circuitry is included to ensure the output does not glitch during power on, power down or power failure.
7	8	$\overline{\text{SC}}$	$\overline{\text{SEEK COMPLETE}}$	I	$\overline{\text{SC}}$ informs the WD1002S-WX2 that the selected head has reached the desired cylinder and has stabilized. Since $\overline{\text{SC}}$ is not checked after a Seek Command, overlapped seeks are allowed.
9	10	$\overline{\text{TK000}}$	$\overline{\text{TRACK 000}}$	I	The drive asserts this signal when the heads are positioned over the outermost cylinder, cylinder 0.
11	12	$\overline{\text{WF}}$	$\overline{\text{WRITE FAULT}}$	I	$\overline{\text{WF}}$ is asserted by the drive when a write error occurs. The command in progress aborts and no other command can be executed while this signal is asserted.
13	14	$\overline{\text{HS0}}$	$\overline{\text{HEAD SELECT 0}}$	O	$\overline{\text{HS0}}$ is one of three (or four) Head Select signals decoded by the drive to select one of eight (or 16) R/W heads.
15		GND	GROUND		
	16		Not Connected		
17	18	$\overline{\text{HS1}}$	$\overline{\text{HEAD SELECT 1}}$	O	$\overline{\text{HS1}}$ is one of three (or four) Head Select signals decoded by the drive to select one of eight (or 16) R/W heads.
19	20	$\overline{\text{INDEX}}$	$\overline{\text{INDEX PULSE}}$	I	This signal indicates the start of a track. It is used as a synchronization point during formatting and as a time out mechanism for retries. This signal pulses once for each revolution of the disk.

TABLE 3-2. DRIVE CONTROL CONNECTOR (J1) PIN DESCRIPTION (CONT'D.)

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
21	22	$\overline{\text{DRDY}}$	$\overline{\text{DRIVE READY}}$	I	The drive asserts this signal when the motor is up to speed. No Read or Write commands can be performed if this signal is not asserted.
23	24	$\overline{\text{STEP}}$	$\overline{\text{STEP PULSE}}$	O	$\overline{\text{STEP}}$, along with $\overline{\text{DIRIN}}$, positions the heads to the desired cylinder. $\overline{\text{STEP}}$ pulses the stepping motor at the rate specified by the SP bits in the Command Block and is controlled by the WD1015. $\overline{\text{DIRIN}}$ specifies the direction.
25	26	$\overline{\text{DSEL 0}}$	$\overline{\text{DRIVE SELECT 0}}$	O	$\overline{\text{DSEL 0}}$ is the decoded output of the SDH Register within the WD1010A-05, latched and sent to the drive by the WD1015 to select drive 0.
27	28	$\overline{\text{DSEL 1}}$	$\overline{\text{DRIVE SELECT 1}}$	O	$\overline{\text{DSEL 1}}$ is the decoded output of the SDH Register within the WD1010A-05, latched and sent to the drive by the WD1015 to select drive 1.
29 thru 32			Not Connected		
33	34	$\overline{\text{DIRIN}}$	$\overline{\text{DIRECTION IN}}$	O	$\overline{\text{DIRIN}}$ determines the direction the R/W heads take when stepped. Asserted = in, de-asserted = out.

3.4 DRIVE DATA CONNECTOR

The data is differential in nature and must be connected to each drive with its own cable, drive 0 to J2 and drive 1 to J3. It should be a flat ribbon cable, or twisted pair, less than 3 meters (10 feet) in length. The connector is a 20 pin vertical header on 0.25 centimeter (0.1 inch) center. Table 3-3 describes the drive data connectors (J2 and J3) pin assignments and functions.

TABLE 3-3. DRIVE DATA CONNECTORS – J2, J3

SIG. GND.	SIG. PIN	I/O	SIGNAL NAME
	1		NC
2			GND
	3		NC
4			GND
	5		NC
6			GND
	7		NC
8			GND
	9		NC
	10		NC
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	- MFM Write Data
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	- MFM Read Data
19			GND
20			GND

SECTION IV
INTERFACE TIMING

4.1 TIMING

Timing diagrams are shown in Figures 4-1 through 4-4 and their values are listed in Tables 4-1 through 4-4 respectively. Since the Controller I/O ports can be accessed by either the Host system DMA Controller or the Host processor, timing is given for both cases. The processor executes I/O and memory reads from the ports and the on-board BIOS ROM, and writes to the ports. DMA is used for data transfers between the data I/O port and the Host RAM.

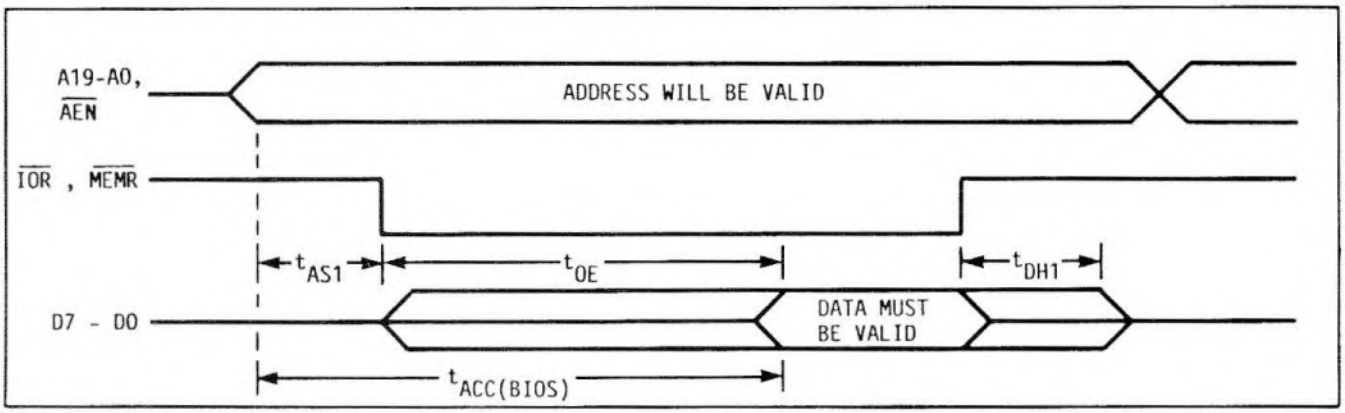


FIGURE 4-1 HOST I/O OR BIOS READ TIMING

TABLE 4-1 HOST I/O OR BIOS READ TIMING

SYMBOL	CHARACTERISTIC	MIN.	MAX.
t_{AS1}	Address Setup Time	50	
t_{ACC}	Address Access Time (BIOS)		250
t_{OE}	Output Enable Time		175
t_{DH1}	Data Hold Time	0	

NOTE: All units in Table 4-1 are in nsec.

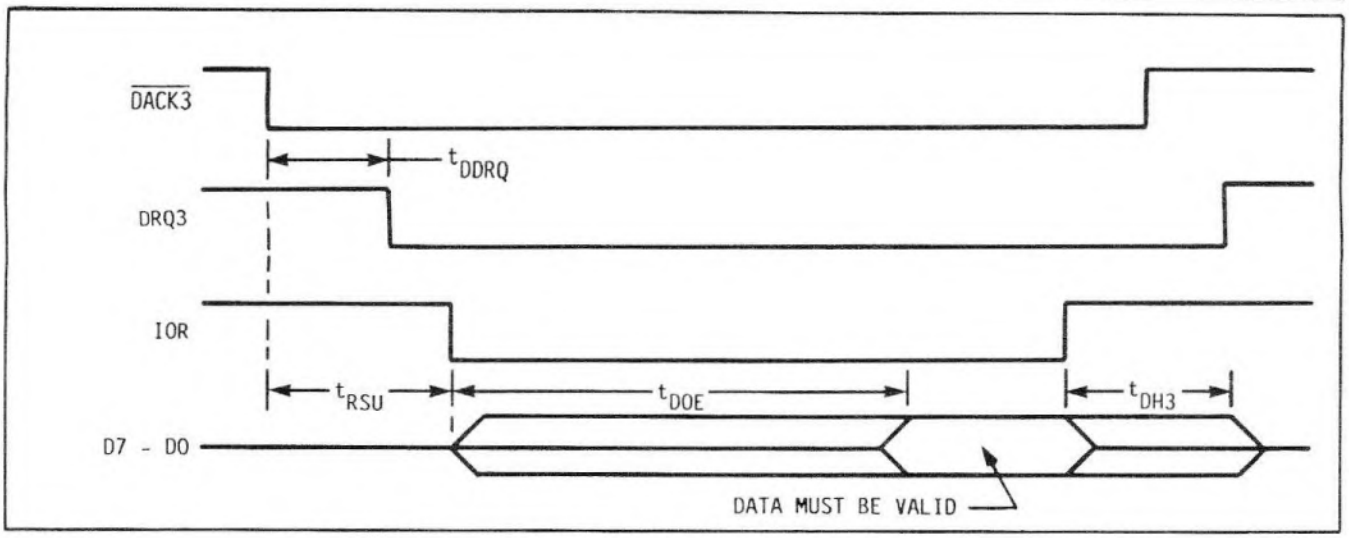


FIGURE 4-2 DMA I/O READ TIMING

Table 4-2 DMA I/O READ TIMING

SYMBOL	CHARACTERISTIC	MIN.	MAX.
t_{DDRQ}	DRQ3 De-assert Delay	20	45
t_{RSU}	Read Setup Time	7	
t_{DOE}	Data Output Enable		175
t_{DH3}	Data Hold Time	0	

NOTE: All units in Table 4-2 are in nsec.

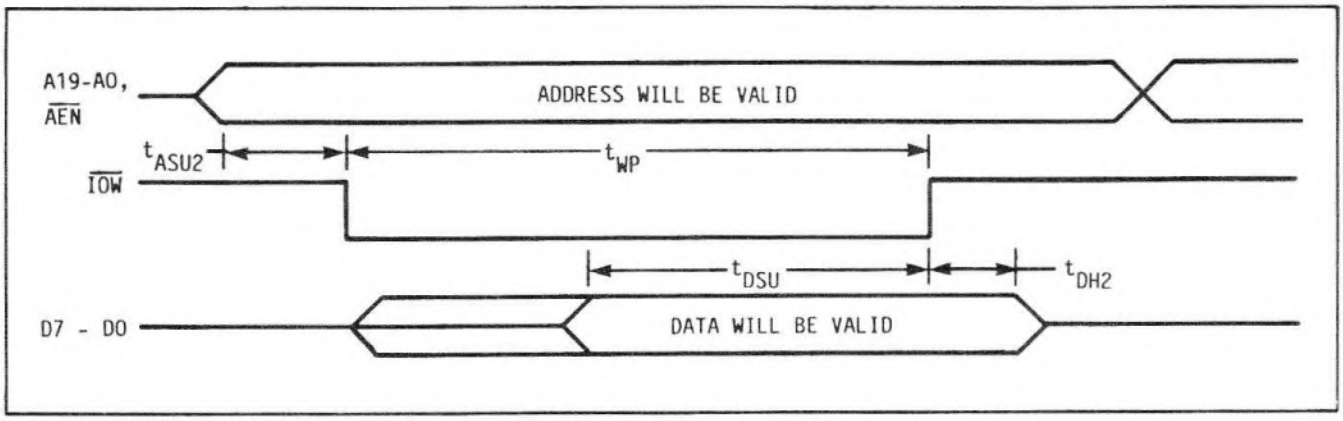


FIGURE 4-3 HOST I/O WRITE TIMING

TABLE 4-3 HOST I/O WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN.
t_{ASU2}	Address Setup Time	50
t_{WP}	Write Pulse Time (I/O)	100
t_{DSU}	Data Setup Time	50
t_{DH2}	Data Hold Time	0

NOTE: All units in Table 4-3 are in nsec.

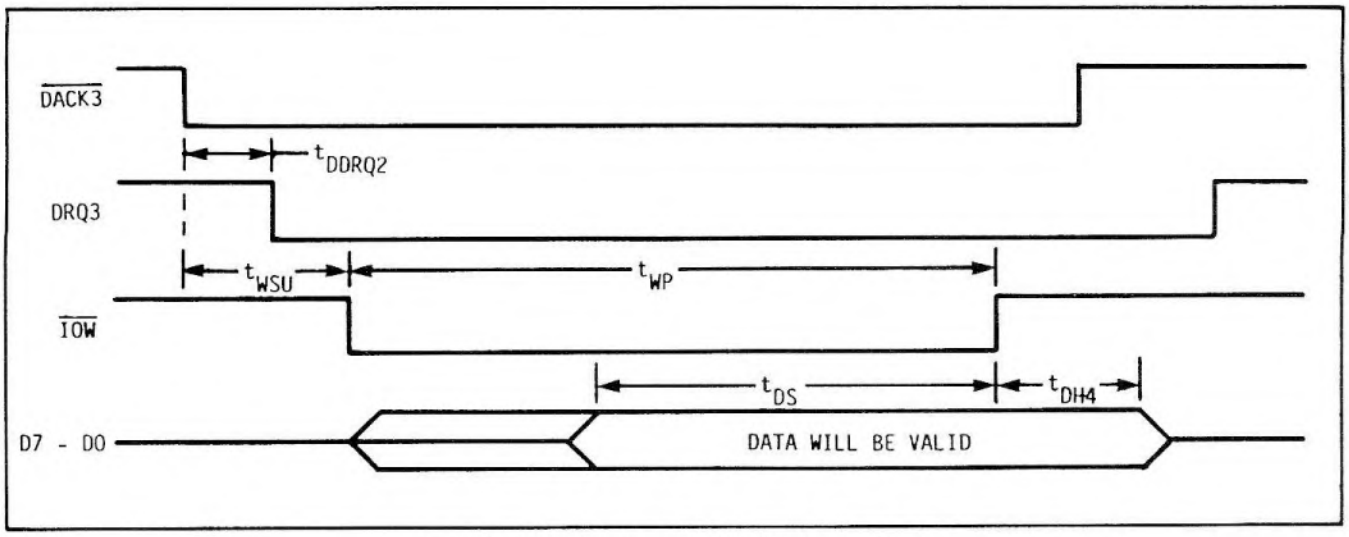


FIGURE 4-4 DMA I/O WRITE TIMING

TABLE 4-4 DMA I/O WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN.	MAX.
t_{DDRQ}	DRQ3 De-assert Delay	20	45
t_{WSU}	Write Setup Time	7	
t_{WP}	Write Pulse Width	100	
t_{DS}	Data Setup Time	50	
t_{DH4}	Data Hold Time	0	

NOTE: All units in Table 4-4 are in nsec.

SECTION V
COMMAND DESCRIPTION

5.1 GENERAL

This section provides a detailed description of the Command Block format and function of the 19 commands supported by the WD1002S-WX2. Fourteen of the commands are operational and five are diagnostic. An explanation of how the commands perform their function is discussed in Section 6 Theory of Operation. Table 5-1 lists a summary of the commands.

TABLE 5-1. COMMAND SUMMARY

COMMAND	PARAMETERS (Refer to Figure 5-1)								
	OP CODE	DRV	HD	CYL	SEC	BLK/INT	R1	R2	STEP
TEST DRIVE READY	00	V	n	n	n	n	n	n	n
RECALIBRATE	01	V	n	n	n	n	V	n	n
READ STATUS OF LAST OPERATION	03	V	n	n	n	n	n	n	n
FORMAT DRIVE	04	V	V	V	DR	V (INT)	V	n	V
VERIFY SECTORS	05	V	V	V	V	V (BLK)	V	V	V
FORMAT TRACK	06	V	V	V	DR	V (INT)	V	n	V
FORMAT BAD TRACK	07	V	V	V	DR	V (INT)	V	n	V
READ SECTORS	08	V	V	V	V	V (BLK)	V	V	V
WRITE SECTORS	0A	V	V	V	V	V (BLK)	V	n	V
SEEK	0B	V	V	V	DR	n	V	n	V
INITIALIZE DRIVE PARAMETERS	0C	V	n	n	n	n	n	n	n
READ ECC BURST ERROR LENGTH	0D	V	n	n	n	n	n	n	n
READ SECTOR BUFFER	0E	n	n	n	n	n	n	n	n
WRITE SECTOR BUFFER	0F	n	n	n	n	n	n	n	n
EXECUTE SECTOR BUFFER DIAGNOSTIC	E0	n	n	n	n	n	n	n	n
EXECUTE DRIVE DIAGNOSTIC	E3	V	n	n	n	n	V	n	V
EXECUTE CONTROLLER DIAGNOSTIC	E4	n	n	n	n	n	n	n	n
READ LONG	E5	V	V	V	V	V (BLK)	V	n	V
WRITE LONG	E6	V	V	V	V	V (BLK)	V	n	V

LEGEND:

V	Must be a valid parameter.
DR	Not used but must be within a valid parameter range.
n	Not used (should be 0 for future compatibility).
INT	Interleave
BLK	Block Count

5.2 I/O PORT DESCRIPTION

There are four contiguous I/O ports addressed 320 hexidecimal through 323 hexidecimal. Each port is bi-directional. The functions of the I/O ports are listed in Table 5-2. These ports are used for all communication between the Host and Controller.

TABLE 5-2. I/O PORT DESCRIPTIONS

ADDRESS	READ PORT FUNCTION	WRITE PORT FUNCTION
320	READ DATA	WRITE DATA
321	READ WD1002S-WX2 HRDWR STATUS	WD1002S-WX2 RESET*
322	READ DRIVE CONFIGURATION INFO	WD1002S-WX2 SELECT
323	Not Used	WRITE DMA AND INTERRUPT MASK REGISTER

***NOTE**

The WD1015-14 automatically executes self-tests after either a Reset command or upon power-up. The WD1015-24 **DOES NOT** automatically execute self-test after either a Reset command or upon power-up. A WD BIOS performs an Execute Controller Diagnostic command as part of the install sequence after power-up regardless of the version of WD1015 on-board. If the Host software interrogates WD1015-24 after a Reset; the WD1015-24 returns good status. The Host must issue an Execute Controller Diagnostic command to perform the WD1015-24 self-test.

5.2.1 PORT 320

This is a bi-directional path over which data, commands, parameters, and status are passed.

5.2.2 PORT 321

The Host reads this port to interrogate the hardware status. This status byte can be read at any time, including command exeuction. The status bits are identified in Table 5-3.

TABLE 5-3. HARDWARE STATUS

BIT							
7	6	5	4	3	2	1	0
d	d	IRQ	DRQ	BSY	C/D	I/O	REQ

d — Not used.

IRQ — Interrupt Request. Assertion (set to 1) signifies that an interrupt is pending.

DRQ — DMA request bit. Assertion (set to 1) signals the Host that the WD1002S-WX2 is ready for a DMA transfer to take place. The direction of the transfer is defined by the I/O bit.

BSY — Busy bit. Assertion (set to 1) signals the Host that the WD1002S-WX2 is busy executing a command and is unable to accept another command.

C/D — Control/Data. Tells the Host which type of transfer the WD1002S-WX2 is expecting. 0 = a command or status byte, 1 = data.

I/O — Input/Output. Identifies the direction of transfers between the Host and WD1002S-WX2. The terms input and output are relative to the Host. 1 = input, 0 = output.

REQ — Request bit. A handshake signal for data transfers between the Host and WD1002S-WX2. The WD1002S-WX2 asserts (sets to 1) this bit when it is ready for data to be transferred between it and the Host. **REQ must be valid for every byte transferred to the Host.**

The Host writes to this port to generate a MR (Master Reset) on the WD1002S-WX2. When writing to this port, the data byte is ignored.

Resetting a WD1002S-WX2 with a WD1015-14 causes automatic execution of a self-test. Automatic execution of self-test does not occur with the WD1015-24. If the Host software interrogates WD1015-24 after a Reset; the WD1015-24 returns good status. The Host must issue an execute Controller Diagnostic command to perform the WD1015-24 self-test.

5.2.3 PORT 322

Reading Port 322 returns a 4-bit drive configuration code in bits 0 through 3. The two least significant bits correspond to drive 1, the two most significant bits to drive 0. The configuration of these bits is established with jumpers on the controller at SW1. Western Digital sets the configuration jumpers to one. Section 7 shows how to set them up for a specific drive.

The two bits associated with each drive is capable of addressing one of four different configuration tables. Both drives can address the same or different tables. The table required by the drive is determined by its formatted capacity. Table 0 = 5MB, 1 = 24MB, 2 = 15MB, 3 = 10MB (default table) with 62-000042-01 and 62-000042-11 WD BIOS. Table 0 = 20MB, Table 1 = 10MB, Table 2 = 20MB, Table 3 = 10MB (default table) with 62-000042-12 WD BIOS.

The parameters established by these tables are:

- Number of Cylinders
- Number of Heads
- The Starting Cylinder for RWC (Reduced Write Current).
- The Starting Cylinder for Write Precomp
- Maximum Correctable Error Burst Length
- Retries Allowed, Stable or Immediate ECC Correction, Step Rate.

Writing to port 322 selects the WD1002S-WX2, sets the Busy bit in the Status Register and prepares it to receive a command. When writing to port 322, the data byte is ignored.

5.2.4 PORT 323

Reading this port has no function.

Writing to this port controls the enabling of the interrupt and DMA request signals to the Host. The bits in this port are defined as follows:

BIT							
7	6	5	4	3	2	1	0
d	d	d	d	d	d	IRQEN	DRQEN

IRQEN Interrupt Request Enable. When asserted (set to one), enables interrupts to the Host.

DRQEN DMA Request Enable. When asserted (set to one), enables DMA requests to the Host.

d Not used.

5.3 COMMAND BLOCK

The Host first selects the WD1002S-WX2 by asserting $\overline{I/OW}$ while at the same time addressing port 322 with the A0 through A19 address bus. The WD1002S-WX2 then asserts the BSY (BUSY) bit in the Status Register. The Host by asserting $\overline{I/OR}$ and addressing port 321 reads the status, finding REQ asserted transmits the first byte of the six byte Command Block to the WD1015. REQ is de-asserted for the second byte of the Command Block transfer. Assertion and de-assertion of REQ must occur for each byte transferred. Figure 5-1 defines the bytes within the Command Block, Table 5-1 is a summary of the commands, Section 6 Theory of Operation explains the hand shake between the Host and WD1002S-WX2 while loading the Command Block in the WD1015.

	BITS							
BYTE	7	6	5	4	3	2	1	0
0	OP CODE							
1	0	0	D	HEAD NUMBER				
2	CYLINDER NUMBER MSB			SECTOR NUMBER				
3	CYLINDER NUMBER LSB							
4	BLOCK COUNT OR INTERLEAVE							
5	R1	R2	0	0	0	SP	SP	SP

FIGURE 5-1. COMMAND BLOCK DESCRIPTION

OP Code: Operation Code identifies the type and function of the command. Bits 7, 6, and 5 designate whether the command is operational (0) or diagnostic (E). Bits 4 through 0 select the function of the command, i.e. Read, Write, etc.

NOTE
The WD1015-24 firmware ignores bit four of byte 0 (op code).

D Drive number, selects one of two drives zero or one.

Head Number Designates the head to be used on the selected drive. 0 through 15. Selection of heads eight through 15 requires WD1015-24.

Cylinder Number MSB and LSB	Designates the cylinder containing the sector(s) to be used by the command. 0 through 1024.
Sector Number	Specifies the starting sector used by the command.
Block Count or Interleave	Block count specifies the number of sectors to be used by a Read, Write, Read Long, or Write Long command. A block count of zero equals 256 sectors. Interleave is used by the Format commands. The maximum interleave is equal to the sectors-per-track minus one. (See Section 5.7.2 for an explanation of interleaving.)
R1	General disk error retry disable bit. R1 controls the retry for all errors except a Data ECC error. With R1 asserted the WD1002S-WX2 makes no attempt to retry an error operation. Instead it aborts the command and sets the appropriate status in the Status Register. Because the disk is soft sectored an ID field error may cause the WD1002S-WX2 to retry for two disk revolutions. With R1 de-asserted, the WD 1002S-WX2 retries the operation for ten disk revolutions before aborting the command and setting the status bit. In the case of an ID Not Found Error the WD1002S-WX2 does a restore to track zero and seeks back to the desired track after the first ten disk revolutions and retries for ten disk revolutions before aborting and setting the error status.
R2	ECC Error retry bit. With R2 = 1 an attempt is made to correct the error on the first syndrome. R2 = 0 there must be two consecutive like syndromes before an attempt is made to correct the error.
SP	The Step Code is used to select the rate at which step pulses are issued to the drive. Table 5-4 defines the rates corresponding to each step pulse code.

TABLE 5-4. STEPPING RATE CODES

BITS			STEPPING RATES	
2	1	0	WD1015-14	WD1015-24
0	0	0	3 msec. per step*	3 msec. per step*
0	0	1	3 msec. per step	45µsec. per step
0	1	0	3 msec. per step	60µsec. per step
0	1	1	3 msec. per step	18µsec. per step
1	0	0	200µsec. per step	210µsec. per step
1	0	1	70µsec. per step	75µsec. per step
1	1	0	3 msec. per step	30µsec. per step
1	1	1	3 msec. per step	18µsec. per step

*This is the preferred 3 msec. step code.

5.4 TEST DRIVE READY
(CLASS 0, OP CODE 00)

This command selects the drive specified by the DRV bit in the Command Block and interrogates the $\overline{DRDY}$, $\overline{WF}$, and $\overline{SC}$ signals returned by that drive. If $\overline{WF}$ and $\overline{SC}$ are de-asserted and $\overline{DRDY}$ asserted, the command returns an error code of 00 No Error Detected.

5.4.1 POSSIBLE ERROR CODES

03 Write Fault
04 Drive Not Ready
08 Drive Still Seeking

5.5 RECALIBRATE
(CLASS 0, OP CODE 01)

This command moves the Read/Write heads to track 0. The $\overline{SC}$ signal from the drive controls the stepping rate of this command. Therefore, this command is slower than commands that implement the implied seek and make use of the stepping rate designated by the SP bits in the Command Block.

NOTE
Timeout on each step during a Recalibrate command is 1 second with a WD1015-14. Timeout on each step during a Recalibrate is 3.5 seconds with a WD1015-24. The 3.5 second timeout supports removable Winchesters.

5.5.1 POSSIBLE ERROR CODES

03 Write Fault
04 Drive Not Ready
06 Track Zero Not Found

5.6 READ STATUS OF LAST OPERATION
(CLASS 0, OP CODE 03)

Upon termination of a command the WD1002S-WX2 develops a Command Completion Byte, de-asserts the BSY bit, and if IRQEN had been enabled, asserts IRQ5. If IRQEN had not been asserted, it is the responsibility of the Host to read port 321 to determine that the WD1002S-WX2 is no longer busy. Once the Host determines that a command has terminated, it must read the Command Completion Byte to learn which drive has terminated and whether an error had occurred. To do this the Host reads port 320. The format of the Command Completion Byte is as follows:

BIT							
7	6	5	4	3	2	1	0
0	0	D	0	0	0	E	0

D = Number of the drive terminating. 0 = drive 0. 1 = drive 1. E = 1 if an error occurred.

If the Command Completion Byte indicates the occurrence of an error, issue a Read Status command for the drive indicating the error. Performance of a Read Status command before any other command execution prevents loss of the error status. When a Read Status of the last operation is written to port 320 the WD1002S-WX2 responds with four bytes of status as shown in Figure 5-2.

	BITS							
BYTE	7	6	5	4	3	2	1	0
0	AV	0	ERROR CODE					
1	0	0	D	HEAD NUMBER				
2	CYLINDER NUMBER MSB			SECTOR NUMBER				
3	CYLINDER NUMBER LSB							

AV Address valid bit. Indicates that the Head, Cylinder, and Sector fields are valid.

Error Codes are shown in Table 5-5.

All other bits are the same as those defined in the Command Block definitions.

FIGURE 5-2. FOUR STATUS BYTES

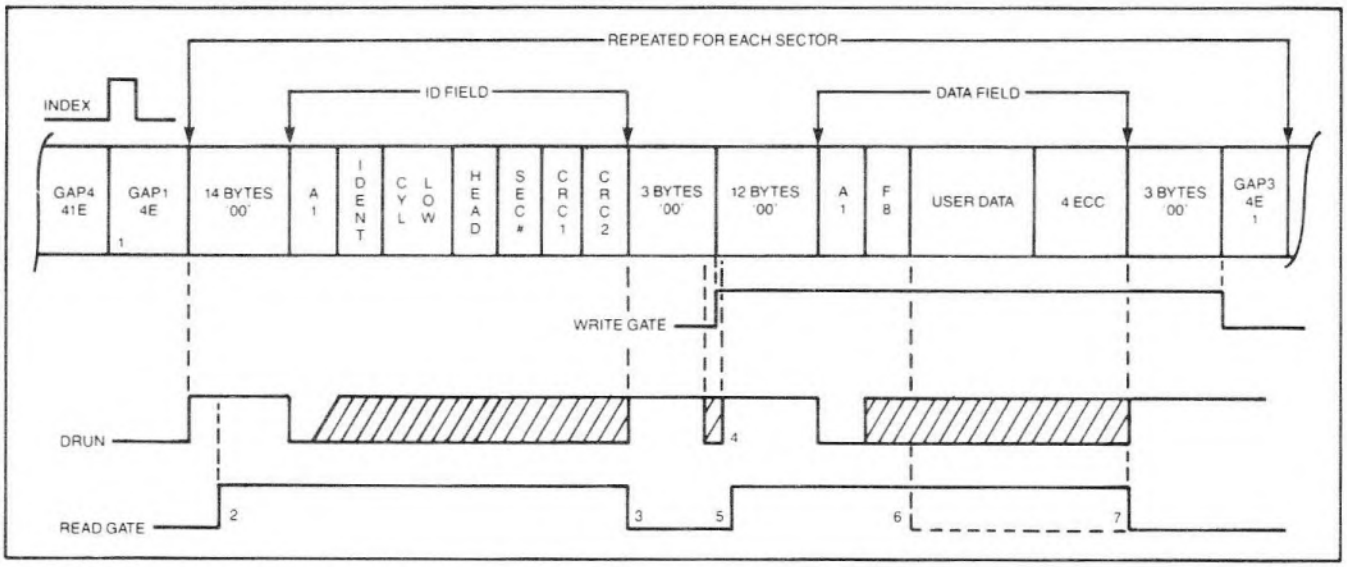
When an error occurs during a multiple sector data transfer (read or write), this command returns the address of the failing sector. If the Read Status command is issued after any of the format commands or the Verify Desired Sectors command, the address returned by the WD1002S-WX2 points one sector beyond the last track formatted or checked, if there was no error. If there was an error, then the address returned points to the track in error.

TABLE 5-5. CONTROLLER RETURNED ERROR CODES

HEX CODE	DEFINITION
00	No error detected.
02	No $\overline{SC}$ signal from the drive. The WD1002S-WX2 has not received a $\overline{SC}$ from the drive within one second (3.5 seconds with WD1015-24) following the last step pulse of a non-buffered seek operation.
03	Write Fault signal received from the drive. This error is reported when the WD1002S-WX2 detects $\overline{WF}$ asserted by a drive either at the completion of a Sector Data Transfer or after initially selecting a drive and the drive indicates ready.
04	Drive Not Ready. The WD1002S-WX2 reports this error when $\overline{DRDY}$ is not received from the drive at the time selection is attempted, or is de-asserted after the drive has been selected.
06	Track 0 Not Found. This error is reported during a Recalibrate command if $\overline{TK000}$ is not received from the drive before stepping the Read/Write Heads 1024 steps.
08	Drive Still Seeking. This status is returned in response to a Test Drive Ready command when a drive performing a buffered seek has not yet asserted $\overline{SC}$.
11	Uncorrectable Data Error. The ECC logic detected an error burst greater than its correction capabilities. The data in the Sector Buffer is not sent to the Host.
12	Data Address Mark Not Found. The proper Sector ID was read by the drive but failed to detect the Data Address Mark.
15	Seek Error. The desired Sector ID field could not be found on the selected track, or a CRC error occurred on the ID field.
18	Correctable Data Error. An error occurred in the data field that was within the tolerance of the ECC logic and was corrected. The data in the Sector Buffer is transmitted to the Host. This status is set as a warning to the Host that a marginal condition may exist.
19	Track Is Flagged Bad. A sector had been encountered that has the Bad Block Mark set in the ID Field. The Format Bad Track command records this bit in all sectors of the designated flagging them all as bad. No retries are attempted in response to this error.
20	Invalid Command. The WD1002S-WX2 has received a command with an invalid class or op code, Interleave Factor.
21	Illegal Sector Address. This error is asserted when a command attempts to address a sector beyond the capacity of the drive. This could be at the time the command is issued, or in the case of a multiple sector transfer, after the last available sector has been used.
30	Sector Buffer Error. An error occurred while performing Sector Buffer Diagnostics (Command Code E0 and E4). A disk drive is not involved in this test.
31	Controller ROM checksum Error. A ROM checksum error was detected during the Controller Diagnostic command (E4).
32	ECC Polynomial Error. During the Controller Diagnostic command (E4), the hardware ECC generator (WD11C00-17) failed its test.

5.7 FORMAT DRIVE STARTING AT DESIRED TRACK (CLASS 0, OP CODE 04)

The WD1002S-WX2 first positions the Read/Write heads to track zero. Then using the parameters specified in the Command Block, positions the heads to the desired track. Formatting always starts with the first sector of the track, regardless of the value of SEC. Even so, SEC must be within the allowable limits. A sample of what is recorded in each sector is shown in Figure 5-3. The data recorded in the Data Field is defaulted to whatever is in the Sector Buffer at the time. The logical sector numbering is specified by the interleave value (INT) included in the Command Block. If a hard error occurs while formatting a track, the WD1002S-WX2 stops the format operation and returns an error code.



ID FIELD

A1	=	A1 hex with 0A hex clock
IDENT	=	Bits 1, 0 = Cylinder High FE = 0-255 Cylinders FF = 256-511 Cylinders FC = 512-767 Cylinders FD = 768-1023 Cylinders
HEAD	=	Bits 0, 1, 2 = Head Number Bits 3, 4 = 0 0 Bits 5, 6 = Sector Size (10) Bit 7 = Bad Block Mark
Sec #	=	Logical Sector Number

DATA FIELD

A1	=	A1 hex with 0A hex clock
F8	=	Data Address Mark; Normal Clock
USER	=	Data Field 512 Bytes

NOTES:

1. GAP 1 and 3 length equals 22 bytes.
2. The decision to assert RG is made 2 bytes after the start of DRUN.
3. RG de-asserted:
   - If DRUN does not last until A1
   - When any part of ID does not match the one expected.
   - After CRC if correct ID has been read.
4. Write splice recorded on disk by asserting WG.
5. RG is suppressed until after write splice.
6. Not a proper A1 or F8, set DAM error.
7. Sector size as stated in ID field, plus four for ECC.

FIGURE 5-3. FORMAT

5.7.1 POSSIBLE ERROR CODES

02 No Seek Complete 03 Write Fault
04 Disk Not Ready 06 Track Zero Not Found
20 Invalid Command 21 Illegal Sector Address

5.7.2 INTERLEAVING

When physically sequential sectors on the disk are to be read, each sector reaches the read/write head before a read or write operation can be set up. The disk must then make a complete rotation to pick up the next sector. When an attempt is made to read all 17 sectors on a particular track, 17 rotations or approximately one fourth of a second per 8K bytes are required. This performance can be significantly improved by interleaving, a technique that allows the system to read or write more than one sector per rotation.

For a system requiring less than two sector times to process the data it has read and to set up for the next read operation, the second logical sector is physically placed three sectors away from the first. The controller can now read the second sector with minimal delay. This three-to-one interleave factor allows a potential reading of the entire track in less than three rotations. In the example given, the throughput is increased by a factor of 5.6.

The simplest way to determine the optimum interleave for any particular system is through experimentation. If the system maintains its directories or virtual memory-swapping areas in a certain place on the disk, it sometimes makes sense to have more than one interleave.

To simplify driver software, the WD1002S-WX2 automatically writes the logical sector number of each sector in its ID field. Figure 5-4 is an example of an interleave table for a 17-sector track with 3:1 interleave. The WD1002S-WX2 accepts any interleave value between zero and one less than the number of sectors per track. An interleave of zero is automatically converted to one, and a value out of range results in an error code 20, Invalid Command Error.

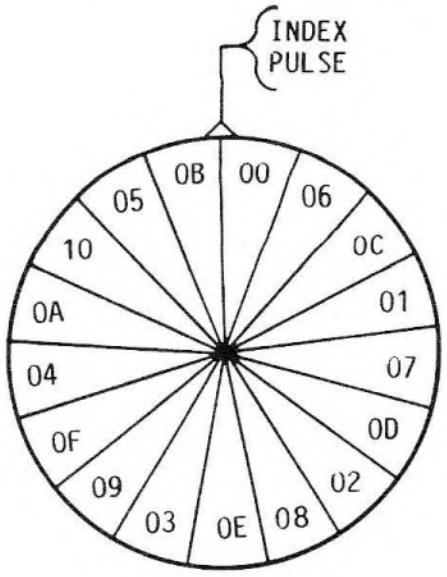


FIGURE 5-4.
17 SECTORS WITH A 3:1 INTERLEAVE

5.8 VERIFY SECTORS (CLASS 0, OP CODE 05)

This command reads from 1 to 256 sectors, as specified by BLK in the Command Block, beginning at the sector specified by HD CYL and SEC. If an error occurs during a multiple sector read, the heads remain positioned at the track containing the error. The Host then issues a Read Status of Last Disk Operation command to determine the error code. To continue the operation, the Host calculates the difference between the number of sectors desired and the number of sectors completed and issues another Seek command to access the remaining sectors.

5.8.1 POSSIBLE ERROR CODES

02 No Seek Complete 03 Write Fault
04 Drive Not Ready 06 Track Zero Not Found
12 Data Address Mark Not Found 15 Seek Error
21 Illegal Disk Address
19 Track Flagged Bad

5.9 FORMAT TRACK (CLASS 0, OP CODE 06)

This command is identical to the Format Drive command, except that only the track specified by the command is formatted. This command can be used to clear the Bad Track Flag, or reformat individual tracks.

5.10 FORMAT BAD TRACK (CLASS 0, OP CODE 07)

This command is the same as the Format Track command, except that the Bad Track Flag is set in the ID field.

5.11 READ SECTORS (CLASS 0, OP CODE 08)

This command reads from 1 to 256 sectors as specified by BLK in the Command Block, beginning at the sector defined by CYL SEC and Head. An uncorrectable error during a multiple sector read causes the operation to terminate at the error sector. The Host then issues a Read Status of Last Disk Operation command to determine the type of error. To continue the operation, the Host calculates the difference between the number of sectors desired and the number of sectors completed, then issues another Read command to access the remaining sectors. Error code 06 can only be asserted if the R1 bit = 0 and the ID Field has not been read for 10 disk revolutions. This causes the WD1002S-WX2 to recalibrate the heads and seek back to the desired track. If track zero is not detected within 1024 steps, Error Code 06 is set. If R1 = 1 the WD1002S-WX2 aborts the command after a maximum of two disk revolutions, therefore no attempt is made to position the heads to track zero.

5.11.1 POSSIBLE ERROR CODES

02	No Seek Complete	03	Write Fault
04	Drive Not Ready	06	Track Zero Not Found
11	Uncorrectable ECC Error	12	Data Address Mark Not Found
15	Seek Error	18	Correctable ECC Error
19	Track Flagged Bad	21	Illegal Sector Address

5.12 WRITE SECTORS (CLASS 0, OP CODE 0A)

This command writes from 1 to 256 sectors as specified by BLK in the Command Block. The multiple sector transfer scheme works the same as the Read command. Error code 06 can only be asserted if the R1 bit is 0 and the ID Field has not been read for 10 disk revolutions. This causes the WD1002S-WX2 to recalibrate the heads and seek back to the desired track. If track zero is not detected within 1024 steps, Error Code 06 is set. If R1 is 1 the WD1002S-WX2 aborts the command on the first failure to read an ID Field, therefore no attempt to position the heads to track zero is made.

5.12.1 POSSIBLE ERROR CODES

02	No Seek Complete	03	Write Fault
04	Drive Not Ready	06	Track Zero Not Found
12	Data Address Mark Not Found	15	Seek Error
19	Track Flagged Bad	21	Illegal Disk Address

5.13 SEEK (CLASS 0, OP CODE 0B)

This command selects the head and initiates a seek to the track specified by HD and CYL in the Command Block. The $\overline{SC}$ signal line is not sampled to allow buffered seeks. The cylinder must be in range. The drive must be formatted. Drives employing buffered steps can be issued step pulses at a high speed freeing the WD1002S-WX2 for other operations. The WD1002S-WX2 does not wait for the drive to complete the seek to return a Command Completion Status. If the return status shows no error, the seek was issued correctly. If there is an error, the seek was not issued. After transferring the status, another command can be issued to either drive. If the WD1002S-WX2 receives a command other than Test Drive Ready for a drive that is still seeking, it asserts BSY and waits for $\overline{SC}$ to be asserted before executing the command. If the command is a Test Drive Ready, it executes and returns an 08 Drive Still Seeking Error. The time-out for non-buffered seeks. For buffered seeks, the WD1015 checks $\overline{SC}$ before a Read or Write (next command).

The rate at which the Step Pulses are issued to the drive is controlled by the SP bits in the Command Block. The drive buffers these pulses and steps at its own rate. This allows the WD1002S-WX2 to continue about its own business, possibly starting the other drive seeking to a new track, without having to wait for the $\overline{SC}$ from the first drive. Refer to Table 5.4 for the available stepping rates.

5.13.1 POSSIBLE ERROR CODES

03	Write Fault	04	Drive Not Ready
15	Seek Error		

5.14 INITIALIZE DRIVE PARAMETERS
(CLASS 0, OP CODE 0C)

The WD1002S-WX2 is capable of controlling two drives with different formatted capacity. The BIOS contains four Winchester parameter tables. The configuration jumpers address the proper Winchester parameter table during the BIOS install cycle at power up. Refer to Section 7 for details on these jumper settings. When the Host reads port 322 and discovers a change in drives, it issues this command, followed by the 8-byte block of drive parameters listed below:

Maximum Number of Cylinders
(2 bytes, 1024 max.)
Maximum Number of Heads
(1 byte, 8 or 16 heads)
Starting Reduced Write Current Cylinder
(2 bytes, 1024 max.)
Starting Write Precompensation Cylinder
(2 bytes, 1024 max.)
Maximum ECC Data Burst Length
(1 byte, 11 max.)

A typical set of parameters for a 10MB drive is as follows:

306 cylinders — 4 heads
RWC at cylinder 153 — Write Precomp at cylinder 153
11-bit burst error length (Western Digital Corp. recommends using a maximum ECC burst length of five or less to ensure optimum integrity of data recovered).

For the exact parameters it is necessary to refer to the specifications for the BIOS in use on the specified board.

5.15 READ ECC BURST ERROR LENGTH
(CLASS 0, OP CODE 0D)

This command is only valid following a correctable ECC error. It transfers one byte indicating the length of the error. The error length is determined by counting the first through last bit in the error.

5.16 READ SECTOR BUFFER
(CLASS 0, OP CODE 0E)

This command transfers the 512 bytes of data currently residing in the Sector Buffer to the Host.

5.17 WRITE SECTOR BUFFER
(CLASS 0, OP CODE 0F)

This command writes 512 bytes of data from the Host into the WD1002S-WX2 Sector Buffer.

5.18 EXECUTE SECTOR BUFFER DIAGNOSTIC
(CLASS E, OP CODE 00)

This command executes a 9-pass test that uses a 9-byte pattern (0, 1, 2, 4, 8, 10, 20, 40, and 80 hex) that is written to the Sector Buffer, then read back. After each successful completion, the whole pattern is shifted one byte position and repeated.

NOTE
The WD Format Drive Utility in the WD BIOS executes this command before physical formatting of the drive. Thus, the data fields are formatted with this 0, 1, 2, 4, 8, 10, 20, 40, and 80 hex pattern.

5.18.1 POSSIBLE ERROR CODES

30 Data error.

5.19 EXECUTE DRIVE DIAGNOSTIC
(CLASS E, OP CODE 03)

This command tests both the drive and the drive-to-WD1002S-WX2 interface. The WD1002S-WX2 sends Recalibrate and Seek commands to the selected drive and reads sector zero of each track verifying both ID and data fields. The WD1002S-WX2 does not perform any write operations.

5.19.1 POSSIBLE ERROR CODES

02 No Seek Complete
03 Write Fault
04 Drive Not Ready
06 Track Zero Not Found
12 Data Address Mark Not Found
15 Seek Error

5.20 EXECUTE CONTROLLER DIAGNOSTICS
(CLASS E, OP CODE 04)

Regardless of the version of the WD1015 on the WD1002S-WX2, the WD1002S-WX2 executes this command when the Host issues a command code of E4 hex to the CCB. The WD1015-14 automatically executes this command after system Reset (RST on connector P1 B2 asserted), write to port 321 hex, or power-up. The WD1015-24 only automatically executes this command when an on-board WD BIOS performs an install sequence after power-up.

Once started, this command continues to run until an error occurs, or the Host selects the WD1002S-WX2 by writing to port 322. If an error occurs when this command has been started at power up, an error code is output at pins 27, 28, and 29 of the WD1015. These are the Head Select 0, 1, and 2 signals and can be monitored at the Drive Control

Connector J1 pins 14, 18, and 4. The error codes generated under this condition are not the same as those reported by a Read Status command.

1 – WD1010A-05 Error
2 – WD11C00-17 ECC Error
3 – Sector Buffer Error
4 – WD1015 RAM Error
5 – WD1015 ROM Error

5.20.1 WD1010A-05 TEST

A pattern is written to and read from the WD1010A-05's Sector Count and Sector Number Registers.

5.20.2 WD11C00-17 ECC TEST

The WD11C00-17 is enabled during the read portion of the Sector Buffer Test. After the contents of the Sector Buffer have been read, the ECC not 0 (pin 20) of the WD11C00-17 is monitored, it should be asserted indicating non-zero Check Bytes. The internal check pattern is then fed back into the chip and pin 20 monitored again. This time it should not be asserted, indicating a Check Byte pattern of zero.

5.20.3 SECTOR BUFFER TEST

The hex pattern 00, 01, 02, 04, 08, 10, 20, 40, 80 is written throughout the entire Sector Buffer and then read to make sure it is correct. The entire contents of the Sector Buffer is then shifted one byte position and read again. This procedure is repeated nine times verifying that every bit in the Sector Buffer can be set and reset.

The WD11C00-17 is enabled during the read functions to verify the operability of that device.

5.20.4 WD1015 RAM TEST

This tests the 100 bytes of internal RAM in the same manner as the Sector Buffer test.

5.20.5 WD1015 ROM TEST

This test verifies the ability to address and read all 2K bytes of internal ROM, using an add and rotate algorithm to generate a single byte result. This result is then compared with the Sumcheck located in the last page of memory.

5.20.6 POSSIBLE ERROR CODES

30 Sector Buffer Error 31 ROM Sumcheck Error
32 ECC Error

5.21 READ LONG (CLASS E, OP CODE 05)

The Host first performs a normal Write command, writing known data, that produces a predictable ECC character; then performs a Readlong command. This command reads the data from the disk without generating any ECC bytes of its own. Instead it reads the four ECC bytes from the disk, as though reading data, resulting in 512 plus 4 for a total of 516 bytes of data. The Host, knowing what the data and ECC bytes are supposed to be, can now determine whether any errors that have occurred, are a result of a data or ECC failure.

5.21.1 POSSIBLE ERROR CODES

02 No Seek Complete 03 Write Fault
04 Drive Not Ready 06 Track Zero Not Found
12 Data Address Mark Not Found 15 Seek Error
21 Illegal Disk Address
19 Track Flagged Bad

5.22 WRITE LONG (CLASS E, OP CODE 06)

After performing the Write normal/Readlong routine to determine that the WD1002S-WX2 is able to write data and generate correct ECC bytes, the Host can execute a Writelong and Read normal routine. This verifies the ability of the WD1002S-WX2 to read the data correctly and generate 4-zero ECC bytes or if an error was forced, correct it. The Writelong command does not generate ECC bytes, instead the Host supplies them along with a known data pattern. Then, performing a normal Read command, the Host can determine whether non-zero ECC bytes are caused by a Read failure or ECC generation failure. (This procedure could be performed prior to the Write normal/Readlong).

5.22.1 POSSIBLE ERROR CODES

02 No Seek Complete 03 Write Fault
04 Drive Not Ready 06 Track Zero Not Found
12 Data Address Mark Not Found 15 Seek Error
21 Illegal Disk Address
19 Track Flagged Bad

SECTION VI
THEORY OF OPERATION

6.1 GENERAL

The WD1002S-WX2 Winchester Controller interfaces an IBM PC or IBM-compatible PC with a maximum of two Seagate Technology ST506-compatible disk drives. Western Digital bases the WD1002S-WX2 architecture on the WD1010A-05 Winchester Disk Controller, WD1015-14 (WD1015-24) Buffer Manager Control Processor, WD11C00-17 Logic Array, WD10C20 Winchester Data Separator and Write Precompensation Device, and BIOS ROM. Therefore, this theory of operation focuses upon these devices. Figure 6-1 is a functional block diagram of the WD1002S-WX2.

6.2 BUSES

This section describes the five buses used by the WD1002S-WX2. Two of the buses are extensions of the Host data and address buses. The other three buses are internal to the WD1002S-WX2. All buses transmit either addresses, commands, data or status information.

6.2.1 HOST INTERFACE ADDRESS BUS A0 THROUGH A19

The Host uses this bus during programmed I/O to address the eight I/O ports 320 hexidecimal through 327 hexidecimal. The Host also addresses the BIOS ROM with address C8000-C8FFF on this bus.

6.2.2 HOST INTERFACE DATA/COMMAND BUS D0 THROUGH D7

This is a bi-directional data bus linking the WD1002S-WX2 to the Host. It is used for the transmittal of data between the Host and Sector Buffer, the Command Control Block (CCB) to the WD1015, and the drive configuration and status to the Host.

6.2.3 WD1002S-WX2 INTRABOARD COMMAND/STATUS BUS BD0 THROUGH BD7

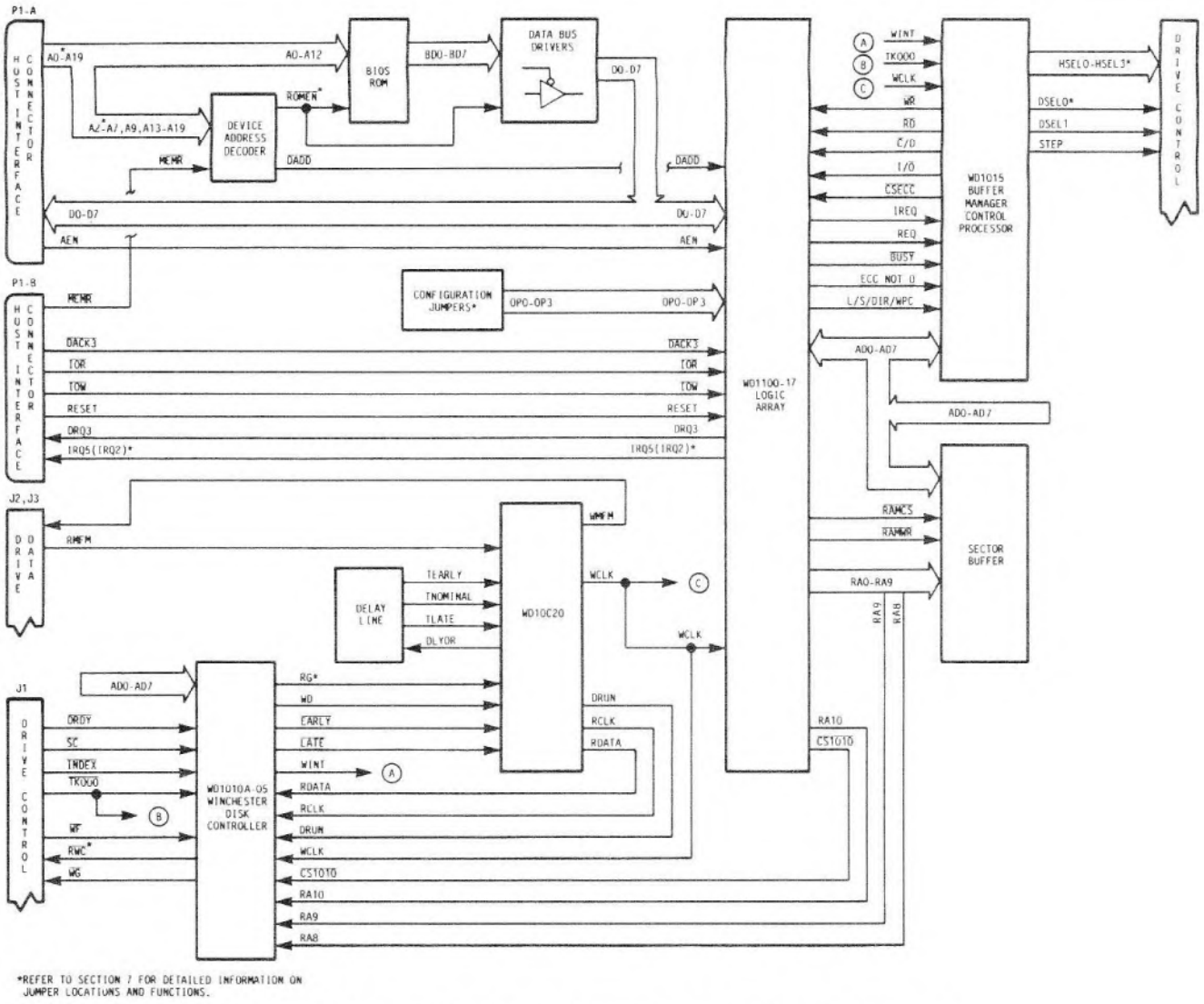
This is a read only bus connecting the BIOS ROM to D0 through D7, through a bus drivers controlled by $\overline{\text{ROMEN}}$. When the Host requests information from the BIOS, the Host addresses the BIOS and enables the bus drivers. The information passes from BD0 - BD7 to D0 - D7. The information transfer between the BIOS and Host follows standard bus protocol.

6.2.4 WD1002S-WX2 INTRABOARD COMMAND/STATUS BUS AD0 THROUGH AD7

This is a bi-directional bus linking the WD1015, WD1010A-05, WD11C00-17, and Sector Buffer. Data, commands, control information and status all pass through this bus. This bus is linked to the D0 through D7 bus by the WD11C00-17.

6.2.5 WD1002S-WX2 INTRABOARD ADDRESS BUS RA0 THROUGH RA10

This bus addresses the Sector Buffer and WD1010A-05 Task File, as well as signaling the WD1010A-05 that the end of the data field has been reached and the ECC is starting. The Task File address is preset into the WD11C00-17 Sector Address Counter which in turn places it on the RA0 through RA10 bus. The Task File address is eight bits long.



*REFER TO SECTION 7 FOR DETAILED INFORMATION ON JUMPER LOCATIONS AND FUNCTIONS.

FIGURE 6-2. WD1002S-WX2 DETAILED BLOCK DIAGRAM

6.3 BUS PROTOCOL

The Host and WD1002S-WX2 protocol consists of the following bus phases:

Select
Command
Data
Completion

Normal execution occurs in the order listed above. Depending upon the type of command being executed, the Data phase does not always occur. Also, depending upon the type of errors detected by the WD1015 or WD1010A-05, an immediate skip to the Completion phase can occur. Execution of the Completion phase always occurs regardless of the command or error.

6.3.1 SELECTION PHASE

The Host selects this phase to start execution of a command by the WD1002S-WX2. The WD11C00-17 asserts $\overline{BUSY}$ to acknowledge selection of the WD1002S-WX2. The Host can sample $\overline{BUSY}$ by reading port 321 hex. For power-up and at the end of every command, the WD1002S-WX2 asserts the hardware status bits required for proper handshake as follows:

$\overline{BUSY}$
$\overline{C}$ ($\overline{C}$/D)
$\overline{I}$ ($\overline{I}$/O)
REQ

When the Host reads the WD1002S-WX2 hardware status the WD11C00-17 complements $\overline{BUSY}$ and $\overline{C}$/D and drives these signals onto the Host data bus. Sections 5.2.1 through 5.2.4 describe the I/O ports in detail.

6.3.2 COMMAND PHASE

Following the Selection phase, the Host sends the six byte Command Control Block (CCB). Transfer of the require assertion of the hardware status bits, $\overline{BUSY}$, $\overline{C}$ ($\overline{C}$/D), $\overline{I}$ ($\overline{I}$/O), and REQ. The WD11C00-17 sends the CCB to page 0 of the Sector Buffer. The WD1015 retrieves the CCB from the Sector Buffer to execute the command. Once this phase is entered, the only way the Host can abort command execution is by asserting RESET. The Host can reissue commands when the WD1002S-WX2 de-asserts $\overline{BUSY}$. Section 5.3 describes the CCB format.

6.3.3 DATA PHASE

After decoding a command and checking for any illegal parameters, the WD1015 sets up the Host for the Data phase depending upon whether the WD1015 needs the data first to execute the command. Otherwise, the Data phase is entered, after the command is executed by the WD1015, as in the case of a Read Command. Assertion of D ($\overline{C}$/D) defines the Data phase. The state of the I/$\overline{O}$ signal and the command determines the direction of the data transfer. Assertion of I (I/$\overline{O}$) indicates data input to the Host. Assertion of $\overline{O}$ (I/$\overline{O}$) indicates data output from the Host.

6.3.3.1 Programmed I/O Data Transfer

The Host usually transfers commands and data in programmed I/O mode except disk data transfers. Disk data transfers can be either programmed I/O or DMA. To the WD1002S-WX2, both methods of data transfer are identical except for the generation of the handshake signals by the WD11C00-17. The WD11C00-17 does not generate the $\overline{DRQ3}$ signal in programmed I/O mode. $\overline{IOR}$ and $\overline{IOW}$ transfer the data when the WD1015 asserts the hardware status bits.

The WD1002S-WX2 I/O ports reside in Host memory address locations 320 hex through 323 hex. (The WD1002S-WX2 allows jumper selection of the I/O port addresses. Refer to Section 7 for further information.) All WD1002S-WX2 port accesses are made in programmed I/O mode. Address enable (AEN) indicates Host control over the buses and connects the I/O channel to the WD1002S-WX2. A0 through A9 address the Host memory locations. A0 and A1 select one of the four ports. $\overline{IOR}$ and $\overline{IOW}$ select the port function. Depending upon the addressed port function, the Host bus may not be used. Section 5.2 describes the I/O ports and their functions. Section 4 describes interface timing for programmed I/O data transfers.

6.3.3.2 DMA Data Transfer

The Host must configure the WD1002S-WX2 for DMA mode before transfer data between the Sector Buffer and Host. The Host writes to port 323 hex to enable DMA mode prior to issuing a command. With DMA eanbled, no access of port 320 is required to transfer data. The Host can then sense $\overline{DRQ3}$ at the start of a byte transfer. Assertion of $\overline{DACK3}$ by the Host causes the WD11C00-17 to de-assert $\overline{DRQ3}$. Data transfer between the Sector Buffer and Host is then controlled by the Host using $\overline{IOW}$ and $\overline{IOR}$ signals as in programmed I/O mode. When $\overline{DACK3}$ is de-asserted, $\overline{DRQ3}$ is asserted by the WD11C00-17. This process repeats until all the data is transferred. De-assertion of REQ signals the end of the DMA transfer. Section 4 describes interface timing for DMA data transfers.

6.3.4 COMPLETION PHASE

The Host senses the Completion phase by sampling IRQ5 (IRQ2 is a jumper selectable option. Refer to Section 7.) or by polling the $\overline{BUSY}$ signal. IRQ5 is available as a port 321 status bit. The Host totally controls IRQ5 by writing to port 323. The WD11C00-17 generates IRQ5 when the Host issues the write to port 323. The Host must disable interrupts before reading the Command Completion byte from the WD1002S-WX2. If the Host does not disable the WD1002S-WX2 interrupts, then the WD1002S-WX2 continuously interrupts the Host. The completion code can be read by the Host when the WD11C00-17 asserts the following hardware status signals:

$\overline{BUSY}$
C (C/$\overline{D}$)
I (I/$\overline{O}$)
REQ

A completion code of zero indicates no error occured. A non-zero value indicates occurrence of an error during command execution. The Host can obtain additional information about the error by executing a Read Status Command. In this case, the Data phase is implemented at command completion by the WD1002S-WX2.

The WD1015 makes the command completion byte available to the Host at port 320 after command completion. This byte contains the drive number of the drive that completion status is valid and an error bit. Section 5.6 describes the format of the command completion byte.

6.4 DEVICE ADDRESS DECODER

The Device Address Deocder generates $\overline{ROM\ ENABLE}$ ($\overline{ROMEN}$) and $\overline{DEVICE\ ADDRESS\ CODE}$ ($\overline{DADD}$). $\overline{ROMEN}$ allows the Host to address the BIOS ROM and enables the ROM Data Bus Drivers to place the BIOS ROM information on the Host Interface Data/Command Bus. $\overline{ROMEN}$ is derived from a valid BIOS address and $\overline{MEMR}$. $\overline{DADD}$ is asserted when address 320 or 324 is present on the address bus.

6.5 BIOS ROM

The BIOS ROM contains firmware driver routines for Winchester disk control. These routines, when installed, reside in Host memory space C8000 hex through C8FFF hex. The BIOS routines are only entered via software interrupts. If your Host operating system is designed to supply the BIOS ROM information, then the WD1002S-WX2 BIOS ROM is not required to operate the controller.

6.6 CONFIGURATION JUMPERS

These jumpers configure the WD1002S-WX2 for different disk drive capacities. Pull-up resistors internal to the WD11C00-17 normally tie the OPTION 0 through 3 (OP0 through OP3) signals to +5V. Installation of a jumper connects the signal to ground. Section 7 describes the Configuration Jumper location and settings for disk drive capacities.

6.7 WD11C00-17 LOGIC ARRAY

The WD11C00-17 Logic Array incorporates several functions in a single package. Implementation of these functions occurs by combining random logic and specialized circuits. The WD11C00-17 contains the following circuits:

Status ports
Read and write ports
Sector Buffer RAM addressing and control
ECC
Reset timing

The WD11C00-17 connects directly to the multiplexed address/data bus, AD0 - AD7.

6.7.1 STATUS, READ, AND WRITE PORTS

Section 5.2 describes these ports' functions. Section 6.3 describes the operation of these ports.

6.7.2 SECTOR BUFFER RAM ADDRESSING AND CONTROL

A counter in the WD11C00-17 generates RAM ADDRESS 0 through 9 (RA0 through RA9). The upper three address bits (RA7, RA8, and RA9) are resettable by the WD1015. This allows the WD1015 to address a range of 8 pages with 256 bytes in each page. The address of any byte within a page can be set by the WD1015 by generating dummy RAM accesses to increment the address counters to the proper address.

In addition to addressing the Sector Buffer, the upper three counter bits (RA8, RA9, and RA10) are used to address the WD1010A-05 Task File when the Sector Buffer is not being used. A Sector Buffer access ends when the Sector Buffer is empty or full. Therefore, the WD11C00-17 asserts RA10.

Assertion of RA10 causes de-assertion of DRQ3. This informs the Host that the Sector Buffer is either empty or full, signals the end of the data field, and indicates the start of the ECC field to the WD11C00-17 ECC logic.

Assertion of RA3 when the Command bus phase ends indicates to the WD1015 placement of the CCB in the Sector Buffer.

6.7.3 ECC CIRCUITRY

During a write operation, the WD1010A-05 receives the data from the Sector Buffer. The WD11C00-17 generates and appends the four byte ECC to the data stream. Proper placement of the ECC requires determination of the end of the data stream. Assertion of RA10 by the WD11C00-17 address counter indicates RAM overflow and the end of the data stream. After writing the ECC to the disk, the WD11C00-17 ECC circuitry supplies all zero bytes to the AD0 through AD7 bus as long as ECC function is selected.

During a read operation, the ECC circuitry recomputes the ECC. Comparison of the previously written ECC and computed ECC occurs at the end of the data stream. (Assertion of RA10 indicates end of the data stream.) The ECC circuitry records the result of the comparison. Any additional writes to the Sector Buffer are ignored. If the result of the comparison is non-zero, then the WD11C00-17 asserts ECC NOT 0 signal. Assertion of ECC NOT 0 enables the WD1015 to attempt error correction.

For diagnostic purposes, during Writelong and Readlong commands the ECC generation and checking is disabled. A Writelong command causes the WD11C00-17 to accept any four bytes from the Host, and stores the bytes internally. These bytes are written to the disk unaltered. A Readlong command causes the WD11C00-17 to accept the four bytes written on the disk. These bytes are passed to the Host unaltered. This allows the Host to induce errors anywhere in the data stream and check for predictable results. Sections 5.21 and 5.22 describe these commands.

During sector reads and writes, CRC error detection capability is used for the I.D. fields. The data field on a hard disk uses error correction for a single burst up to 11 bits in error. The bit correction span is user programmable. Use the 11 bit correction span sparingly or only for diagnostic purposes. Eleven bit error correction spans significantly reduce error detection for multiple error bursts. A five bit correction span is adequate for most applications.

6.7.4 RESET TIMING CIRCUITRY

For a reset, the WD1002S-WX2 executes a power-up sequence to setup internal parameters and initializes the on-board circuitry properly. The WD1002S-WX2 design requires a minimum warm reset pulse width of 15µsec. The Reset Timing circuitry provides a warm reset pulse of 1.35 msec. For a cold start, the minimum reset required pulse width is 10 msec. The Reset Timing circuitry provides a cold reset pulse of 128 msec.

To detect any power up diagnostic failures, the Host should issue an Execute Controller Diagnostic command if the WD1002S-WX2 DOES NOT use either a WD1015-14 or a WD BIOS. The WD1015-14 automatically performs an Execute Controller Diagnostic command after power-up or a software reset. A WD BIOS issues an Execute Controller Diagnostic command as part of the install sequence regardless of the version of the WD1015 on-board.

6.8 WD1015 BUFFER MANAGER CONTROL PROCESSOR

The WD1015 is a self contained CPU designed to receive commands from the Host. Firmware in the WD1015 translates the Host command format into the WD1010A-05 format. The WD1015 controls any programmable retries and data error correction.

There are two versions of the WD1015 for the WD1002S-WX2. The WD1015-14 supports up to eight heads. The WD1015-14 uses the $\overline{\text{REDUCED WRITE CURRENT}}$ ($\overline{\text{RWC}}$) signal. The WD1015-24 supports up to 16 heads. The WD1015-24 uses the $\overline{\text{RWC}}$ pin on J1 as $\overline{\text{HEAD SELECT 3}}$ ($\overline{\text{HSEL3}}$). The acronym WD1015 refers to both versions. When a specific reference is made to a specific version, the appropriate acronym is used.

The WD1015 controls the transfer of information within the WD1002S-WX2 and maintains the necessary copies of the WD1010A-05 Task Files. The WD1015 accesses the CCB in the Sector Buffer. Prior to the command being issued to the WD1010A-05 by the WD1015, the drive and head select information is set in a port latch for the drive interface (DSEL0, DSEL1, and HSEL0 through HSEL3). The heads are stepped, if required, by the STEP signal and positioned over the

desired cylinder. The CCB is translated and issued to the WD1010A-05, after observing the required protocol. At the end of command execution, the WD1010A-05 asserts WINT. The WD1015 polls WINT.

The WD1015 controls multiple sector transfers without the Host reissuing the command. The WD1015 breaks all multiple sector transfers into a series of single sector commands to the WD1010A-05. The WD1015 provides head changes and steps as required between WD1010A-05 commands until the block count is satisfied. There can be many WD1010A-05 interrupts (WINT) for one Host command. However, the WD1015 enables the WD11C00-17 to send only one interrupt to the Host at the end of the transfer.

6.8.1 EXCEPTION HANDLING

No commands can be executed by the WD1010A-05 with $\overline{DRDY}$ de-asserted, $\overline{SC}$ de-asserted, or $\overline{WF}$ asserted. In these cases, the WD1015 aborts the issued command. No attempts are made to recover from these conditions.

Before any data transfer can take place, the WD1010A-05 attempts to read the I.D. field of the logical block address specified. If any errors are detected in this process, the WD1010A-05 attempts to read the I.D. field until two index pulses are detected. If the I.D. field can not be read, the WD1015 reissues the command once each disk revolution for ten disk revolutions to recover from the error. If this is unsuccessful, the WD1015 performs an Autorestore. The Autorestore recalibrates the selected logical unit and performs a re-seek to the logical block address specified. The WD1010A-05 attempts to read the I.D. field once each disk revolution for ten disk revolutions. If the error is unrecoverable, the operation is terminated. The error reported is the last error encountered, assuming that the same error is responsible for any attempted retries.

A similar operation is performed on all missing Data Address Marks during a read operation. If the I.D. field can be read correctly, data transfer between the Host and WD1010A-05 can take place. For a write operation, the location of the desired I.D. field is all that is required to write data to the disk from the Sector Buffer. Multiple sector transfers are broken into single sector transfers as described in Section 6.8. For a read operation, the data field is corrected, if possible, before being transferred to the Host.

The WD1015 controls the operation of the WD11C00-17 ECC circuitry. During the transfer of data from the Sector Buffer to the disk, the WD11C00-17 computes a four byte ECC that is appended to the end of the data transferred to the WD1010A-05 and recorded on the disk. During data transfers from the WD1010A-05 to the Sector Buffer, the WD11C00-17 uses the ECC circuitry to validate the data. If data is corrputed, the WD1015 performs retries and correction. A maximum of eight retries are attempted if two consecutive syndromes do not match. Correction is attempted only when two consecutive syndromes match. If the error is uncorrectable, the operation is terminated.

All exception handling results in a loss of at least one disk revolution.

6.9 SECTOR BUFFER

The Sector Buffer consists of a 2KB by 8 bit RAM that is used to hold data or the CCB. Only the lower 1KB of the RAM is actually used. Therefore, the terms upper and lower in the succeeding paragraph are relative to the lower 1KB of the RAM.

The lower half of the RAM is used mainly for the CCB, status and error information, and storage for the ECC bytes. The eight bytes of drive characteristics from the Host during an Initialize Drive Parameters command are also stored in page zero of the RAM. The sector data is stored in the upper half of the RAM. The Sector Buffer also holds the information to be recorded on the disk during a Format command in exactly the same way as a sector of data written to the disk.

6.10 WD1010A-05 WINCHESTER DISK CONTROLLER

The WD1010A-05 is a single chip device designed for use with Seagate Technology ST506 and other compatible disk drives. All disk commands are started by the WD1015 after the CCB has been read and properly translated. The primary purpose of the WD1010A-05 is to control data (this includes data separation for Read Data) transfer between the disk and the Sector Buffer after the WD1015 has positioned the selected head over the desired track. The WD1010A-05 can position the disk heads, but this capability is not used in the design because the desired step rates are not supported by the WD1010A-05. Refer to the WD1010-05 data sheet in the Western Digital Storage Management Products Handbook for further details on the WD1010A-05.

6.11 WD10C20

The WD10C20 interfaces the disk drive to the other circuitry on the WD1002S-WX2. The WD10C20 contains two major circuits. These two circuits are the Write Precompensation circuitry and data synchronization.

6.11.1 CLOCK GENERATOR

A 10 MHz fundamental frequency crystal is required by the WD10C20. The crystal frequency is used as a reference clock and then divided by two for a WRITE CLOCK (WCLK) which is used to produce MFM write data for the disk. These clock sources are provided by the WD10C20.

The WD1015 uses the 5 MHz WCLK, provided by the WD10C20, giving an instruction cycle time of 3.0μsec. Most instructions execute in two cycles or 6.0μsec.

6.11.2 WRITE PRECOMPENSATION CIRCUIT

The generation of MFM Write Data takes place in the WD1010A-05. The WD1010A-05 accepts a byte of data and a WCLK to internally produce MFM data. The MFM data is now totally compatible with the required format for transmission to the disk via line drivers with one exception. Due to decreasing radius on the physical surface of the disk, the inside tracks have less circumference and therefore exhibit an increase in recording flux density over the outside tracks. This increase in flux density aggravates a problem known as dynamic bit shift.

Dynamic bit shift comes about as a result of one bit on the disk (a flux reversal) influencing an adjacent bit. The result is to shift the leading edge of both bits closer together or further apart than originally recorded. The net result is that enough jitter is added to the data recorded on the inside tracks to make them harder to recover without error.

Write precompensation is used to reduce the effect of dynamic bit shift on the recorded data. It is a method of predicting which direction a particular bit is shifted and intentionally writing that bit out of position in the opposite direction from the expected shift. This is performed by examining two data bits: the last one written and the present one to be written to the disk. A comparison of these bits produces one of three signals: EARLY, NOMINAL, or LATE. These signals are used with a delay line (intervals of 12nsec) to cause the leading edge of the data or clock bit to be written EARLY, LATE, or on time (NOMINAL).

The WD1015 enables or disables the generation of these write precompensation signals by controlling the LS signal. Assertion of LS enables write precompensation. De-assertion of LS disables write precompensation and the NOMINAL output is asserted.

The WD10C20 internal logic performs the write precompensation. The MFM write pulses are applied to internal logic. The WMFM output depends upon the state of the three write precompensation signals. From here, the data is converted to a differential form and then transmitted to the disk drive.

6.11.3 DATA SEPARATOR

Data is recorded on the disks using MFM techniques. This technique requires clock bits to be recorded only when two successive data bits are missing in the serial data stream. In other words, if two successive data bits are zeroes, then a clock pulse is generated. A logical one data bit is recorded as a pulse and a logical zero is recorded as not pulse. The fact that clock bits are not recorded with every data bit cell requires circuitry that can remain in synchronization with data during the absence of clock bits. Synchronous decoding of MFM data streams requires the decoder circuitry to synthesize clock bit timing when clocks are missing and synchronize to clock bits when they are present. This is accomplished by using a phase locked oscillator employing an error amplifier and filter to synchronize with and hold a specific phase relationship to the data and clock bits in the data stream. The phase lock occurs at the crystal frequency, which in turn is used to synthesize a clock called RCLK with a frequency one half of the crystal frequency. This synthesized clock is used to separate data bits from clock bits by the external logic for deserialization into bytes.

Refer to the WD10C20 Data Sheet for further details.

SECTION VII
INSTALLATION

7.1 HARDWARE AND SOFTWARE INSTALLATION

This section briefly describes installation of the WD1002S-WX2 in an IBM PC or IBM-compatible computer.

1. Ensure system power is off.
2. Insert WD1002S-WX2 in computer chassis and connect drive cables. (J1 = control cable, J2 = drive 0 cable, J3 = drive 1 cable.)
3. Power up the system.
4. Insert IBM PCDOS 2.0 or IBM PCDOS 2.1 diskette.

CAUTION
Performing steps 5 through 9 destroys any data presently on the disk.

5. Load DEBUG utility by typing "debug" and ENTER after the DOS prompt.
6. Initiate the WX2FMT (format) program by typing the following command line: -g=c800:5
7. Press "y" to begin formatting drive 0 (logical drive C).
8. To format drive 1 or second drive in a daisy chain, reload DEBUG utility. Type "RAX" and ENTER. Prompt returns "AX 0000". Type "0103", ENTER which defines relative drive number and interleave factor (01 = relative drive number; 03 = interleave factor). Type "G=C800:5", ENTER, and type "y" to begin formatting drive 1 (logical drive D).
9. Run standard DOS utilities, FDISK and FORMAT.

7.2 JUMPER INSTALLATION AND LOCATIONS

The WD1002S-WX2 is configured for the standard IBM PCXT with jumper plugs installed at W3, W4, and W6. No jumpers are required at W5 and W7. To change the configuration, a jumper plug can be installed in the appropriate block. Installation of jumpers on W5 and W7 requires carefully cutting an etch and placing a jumper plug onto the Jumpered position. To restore the standard setting, move the jumper plug to the Standard position. Table 7-1 describes these jumpers and options. Table 7-2 describes the drive configuration jumpers and an INTERRUPT REQUEST (IRQ) jumper in SW1. Figure 7-1 illustrates the locations of W1 through W7 and SW1.

TABLE 7-1. JUMPER SELECTABLE OPTIONS (W1 THROUGH W5)

JUMPER	FUNCTION	PIN	DESCRIPTION
W1, W2			For Western Digital Manufacturing use only.
W3	Standard:	1-2	Closed by etch or jumper. Enables BIOS ROM.
	Jumpered:	1-2	Open. Disables BIOS ROM.
W4	Standard:	2-3	Selects primary port 320 hex.
	Jumpered:	1-2	Selects secondary port 324 hex. Requires custom BIOS.
			NOTE The WD1002S-WX2 provides two sets of I/O ports. The primary port addresses are 320 through 323 hex. The secondary port addresses are 324 through 327 hex. However, secondary ports on the WD1002S-WX2 are **NOT** supported by any version DOS.
W5	Standard:	1-2	Selects 2732 or 2764 BIOS ROM size.
	Jumpered:	2-3	Selects 2716 BIOS ROM size. W5 pin 1-2 etch must be cut.
W6	Standard:	2-3	8 head configuration, RWC used.
	Jumpered:	1-2	16 head configuration, RWC **not** used, requires custom BIOS ROM and WD1015-24.
W7	Standard:	1-2	Selects IRQ5.
	Jumpered:	2-3	Selects IRQ2. SW1 position 8 must also be jumpered (closed) and W7 pin 1-2 etch must be cut.

TABLE 7-2. SW1 JUMPER BLOCK DESCRIPTION

WD BIOS 62-000042-01 (ROM) or 62-000042-11 (EPROM)

BIOS TABLE	FORMATTED CAPACITY	POSITION 1 2 DRIVE 1	POSITION 3 4 DRIVE 0	DRIVE TYPE	HEADS	NUMBER OF CYLINDERS	PRE-COMP RWC
3	10MB	1 1	1 1	ST412 Seagate	4	306	0 None
2	15MB	0 1	0 1	ST419 Seagate	6	306	256 RWC = 128
1	26MB	1 0	1 0	5820 Evotek	8	375	0 None
0	5MB	0 0	0 0	ST506 Seagate	2	306	0 None
WD BIOS 62-000042-12 (EPROM)							
3	10MB	1 1	1 1	ST412 Seagate	4	306	0 None
2	20MB	0 1	0 1	ST225 Seagate	4	612	128 None
1	10MB	1 0	1 0	3012 MiniScribe	2	612	128 RWC = 128
0	20MB	0 0	0 0	HH725 Microscience	4	612	None None

Factory sets jumpers for BIOS Table 3. Position 5 of SW1 select IRQ5 (factory setting) or IRQ2. 1 = IRQ5. 0 = IRQ2. Positions 6, 7, and 8 of SW1 are reserved.

LEGEND: 1 = no jumper installed, ties input to +5vdc. 0 = jumper installed, ties input to ground.

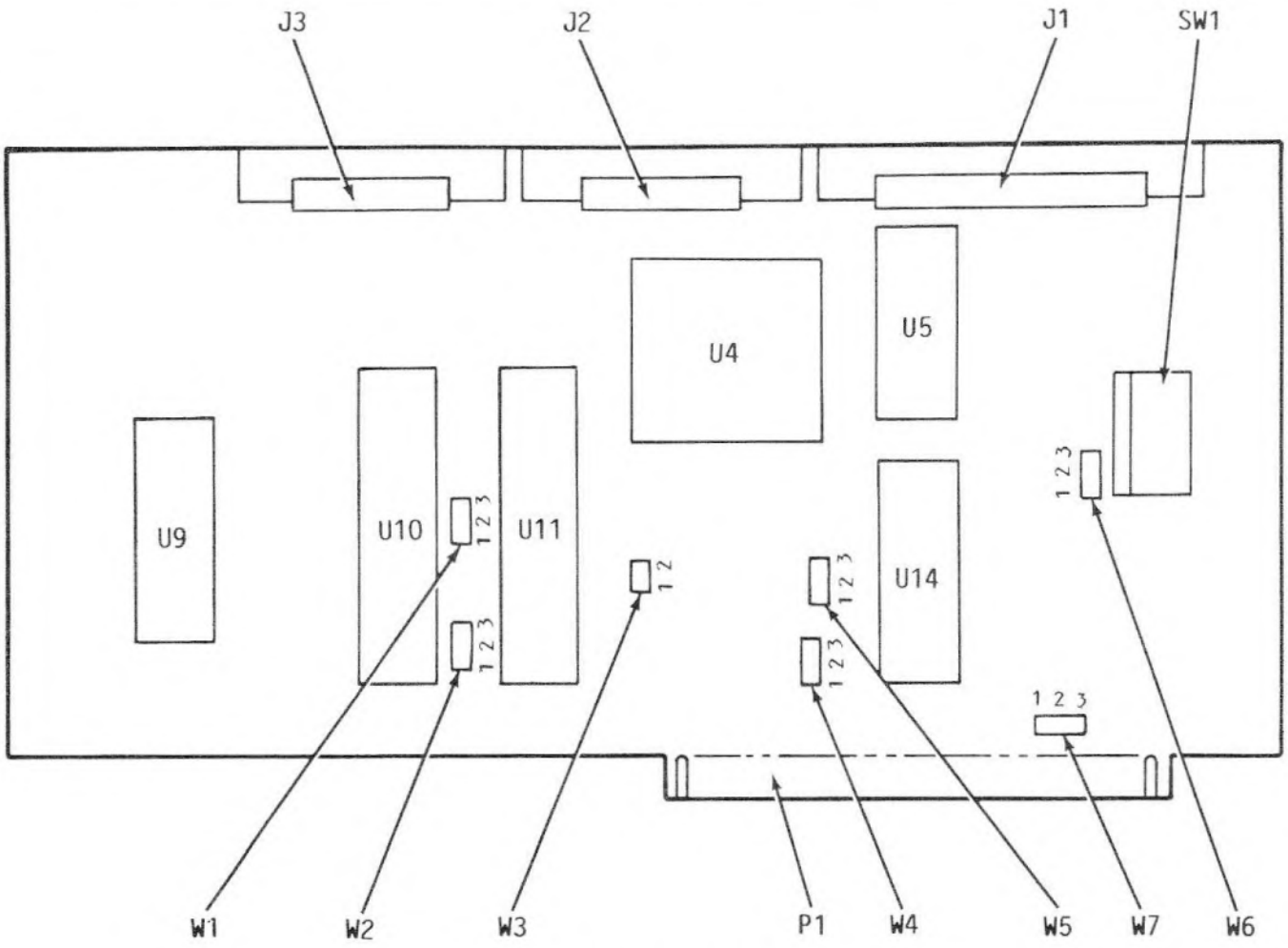


FIGURE 7-1. JUMPER LOCATIONS

7.3 BIOS ROM INSTALLATION

The WD1002S-WX2 firmware driver routines, supplied by Western Digital Corporation, reside in a 4KB x 8 bit EPROM. This BIOS ROM is available in three sizes as follows:

2716 2KB x 8 bit
2732 4KB x 8 bit (standard from the factory)
2764 8KB x 8 bit

The WD1002S-WX2 provides a 28 pin DIP socket for the BIOS ROM. This socket accomodates a 2732 or 2764 JEDEC EPROM. Figure 7-2 illustrates the standard connections for the 2732 or 2764. These connections can be modified to support a 2716. Perform the following steps to modify the standard connections:

1. Cut the etch between pads 1 and 2 on W5
2. Jumper pad 3 to pad 2
3. Wire pins 20 and 26 as shown.
4. Plug BIOS in the socket. Pin 1 of the 2716 BIOS should be in position 3 of the socket.

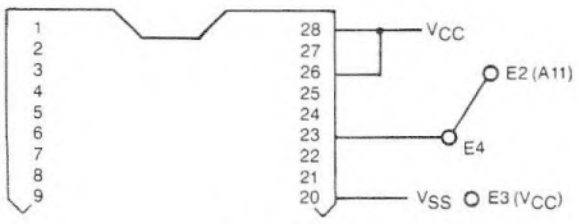


FIGURE 7-2.
BIOS ROM SOCKET CONNECTIONS

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WD10C20 READ/WRITE CHANNEL DEVICE

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1. WD1020 FEATURES

- Designed specifically for the industry standard WD1010/WD2010 Hard Disk Controllers and ST506 type Winchester disk drives.
- Provides all processing of the sensitive read/write data signals
- Highly stable LC type Voltage Controlled Oscillator
- Self Adjusting VCO compensates for component, temperature, voltage, and aging variations
- Uses frequency detection on crystal reference and on the data synchronization field to eliminate 180 degree lock due to drive asymmetry, and to eliminate harmonic lock from write splices
- Zero Phase Startup for faster, more predictable lock acquisition
- Locks to crystal reference while idle
- Dual gain: high for faster acquisition
  low for more jitter rejection while tracking
- External pump current control
- Integrated crystal oscillator circuit
- Inexpensive external components
- Will accomodate other data rates through selection of external components
- Available in 28-pin DIP or 28-pin QSM leaded surface mount chip carrier
- Low power CMOS design

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2. GENERAL DESCRIPTION

The WD1020 Read/Write Channel is an LSI device implemented in 3 micron high-speed CMOS. It is specifically designed to be compatible with the Western Digital WD1010/WD2010 series of Hard Disk Controllers, and with disk drives conforming to the popular ST506 interface standard. In a typical application, it performs all of the handling of the sensitive read/write signals between a Hard Disk Controller and data drivers and receivers. Read data corresponds to previous write data, with added phase, frequency, and write splice noise. The fundamental purpose of the WD1020 is to remove these sources of noise, and present a clean, digital read signal to the Hard Disk Controller.

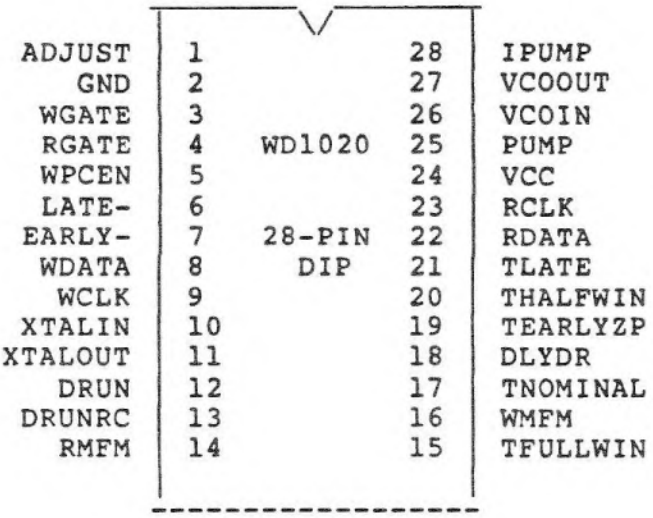
The WD1020 performs phase-locked loop data synchronization on read data from the drive. An on-board synch field detector automatically switches the PLL from the stable crystal reference to the read data. The VCO is halted and restarted in phase with the data to eliminate initial acquisition in the wrong frequency direction. Frequency-phase detection is used at the beginning of the synch field to quickly and reliably acquire lock to the data. Use of this technique eliminates susceptibility to harmonics and asymmetry. The WD1020 then switches to phase-only detection to complete the phase acquisition before the end of the synch field, and to enable tracking of random MFM read data. When switching to phase detection, the WD1020 reduces the error amplifier gain for better rejection of drive jitter. A precisely aligned detector samples the data at the underlying data rate to remove the phase jitter. The regenerated signal, along with a fixed-phase synchronous clock, are output for the Hard Disk Controller's digital circuits.

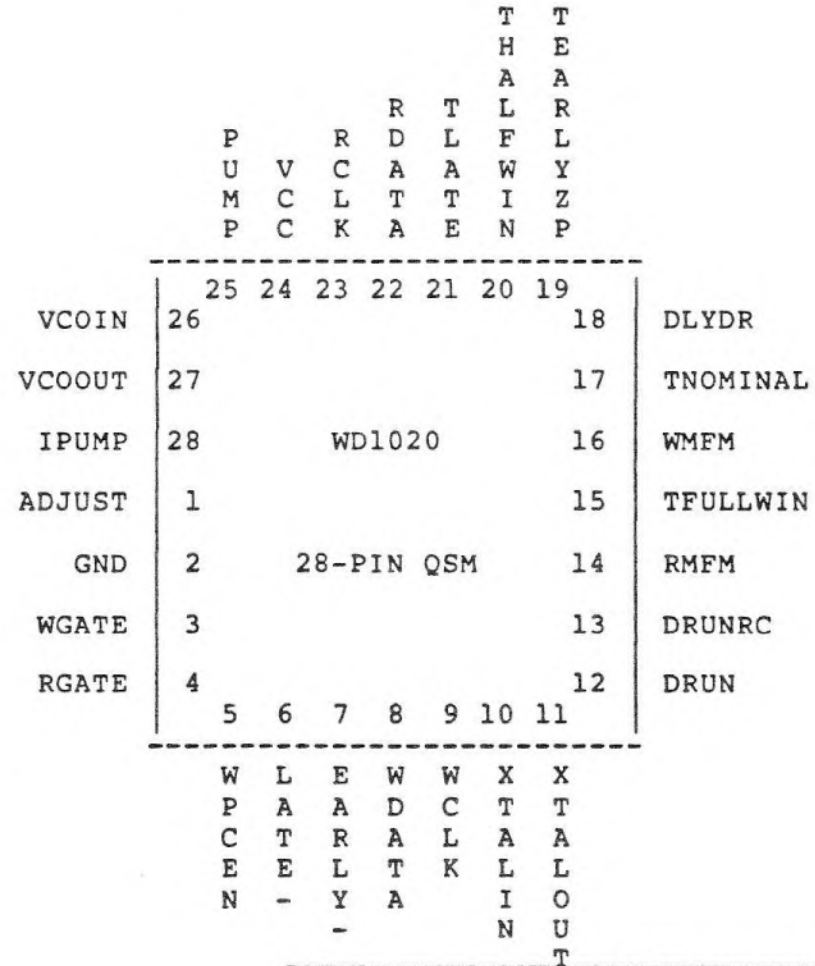
The WD1020 performs conditioning on write data to the drive. MFM data from the Hard Disk Controller is precisely clocked with a signal at twice the data frequency to minimize digital phase noise. If precompensation is enabled, early, nominal, and late taps on an external delay line are multiplexed through matched delay paths to produce synchronized, precompensated write data, which is sent directly to the drive's write circuits.

The device has been designed to work at the 5 Mbit/sec data rate of the ST506 interface. Other data rates may be accomodated through selection of external components.

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3. PINOUTS





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CLASS CODE	BASE NUMBER	DASH	BIN/ROM CODE	REV.	DCLC
96	000052			A	
SCALE		SHT 6 OF 30			

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4. PIN DESCRIPTIONS

NOTE: Signals have the same pin numbers for both packages.

NAME	I/O	PIN#	FUNCTION
RMFM	I	14	MFM data received from the drive read circuits. Includes an internal nominally 4K ohm pullup resistor to allow tri-state multiplexing of drives' data receivers.
RDATA	O	22	Detected and regenerated version of RMFM. Jitter has been removed and pulses have been synchronized with RCLK.
RCLK	O	23	VCOIN divided to half frequency. Tracks the base frequency of RMFM during a read operation; otherwise tracks the crystal frequency.
DRUN	O	12	The output of a frequency detector connected to the RMFM read data. It's detection threshold is nominally set to a period of 1 3/8 bit times. Short, high frequency periods cause it to go high; long, low frequency periods cause it to go low.
DRUNRC	I/O	13	Connected to an external RC timing circuit for generating DRUN
RGATE	I	4	Read gate. Set high when the Controller intends to read.
WGATE	I	3	Write gate. Set high when recording onto the disk.
WDATA	I	8	Write data. MFM data to be conditioned and sent out through WMFM and written onto the disk.
EARLY-	I	7	Negative true inputs used to advance or delay write data
LATE-	I	6	for write precompensation.
WPCEN	I	5	Write precompensation enable. When high, it enables EARLY- and LATE-.
WMFM	I	16	Write data sent to the drive write circuits. Low when WGATE is low.
XTALIN	I	10	Input/output pins for a crystal oscillator circuit. If
XTALOUT	O	11	an external frequency source is desired, XTALIN can be driven by a TTL output and XTALOUT left open.
WCLK	O	9	Clock signal at one half the crystal frequency.
DLYDR	O	18	Delay line driver to external delay line.
TEARLYZP	I	19	Delay line tap for early precompensated write data and for timing the zero phase startup of the VCO.
TNOMINAL	I	17	Delay line tap for uncompensated write data.

TLATE	I	21	Delay line tap for late precompensated write data.
THALFWIN	I	20	Delay line tap for generating the enable phase delay when in phase detection mode.
TFULLWIN	I	15	Delay line tap for generating full window MFM pulses.
PUMP	I/O	25	Charge pump output to the PLL filter. Also a voltage input to the self adjust sensing circuitry.
VCOIN	I/O	26	Input/output of the VCO gain stage. VCOIN is clamped
VCOOUT	O	27	low and then released during zero phase startup.
ADJUST	O	1	Output pin for self calibration of the PLL.
IPUMP	I	28	An external resistor connected to this pin sets the magnitude of the charge pump current and the ADJUST current.
GND	I	2	GROUND
VCC	I	24	+5 Volts

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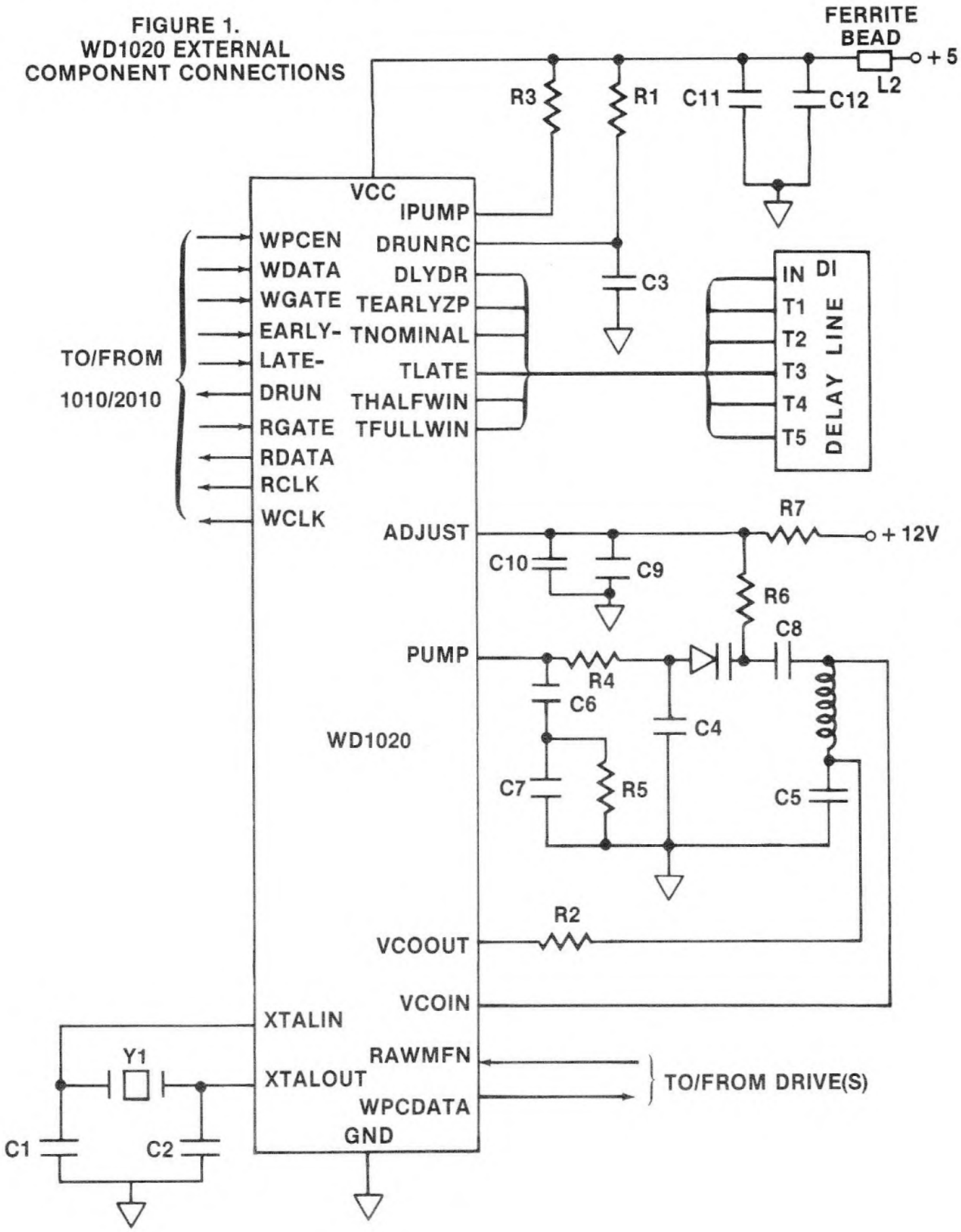
5. ORGANIZATION

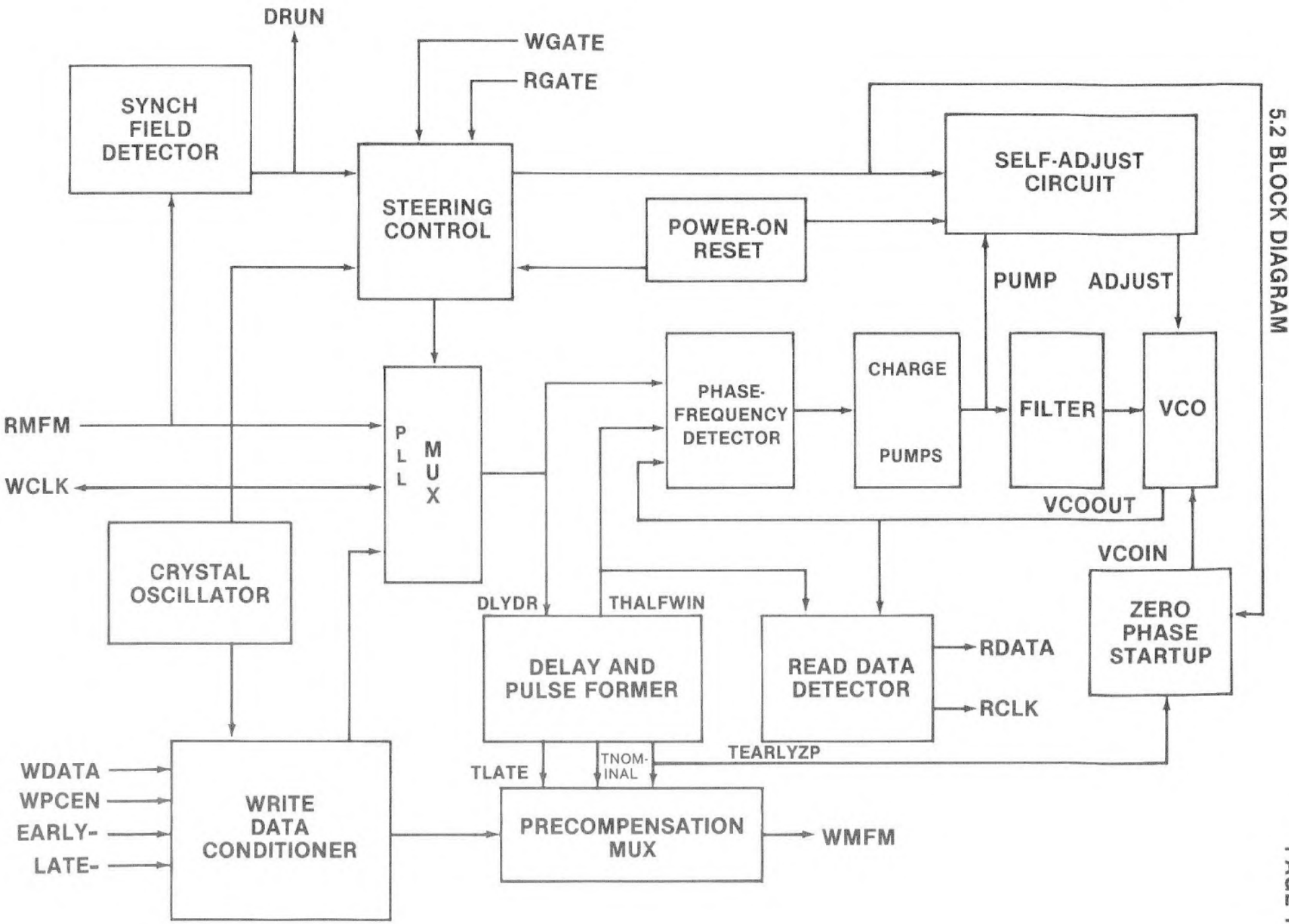
A schematic showing the connections of external components to the WD1020 is shown in Figure 1. This circuit is represented functionally by the block diagram of Figure 2.

The elements in the circuit are a Crystal Oscillator, Synchronization Field Detector, Write Data Conditioner, Delay and Pulse Former, Steering Control, Power-On Reset, Read Data Detector, and Phase-Locked Loop, which consists of a Phase-Frequency Detector, Charge Pumps, Filter, Voltage Controlled Oscillator, Zero Phase Startup Circuit, and Self-Adjustment Circuit.

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FIGURE 1.
WD1020 EXTERNAL
COMPONENT CONNECTIONS





WD1020 BLOCK DIAGRAM
FIGURE 2

5.3 CIRCUIT ELEMENTS

5.3.1 SYNCHRONIZATION FIELD DETECTOR

The purpose of this section is to detect the presence of a synchronization field preceding an MFM field which the Hard Disk Controller may wish to read.
The criterion used is pulse period discrimination on the RMFM read data. The external resistor and capacitor connected to the DRUNRC pin are used to set the nominal detection threshold of 1 3/8 bit times. If the period between consecutive rising edges of RMFM is short with respect to the threshold, then DRUN will go high; if long, then DRUN will go low.

5.3.2 STEERING CONTROL

This logic controls the sequencing of events when the WD1020 is switching between read, write, and idle modes. When switching, the Steering Control disables the Phase-Frequency Detector and Charge Pumps, switches the MUX source, invokes zero phase startup, and selects the velocity lock mode of the Phase-Frequency Detector. After the zero-phase startup is complete, the Phase-Frequency Detector and Charge Pumps are enabled. If the device is in read or write mode, then after four byte times the Steering Control switches to phase detection.

5.3.3 PHASE-LOCKED LOOP (PLL)

5.3.3.1 PHASE-FREQUENCY DETECTOR

The Phase-Frequency Detector can be operated in two modes. The velocity lock mode is used for acquisition when the PLL is switched to read or write data, and is always used when the PLL is following the reference crystal oscillator. The second mode is standard phase-only detection. The Steering Control logic switches to this mode when frequency acquisition is essentially complete on data, and phase acquisition is nearly complete as well. Internal delay paths have been carefully matched to minimize introduction of a phase error due to switching. Phase-only mode must, of course, be used to lock to the MFM following the synch field, since that will contain the three MFM frequencies.

In either mode, the Phase-Frequency detector converts a phase difference between the VCO and input to a pulse width equal to the phase difference. The polarity of the phase error determines whether a signal will be routed to the pump up or down circuitry in the Charge Pump section.

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5.3.3.2 CHARGE PUMPS

This circuit converts the pulse widths received from the Phase-Frequency Detector to proportional amounts of charge into or out of the Filter. The gain of the Charge Pumps is set by the input current on the IPUMP pin. This current is set by an external resistor connected to VCC.

5.3.3.3 FILTER

The Filter converts the current pulses from the Charge Pumps to a voltage output to the VCO. It also performs the sample-and-hold function necessary for an edge locked PLL, and also necessary during the Zero Phase Startup period. As can be seen in the topology of Figure 1, one of the Filter's capacitors is also part of the VCO's series resonant oscillator.

The Filter must be carefully designed to the specific requirements of acquisition time, capture range, and jitter rejection, and within the context of its effect on VCO operation. Roughly speaking, it functions to filter out high frequency signals due to RMFM read data jitter, while passing the low frequency signals associated with the slowly varying underlying frequency of RMFM.

5.3.3.4 VOLTAGE CONTROLLED OSCILLATOR (VCO)

The VCO is a series resonant LC oscillator. The active gain element providing the energy to sustain oscillation is within the WD1020, between the VCOIN and VCOOUT pins. The VCO is controlled and tuned with an inexpensive varactor. The filter is connected to the anode of the varactor, providing the voltage for loop operation of the PLL. Note that higher voltages at the VCO input correspond to lower frequencies, and vice-versa. The cathode of the varactor is connected to the Self-Adjustment Circuit. The voltage bias on the cathode determines the location of the VCO's V-F characteristic curve. The bias is set for a favorable voltage at the nominal frequency of the VCO.

5.3.3.5 ZERO PHASE STARTUP CIRCUIT

The Zero Phase Startup circuit is a set of logic and a clamp on the VCOIN pin. When the WD1020 changes the PLL input signal, the logic turns on the clamp for a minimum of one input data period. The clamp stops the operation of the VCO oscillator gain stage and removes the AC energy from the passive VCO components. This puts the VCO into a known state, so that there is a predictable time from release of the clamp until the first VCO edge reaches the Phase Frequency Detector. So that this event can be made to coincide with the arrival of a data pulse, the TEARLYZP tap of the delay line is set with respect to THALFWIN.

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5.3.3.6 SELF ADJUSTMENT CIRCUIT

The Self Adjustment Circuit tunes the VCO so that its nominal output frequency of twice the data rate will correspond to an input voltage favorable to the Charge Pumps. This voltage is approximately half of VCC, and centers the capture range. An internal comparator connected to the PUMP pin detects whether the voltage into the VCO is above or below the threshold voltage, called VSENSE. The comparator is sampled at a low frequency derived from the crystal, and the output is used as the up/down control to a six-bit counter. At power-on, this counter is set to half full scale. The least significant two bits are for noise immunity only. The most significant four bits are connected to a digital-to-analog converter (DAC), which controls the current sinking ability of the ADJUST pin. Externally, a resistor to +12 volts is connected to the ADJUST pin to convert the current to a voltage. A large capacitor is also connected to the ADJUST pin to heavily filter the DAC steps and transients. A large value resistor from the ADJUST pin to the cathode of the VCO varactor completes the circuit. The Self Adjustment Circuit functions to slowly keep the VCO's input voltage near the VSENSE level. It not only performs compensation for component variations in the same way that a manual adjustment would, but it also compensates for dynamic variations such as temperature, voltage, and aging. Another beneficial characteristic of this circuit is heavy RC filtering of the +12 volt supply.

5.3.4 READ DATA DETECTOR

This circuit produces the signals RCLK and RDATA. RCLK is a square wave at one half the VCO frequency. During data tracking, the frequency of RCLK mirrors the slowly varying frequency of the RMFM read data. RDATA is a regenerated form of RMFM, with jitter removed and one-half bit time pulse widths.
It is exactly synchronous with RCLK.
RCLK edges occur nominally in the center of RDATA pulses to allow sufficient setup and hold time for the digital circuits in the Hard Disk Controller that use these signals.

5.3.5 CRYSTAL OSCILLATOR

The Crystal Oscillator is designed to operate in the parallel resonant mode, with an external crystal and two capacitors. It generates the WCLK signal used externally. Internally, various divisions of it are used by the Write Data Conditioner, the Phase Locked Loop, and the Self Adjustment Circuit.

When an externally generated clock is desired, the crystal and capacitors are omitted. The XTALIN pin is connected to the clock source, with XTALOUT left disconnected. Note that the input levels of the XTALIN pin are not TTL, and must be guaranteed by the clock source.

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5.3.6 WRITE DATA CONDITIONER

The Write Data Conditioner samples and precisely synchronizes WDATA, EARLY-, and LATE- on the rising and falling edges of WCLK. When WGATE is active, the synchronized WDATA is channeled through the MUX and passes through the DLYDR pin to the delay line. It returns to the WD1020 through the TEARLYZP, TNOMINAL, and TLATE input pins. If WPCEN is low, then the TNOMINAL tap is selected and passed to the WMFM output pin. If WPCEN is high, then the EARLY- and LATE- signals will select the TEARLYZP- and TLATE inputs, respectively. The differential delay between TEARLYZP and TNOMINAL at the delay line defines the amount of early precompensation, and similarly, TNOMINAL to TLATE defines the amount of late precompensation. The internal paths used for multiplexing these three inputs use precisely matched elements, and do not alter the amount of precompensation set by the delay line.

When WGATE goes high, one of the initial MFM pulses is supressed to create an interval of two bit times. This ensures that DRUN will go low at the beginning of a data synch field, so that zero phase startup and velocity lock will be executed properly. When WGATE goes low, WMFM will be held low.

5.3.7 DELAY AND PULSE FORMER

This section includes the external delay line and logic internal to th WD1020. In response to input rising edges it produces positive pulses slightl longer than one detection window, which is half of a bit time. The taps are also used for write precompensation, zero-phase startup, and defining the enable window for phase detection. Depending upon the mode of operation, its input is RMFM read data, synchronized WDATA, or WCLK.

5.3.8 POWER-ON RESET

This integrated function is used to reliably set flip-flops to a predictable state during the application of VCC. It is used by the Steering Control and Self Adjustment sections.

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6. DC ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

VCC with respect to GROUND	+5.5 volts
Max voltage on any pin with respect to GROUND, with the exception of ADJUST	-0.5 to VCC + 0.5 volts
Max voltage on ADJUST pin with respect to GROUND	-0.5 to +13.2 volts

DC OPERATING CHARACTERISTICS OVER Ta = 0 to 60 deg. C; VCC = 4.75 to 5.25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
INPUTS:	TEARLYZP,TNOMINAL,TLATE,THALFWIN,TFULLWIN,RGATE,WGATE, WPCEN,WDATA,EARLY-,LATE-,RMFM					
VIH	INPUT HIGH VOLTAGE	2.0			V	
VIL	INPUT LOW VOLTAGE			.8	V	
INPUT:	XTALIN					
VIH	INPUT HIGH VOLTAGE	3.0			V	
VIL	INPUT LOW VOLTAGE			.8	V	
INPUTS:	TEARLYZP,TNOMINAL,TLATE,THALFWIN,TFULLWIN,RGATE,WGATE					
IIN	INPUT LEAKAGE CURRENT			+/-10	uA	VIN = GND TO VCC
INPUTS:	WPCEN,WDATA,EARLY-,LATE-					
IIH	INPUT HIGH CURRENT			+/-10	uA	VIH = 2.4 V
IIL	INPUT LOW CURRENT			-1.6	mA	VIL = .4 V
INPUTS:	XTALIN					
IIH	INPUT HIGH CURRENT			125	uA	VIH = 3.4 V
IIL	INPUT LOW CURRENT			-250	uA	VIL = .4 V
INPUT:	RMFM					
IIH	INPUT HIGH CURRENT			0	mA	VIH = 2.4 V INTERNAL
IIL	INPUT LOW CURRENT			-2.5	mA	VIL = .4 V PULLUP RESISTOR
OUTPUTS:	WCLK,WMFM,DLYDR,XTALOUT					
VOH	OUTPUT HIGH VOLTAGE	2.4			V	IOH = -1 mA
VOL	OUTPUT LOW VOLTAGE			.4	V	IOL = 4 mA
TRISE	RISE TIME .8 TO 2.0 V	10			nsec	CL = 30 pf
TFALL	FALL TIME 2.0 TO .8 V	10			nsec	CL = 30 pf
OUTPUTS:	WCLK,RCLK,RDATA,DRUN					
VOH	OUTPUT HIGH VOLTAGE	4.7			V	IOH = -100 uA
VOL	OUTPUT LOW VOLTAGE			.2	V	IOL = 400 uA
TRISE	RISE TIME .9 TO 4.2 V	30			nsec	CL = 15 pf
TFALL	FALL TIME 4.2 TO .9 V	30			nsec	CL = 15 pf

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SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS	
VS	VSENSE THRESHOLD		2.4		V		NOTE
IA	ACQUISITION PUMP CURRENT		+/-6		mA	3.57K on IPUMP	NOTE
IT	TRACKING PUMP CURRENT		+/-4.5		mA	3.57K on IPUMP	NOTE
IJMX	ADJUST MAX CURRENT	.4	.6	1.0	mA	3.57K on IPUMP	
IJMN	ADJUST MIN CURRENT			+/-10	uA		
ICC	POWER SUPPLY CURRENT		40		mA	3.57K on IPUMP, 5MHz	

NOTE 1: Depending upon the application, there are specific requirements upon the pump currents and their relationship to VSENSE. See section 8. for requirements for 5 Mbit/sec operation.

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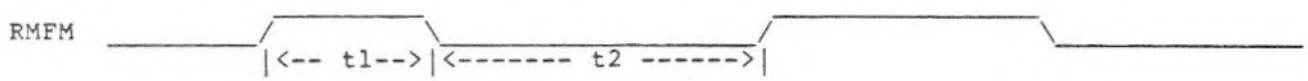
7. TIMING CHARACTERISTICS

Timing on signals RDATA, RCLK, WCLK, and DRUN are measured at the voltage halfway between the 1010/2010's VIH & VIL: 2.55 Volts.
All other signals measured from the 1.4 V transitions.

The following are timings that are independent of the application of the device. More timings are specified in the section on 5Mbit operation.

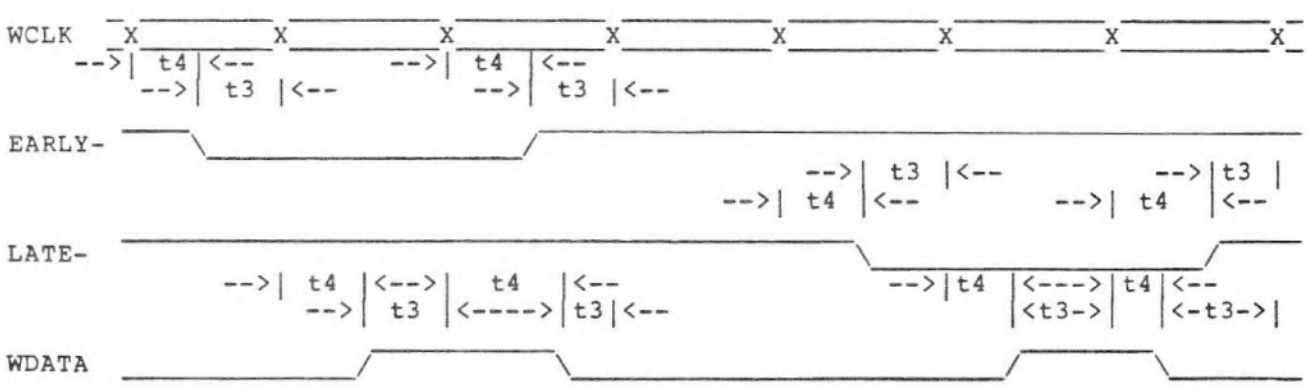
7.1 DISK DRIVE READ DATA

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
t1	RMFM PULSE WIDTH HIGH	20	-	nsec	
t2	RMFM PULSE WIDTH LOW	20	-	nsec	



7.2 WRITE PRECOMPENSATION

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
t3	SETUP TIME: EITHER EDGE OF EARLY-,LATE-, OR WDATA TO EITHER EDGE OF WCLK	20	-	nsec	
t4	HOLD TIME: EITHER EDGE OF EARLY-,LATE-, OR WDATA TO EITHER EDGE OF WCLK	5	-	nsec	



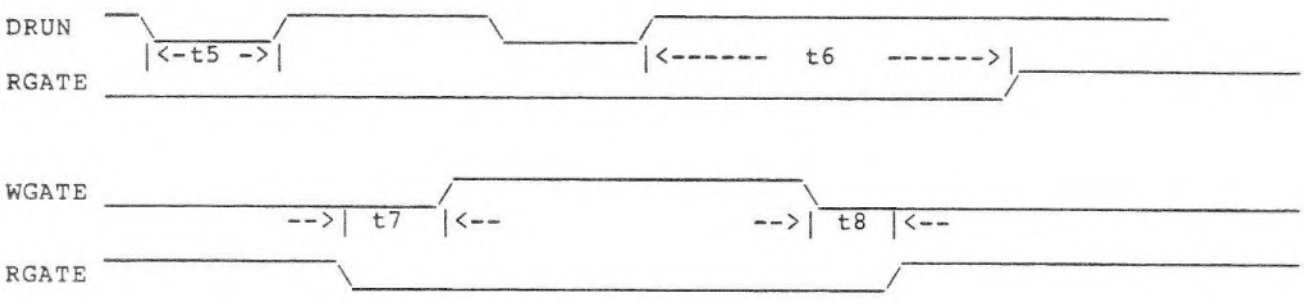
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SCALE		SHT 18 OF 30			

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7.3 DRUN, RGATE, WGATE

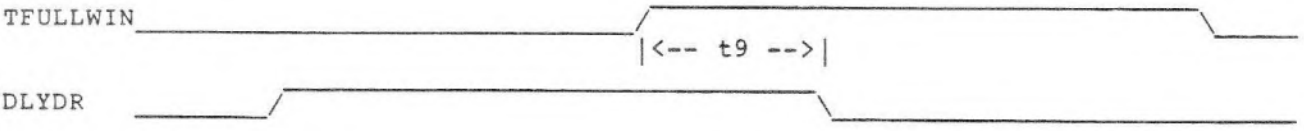
SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
t5	DRUN LOW PULSE WIDTH	30		nsec	note 3
t6	DRUN HIGH TO RGATE HIGH	0	4	byte times	note 4
t7	RGATE LOW TO WGATE HIGH	20		nsec	
t8	WGATE LOW TO RGATE HIGH	20		nsec	

note 3: No requirement on DRUN pulse width high.
note 4: During Controller read.



7.4 DLYDR, TFULLWIN

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
t9	DLYDR SHUTOFF TIME	12	24	nsec	



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8. APPLICATION SPECIFICATION: 5 MBIT/SEC, WD1010/2010, ST506 DRIVE

This section details the specific requirements and performance of the WD1020 in its most common application. The Hard Disk Controller is a WD1010 or WD2010, the disk drive conforms to ST506, and the data rate is 5Mbit/sec. The relevant schematic is the same as in Figure 1. Following are the component and performance specifications.

8.1 EXTERNAL COMPONENT LIST

ITEM	REF DESIGNATOR	DESCRIPTION	QUANTITY
1	D1	DELAY LINE 12,24,36,60,96 NSEC	1
2	Y1	CRYSTAL, 10.00MHZ	1
3	CR1	TUNING DIODE, MVAM109	1
4	L1	INDUCTOR 4.7 UH, 5%	1
5	L2	FERRITE BEAD	1
6	R2	RESISTOR, 220 1/4W 5%	1
7	R5	RESISTOR, 750 1/8W 1%	1
8	R4	RESISTOR, 1.5 K 1/8W 1%	1
9	R1	RESISTOR, TAS* 1/8W 1%	1
10	R3	RESISTOR, 3.57K 1/8W 1%	1
11	R7	RESISTOR, 15.0K 1/8W 1%	1
12	R6	RESISTOR, 100K 1/4W 5%	1
13	C3	CAP 68PF 50V 5% CER N750	1
14	C1	CAP 100PF 50V 5% CER NPO	1
15	C2	CAP 120PF 50V 5% CER NPO	1
16	C7	CAP 150PF 50V 5% CER NPO	1
17	C4,C5	CAP 180PF 50V 5% CER NPO	2
18	C8	CAP 1000PF 50V 5% CER NPO	1
19	C6	CAP 4700PF 50V 5% CER NPO	1
20	C10,C12,C13	CAP .01MF 50V +80/-20% CER	3
21	C11	CAP 1MF 10V 50% TANT	1
22	C9	CAP 10MF 25V 20% TANT	1

* Test And Select. This resistor's nominal value is 2.98K. In production, the board is tested and the proper fixed resistor is installed.

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8.2 EXTERNAL COMPONENT SPECIFICATIONS

The following apply in addition to the previous components list. In all cases, components must be compatible with the standard PC layout defined in section 8.3, and Western Digital's standards for manufacturability.

8.2.1 RESISTORS - 1%

The 1% resistors shall conform to MIL-R-10509, except that the temperature tolerance shall not exceed +/- 100 ppm. Resistors are 1% metal film, 1/8 Watt.

8.2.2 CAPACITORS - CERAMIC

The general capacitor specifications are described in Sprague Engineering Bulletin # 6249, titled "PERFORMANCE CHARACTERISTICS - COG (NPO) Temperature Compensating", a copy of which is attached.

8.2.3 INDUCTOR

Requirements:	Value:	4.7 uH
	Tolerance:	+/-5%
	Self-resonant frequency:	>40 MHz
	Q	>40 @ 10 MHz
	DC resistance	<1.5 ohms
	DC rated current	>100 mA
	Inductance change/temperature	<1% over the range 0-50 deg C

8.2.4 FERRITE BEAD

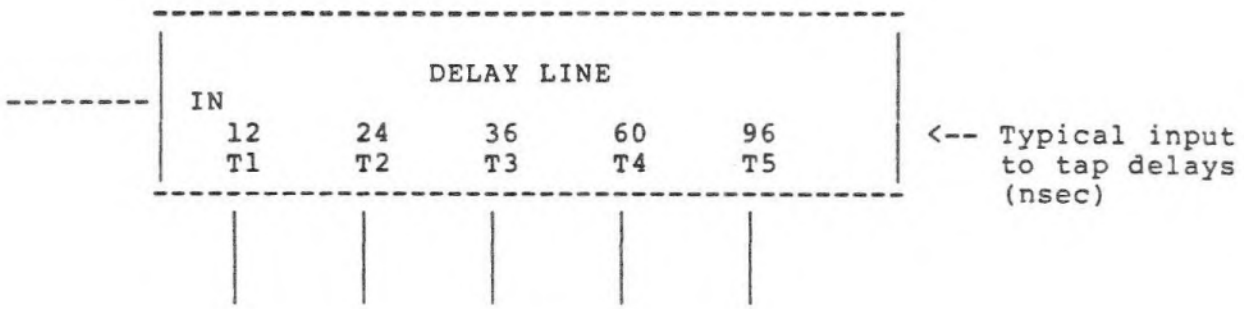
- Fair-Rite p/n 2743002122 or equivalent
- Impedance at 10 MHz > 10 ohms
- General impedance vs. frequency requirements, see Fair-Rite catalog, figure 4 "Parallel Resistance, Reactance and Impedance Per Air Core Inductance vs. Frequency", a copy of which is attached

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8.2.5 DELAY LINE

Attached is WD dwg # 39-002005-00. The following specifications apply in addition to those in that document.
All timings rising edge to rising edge unless specified otherwise.

The following specifications must be met over the ranges:
VCC = 4.75 to 5.25 volts; T = 0 to 60 deg C



ALL TIMES ARE IN NANOSECONDS

	RISING EDGE TO RISING EDGE DELAY MIN	RISING EDGE TO RISING EDGE DELAY MAX	INPUT PULSE WIDTH HIGH MIN	INPUT PULSE WIDTH HIGH MAX	RISING EDGE TO RISING EDGE INPUT PERIOD MIN	RISING EDGE TO RISING EDGE INPUT PERIOD MAX
IN to T4	57	63	104	IN TO T5 + 24	150	600
T1 to T4	43	53	104	IN TO T5 + 24	150	600
T1 to T2	9	15	104	IN TO T5 + 24	200	400
T2 to T3	9	15	104	IN TO T5 + 24	200	400
IN to T5	92	NOTE 1	104	IN TO T5 + 24	150	600

NOTE 1: The IN to T5 delay determines the maximum input pulse width, as can be seen above. When the maximum input pulse width high is applie to the IN pin every 150 nsec, the output pulse width low at the T1, T4, and T5 pins must be below .8 volts for at least 5 nsec. For instance, if the max delay from IN to T5 was 100 nsec, then the max pulse width applied to the IN pin would be 124 nsec. If the max delay is tighter, say 97 nsec, then the pulse width is 121 nsec, making it easier to meet the pulse width low criteria. The output pulse width at T4 must be at least 104 nsec. This requirement does not apply to the other output taps.

Since the 1020's delay increases with increasing temperature and decreasing voltage, it is an advantage for the delay line to have its delays decrease with increasing temperature and decreasing voltage.

8.2.6 VARACTOR

Attached is WD dwg # 32-001001-00. The following specifications apply in addition to those in that document.

1. Varactor capacitance vs. voltage curves must fall into the range shown in Figure 4 of the varactor document.

2. The varactor curve must not exhibit any discontinuities; it must be a smooth curve.

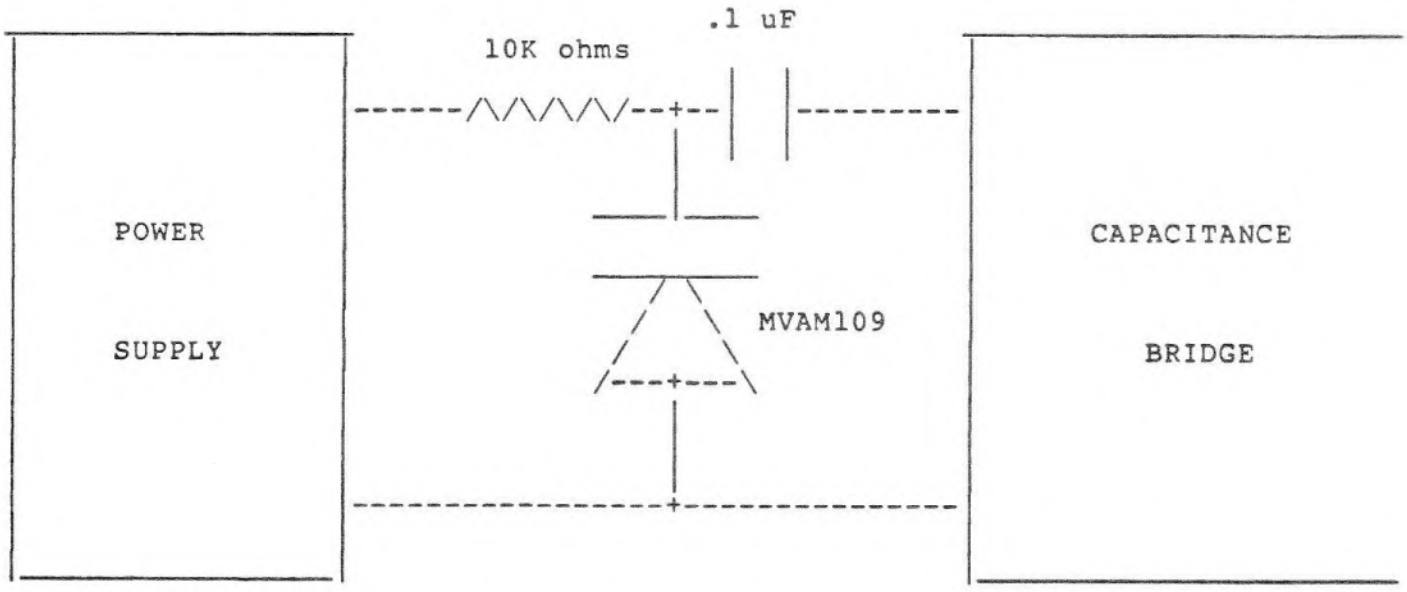
A minimum test is specified below:

1. VX = bias voltage at which the varactor capacitance = 70 pf

2. VX must be in the range 4.0 Volts <= VX <= 7.0 Volts

3. At a bias voltage of VX - 1.0 Volts, the varactor capacitance VC must be in the range 98 pf <= VC <= 150 pf

4. Test fixture requirements:



FREQUENCY = 10MHZ AMPLITUDE = 1 VOLT PEAK-TO-PEAK

TEST FIXTURE CAPACITANCE MUST BE <= 2 pf

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8.2.7 CRYSTAL

The crystal specification is contained in WD dwg # 33-000006-00, a copy of which is attached.

8.3 STANDARD PC LAYOUT AND APPLICATION RULES

The standard layout instructions are presently being placed in a document by Drafting. It will be attached when ready.

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8.4 PERFORMANCE SPECIFICATIONS

The following specifications apply with external components meeting their specifications, and over the folowing ranges:

VCC = 4.75 to 5.25 Volts with <= 100 mV ripple, 0 to 30 Khz

+12 = 10.8 to 13.2 Volts with <= 200 mV ripple, 0 to 30 Khz

Temp = 0 to 60 degrees C

8.4.1 PLL LOOP SPECIFICATIONS

Acquisition time	< 12.8 usec (16 usec from DRUN high)	
Capture range	> +/- 2.2 % (+/- 1% drive +/- .1% crystal osc)	
Jitter rejection	> 40 db @ 2.5 MHz	
Damping factor	min .7 typ 1 max 1.4	Velocity Lock
	min .5 typ .7 max 1.1	Phase Detectio
Kd Error Amplifier Gain (100 % duty cycle)	min 3.75 mA typ 6 mA max 10 mA	Velocity Lock operating range VSENSE +/- 1060 mV
	min 3 mA typ 4.5 mA max 7.5 mA	Phase Detection operating range VSENSE +/- 950 mV
Error Amplifier Balance Ratio	max 2:1	Phase Detection operating range VSENSE +/- 950 mV Phase: +/- 5 to +/- 40 nsec
Ko VCO Gain	min 4 typ 5 max 6 % per volt	
Drive Margin	min +/- 16 nsec, including defects precompensation turned off	

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8.4.1.2 FREQUENCY DETECTOR

DRUN must be high in response to RMFM rising edge to rising edge periods less than 250 nsec. DRUN must be low for periods greater than 300 nsec.

8.4.1.3 CRYSTAL OSCILLATOR

The operational frequency must be within +/- .1% of 10 MHz. At power on, the time from VCC passing 4.75 V until WCLK is within specification must be no longer than 5 msec.

8.4.1.4 PHASE DETECTOR/CHARGE PUMPS

8.4.1.4.1 PHASE DECISION POINTS

While in the phase detection mode, the phase difference from null (zero pump current) to the decision points must be no less than +/- 40 nsec.

8.4.1.4.2 PHASE ERROR DUE TO PUMP IMBALANCE

After acquisition has been completed, over the range of voltages on the PUMP pin: VSENSE nominal +/- 950 mV, and an RMFM (test) signal with 0 to 40 nsec of asymmetry, the center between the early and late signals with respect to null will not be more than +/- 3 nsec from the null phase. This is a realistic approximation of worst case phase error that can occur in drive data. It can be measured from the empirical current vs. phase plots.

8.4.1.5 VCO GAIN

Over the VCO input voltage range: VSENSE nominal +/- 1060 mV, the VCO gain shall be within the range 4% to 6% per volt. There must be no discontinuities in its characteristic V-F curve over the input voltage range.

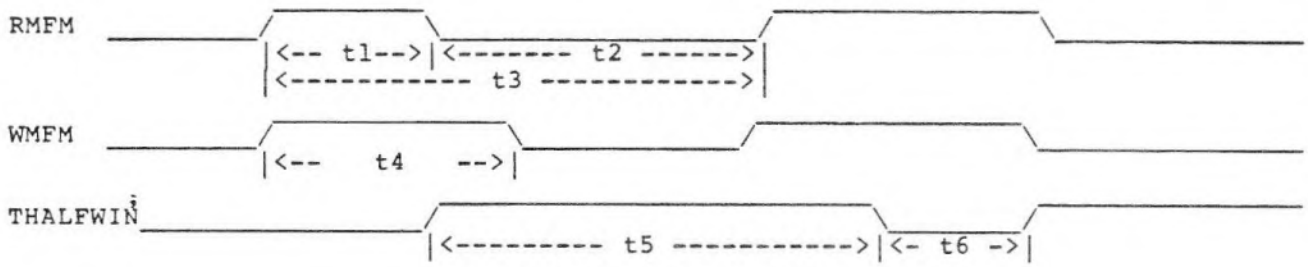
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8.4.2 TIMING SPECIFICATION

Timing on signals RDATA, RCLK, WCLK, and DRUN are measured at the voltage halfway between the 1010/2010's VIH & VIL: 2.55 Volts.
All other signals measured from the 1.4 V transitions.

8.4.2.1 DISK DRIVE READ AND WRITE DATA, PULSE FORMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
t1	RMFM PULSE WIDTH HIGH	20	150	nsec	
t2	RMFM PULSE WIDTH LOW	20	-	nsec	
t3	RMFM PERIOD	150	-	nsec	
t4	WMFM PULSE WIDTH HIGH	104	130	nsec	
t5	THALFWIN PULSE WIDTH HIGH	104	-	nsec	
t6	THALFWIN PULSE WIDTH LOW	5	-	nsec	any RMFM period; .8V leve

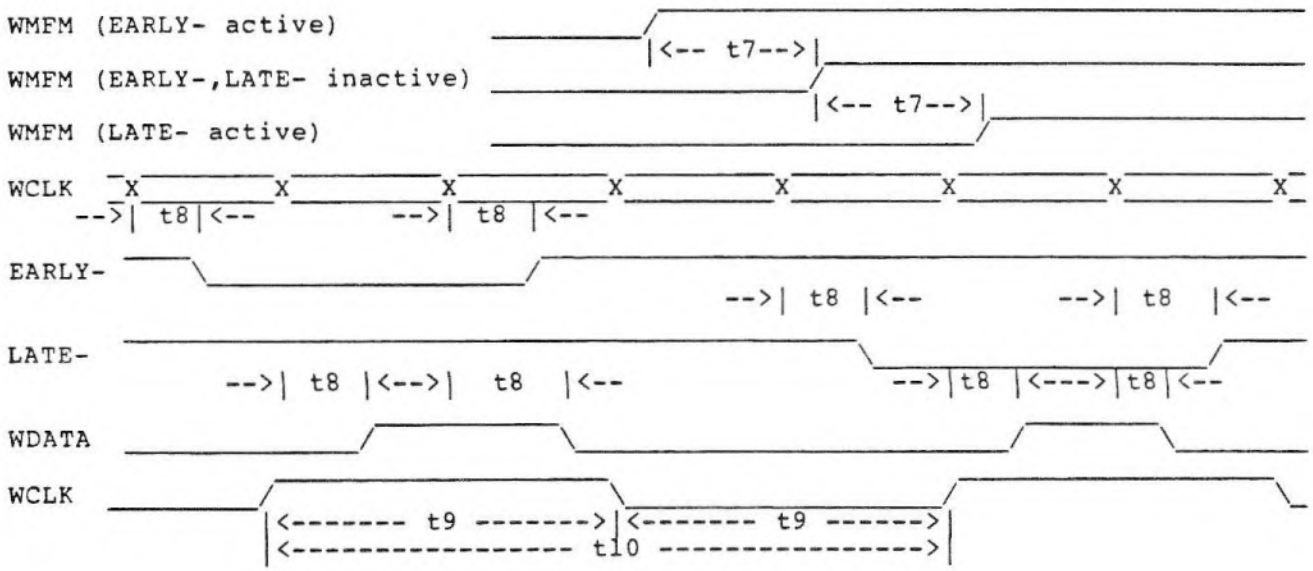


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8.4.2.2 WRITE PRECOMPENSATION

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
t7	WRITE PRECOMPENSATION DELTA	9	15	nsec	
t8	SETUP TIME: EITHER EDGE OF EARLY-,LATE-, OR WDATA TO EITHER EDGE OF WCLK	20	-	nsec	
t9	WCLK PULSE WIDTH	95	105	nsec	
t10	WCLK FREQUENCY			5 MHz +/- .1 %	



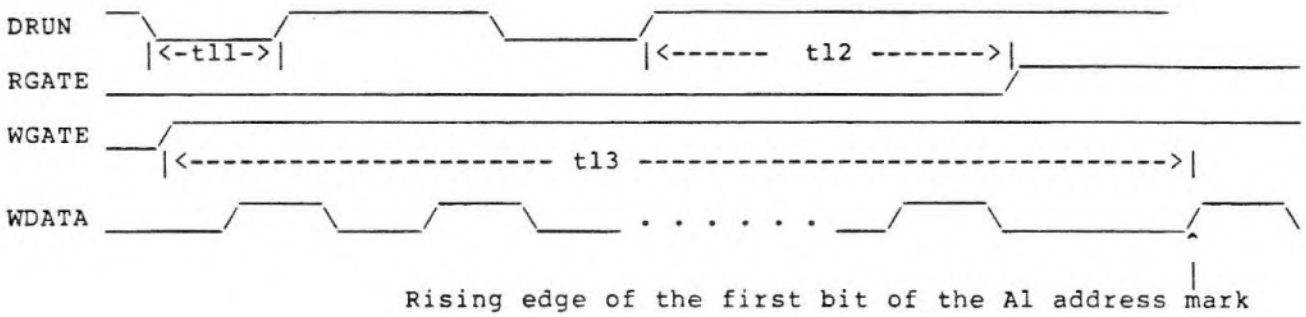
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.4.2.3 DRUN, RGATE, WGATE timing

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
t11	DRUN LOW PULSE WIDTH	30		nsec	note 3
t12	DRUN HIGH TO RGATE HIGH	0	32	bits	note 4
t13	WGATE HIGH TO 1ST ADR MARK BIT	92	-	bits	

note 3: No requirement on DRUN pulse width high.
note 4: During 1010/2010 read.



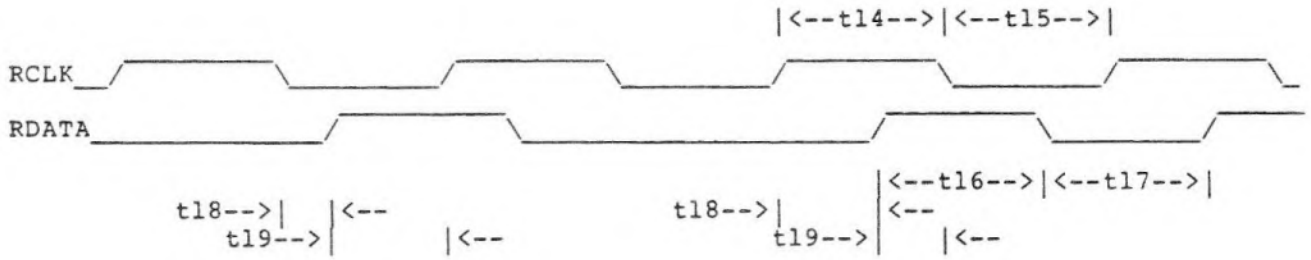
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8.4.2.4 RCLK, RDATA timing

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
t14	RCLK HIGH PULSE WIDTH	93	108	nsec	
t15	RCLK LOW PULSE WIDTH	93	108	nsec	
t16	RDATA HIGH PULSE WIDTH	93	108	nsec	
t17	RDATA LOW PULSE WIDTH	93	108	nsec	
t18	RCLK EDGE TO RDATA RISING EDGE	30		nsec	max is implicit in t19 mi
t19	RDATA RISING EDGE TO RCLK EDGE	30		nsec	max is implicit in t18 mi

t14 & t15 each define an MFM detection window. The rising edge of RDATA must occur within the proper window.
t14 + t15 = the current MFM bit cell time



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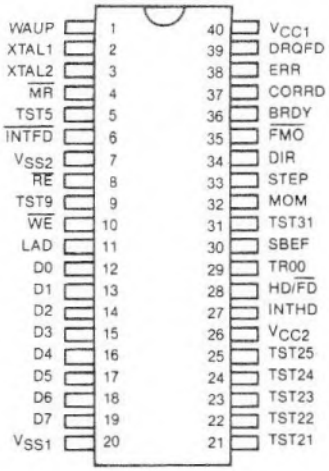
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ADVANCE INFORMATION

WD1015 Buffer Manager Control Processor

FEATURES

- SINGLE +5V POWER SUPPLY
- COMPLETE BUFFER MANAGER
- PROGRAMMABLE SECTOR SIZES — 128, 256, 512, OR 1024 BYTES
- ECC BURST ERROR CORRECTION UP TO 5 BITS ON HARD DISK DATA
- 8 BIT MULTIPLEXED ADDRESS/DATA I/O BUS
- FLOPPY DISK COMMAND TRANSLATION
- SUPPORTS MOTOR ON OR HEAD LOAD DRIVES
- SUPPORTS 250 OR 500 KBS FLOPPIES
- BUFFERED SEEKS WITH FLOPPIES AND WINCHESTERS
- 16 POPULAR STEPPING RATES AVAILABLE
- AUTOMATIC RETRIES ON ALL ERRORS WITH SIMULATED COMPLETION
- POWER-ON DIAGNOSTICS INCLUDED
- 10 MHZ CLOCK RATE
- 40 PIN DIP PACKAGE



PIN DESIGNATION

DESCRIPTION

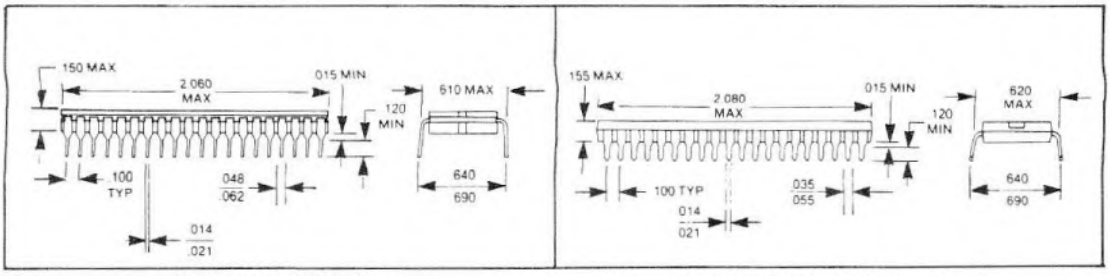
The WD1015 is a complete Control Processor (CP) that is used to handle all aspects of buffer management, in conjunction with the EDS (WD1014) device, for the Winchester/Floppy Controller board (WD1002-05). It executes all of the commands used by the WD1002-05 and does all of the control required except for real time processing, which is done by the WD1014. Throughout this specification this device will be referred to as the WD1015, or BMAC (buffer manager and controller), or simply as the CP (control processor). The WD1015 is programmed to control the transfer of information within the WFC and it maintains the necessary copies of the task files (TSF) found on both drives. Host access to the WFC causes the CP to access task file information in the TSF after a command is issued. Depending on the command, the CP will make the buffer accessible to the host or the WD1010 or 2797 controllers. The CP also controls the operation of the Error Correcting logic. During the transfer of data from the host to the WD1010, the EDS monitors the data bus, if so enabled, to compute a 4 byte ECC which is appended to the end of data transferred to the WD1010 and recorded on the disk. During data transfers from the WD1010 to the host the CP uses the ECC to validate the data. If data is corrupted the CP envokes recovery techniques such as retries and correction. A maximum of 8 retries are attempted if two consecutive syndromes do not match. Correction is attempted only if two consecutive syndromes match. If the error is uncorrectable, the operation is terminated. The CP is also used to handle data transfers from/to the SF for the floppy disk controller, which only uses CRC check bytes for its data fields. Two commands, RESTORE and SEEK, are directly executed by the CP rather than the WD2797 floppy disk controller. During status reads by the host, the CP consolidates the normal completion status from the WD1010, the WD2797 and the current EDS status into a form consistant with established WD1010 error reporting. This consolidated status is then presented to the host. The WD1015 is fabricated using HMOS technology and is available in a 40 pin DIP package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	WAKE-UP	WAUP	This input is used by the BMAC to poll a command from the host. The BUSY status bit is set immediately except in case of a WRITE/FORMAT command. In that case, WAUP and BUSY, are set only after the sector buffer has been filled by the host. WAUP is reset when the command has been executed.
2	CRYSTAL 1	XTAL1	One side of crystal input for internal oscillator. Also input for external source.
3	CRYSTAL 2	XTAL2	Other side of crystal/external source input. Frequency should be 10 MHz.
4	MASTER RESET	$\overline{MR}$	This input is used to initialize the internal logic of the processor.
5	TEST 5	TST5	This input is to be left open by the user. Internal pullup — 300K ohm.
6	FLOPPY DISK INTERRUPT	$\overline{INTFD}$	Initiates an interrupt if interrupt is enabled; disabled on reset.
7	V_{SS2}	V_{SS2}	This input is to be left open by the user. Internal pullup — 10M ohm.
8	READ ENABLE	$\overline{RE}$	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.
9	TEST 9	$\overline{TST9}$	This output is left open by the user.
10	WRITE	$\overline{WE}$	Output strobe during a BUS write. Used as write strobe to an external device. Signifies that valid data has been put on the BUS.
11	ADDRESS LATCH	LAD	This output signal occurs once during each instruction cycle. The negative edge of LAD strobes address into an external latch, used to communicate to the WD1010, WD2797, and the WD1014 chips.
12-19	DATA BUS	D7-D0	True I/O bidirectional BUS which can be written to or read synchronously using $\overline{RE}$, $\overline{WE}$, strobes. Also contains the address and data during an external acess to/from port devices, under control of LAD, $\overline{RE}$, and $\overline{WE}$.
20	GROUND	V_{SS1}	Ground.
21-25	TEST 21-25	TST21-25	Unused pins to be left open by the user.
26	V_{CC2}	V_{CC2}	+5V during operation.
27	HARD DISK INTERRUPT	INTHD	This input is polled to sense an interrupt from the WD1010, indicating completion of command issued to it by the BMAC.
28	HARD DISK/FLOPPY DISK	HD/$\overline{FD}$	This input is used to sense hard disk operation when high, and floppy disk operation when low.
29	TRACK 00	TR00	This input indicates that the R/$\overline{W}$ heads of the selected floppy drive are positioned over the outermost cylinder.
30	SECTOR BUFFER EMPTY/FULL	SBEF	This input to the BMAC is set high whenever a sector of data has been written to or read from the sector buffer.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	TEST 31	TST31	Normally left open by the user.
32	MOTOR MODE	MOM	Input used to select motor-on or head load timings for floppies. This line should be left open for motor-on type drives such as the mini floppies. A delay of 1 second will be observed before $\overline{FMO}$ is activated. For head load type drives like the standard floppies, this input should be grounded. A delay of 40 mS, will be observed before $\overline{FMO}$ is activated, thereby improving the overall performance when accessing the floppies.
33	STEP	STEP	The STEP output is pulsed once for each cylinder to be stepped on the floppies. The step pulse period is normally determined by the stepping rate selected. On a RESTORE for the floppies, however, a stepping rate of 8 mS, is used if the specified stepping rate is faster than 8 mS.
34	DIRECTION	DIR	This output is used by the floppy drive to determine the direction of a seek operation. A low defines direction as out and a high specifies direction as in.
35	FLOPPY MOTOR-ON	$\overline{FMO}$	This output is used to turn the motor on, on all floppy drives supported by the WD1002 WFC board. The drives must be configured such that the heads are loaded when this signal is activated. When the floppies are being accessed for the first time, a delay as determined by MOM, is observed before activating $\overline{FMO}$. Motor on is turned off after — 3 seconds, if no further floppy accesses are made.
36	BUFFER READY	BRDY	This output signal indicates the sector buffer is ready to be accessed by an external device such as the WD1010.
37	CORRECTED DATA	CORRD	This output status indicates to the host that the BMAC has successfully corrected a data error in the data buffer, at least once. To determine if more than one correction has taken place during a multisector read, each sector specified must be reread by the host on an individual basis.
38	ERROR	ERR	Output status bit indicates that the BMAC encountered an error during the execution of a command. The error reg, on the WFC board must be read by the host to determine the type of error that occurred.
39	DATA REQUEST	DRQFD	This input indicates to the BMAC that the WD2797 has a byte of data available to be read from the disk, or requires a byte of data to be written to the floppy disk.
40	V_{CC1}	V_{CC1}	Main power supply. +5V +/−5%

Package Diagrams



40 LEAD CERDIP "CL" **40 LEAD PLASTIC "P" or "PL"**

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WD1015-14 SPECIFICATION

1.0 Introduction

The WD1015-14 is a complete control processor that is used to handle buffer management in conjunction with the ECC (WD1100-13) and winchester controller (WD1010) devices for the Winchester controller board (WD1002-HYP). It decodes and executes all of the SASI commands used by the WD1002-HYP and does all of the control required. Throughout this specification this device will be refered to as the WD1015-HYP, or BMAC (buffer manager and controller), or simply as the CP (control processor).

The CP also performs the operation of Error Correction. During the transfer of data from the host to the WD1010, the WD1100-13 monitors the data bus, to compute a 4 byte ECC (if so enabled), which is appended to the end of data transferred to the WD1010 and recorded on the disk. During data transfers from the WD1010 to the host the CP uses the ECC to validate the data. If data is corrupted the CP envokes recovery techniques such as retries and correction. A maximum of 8 retries are attempted if two consecutive syndromes do not match. Correction is attempted only if, two consecutive syndromes match when an error exists. If the error is uncorrectable, the operation is terminated.

During status reported back to the host, the CP consolidates the normal completion status from the WD1010 and the current ECC device status into a form consistant with established error reporting for SASI protocol. This consolidated status is then presented to the host. If an error existed the host is required to send the request status command to the controller.

The WD1015-14 is fabricated using HMOS technology, and is available in a 40 pin DIP package.

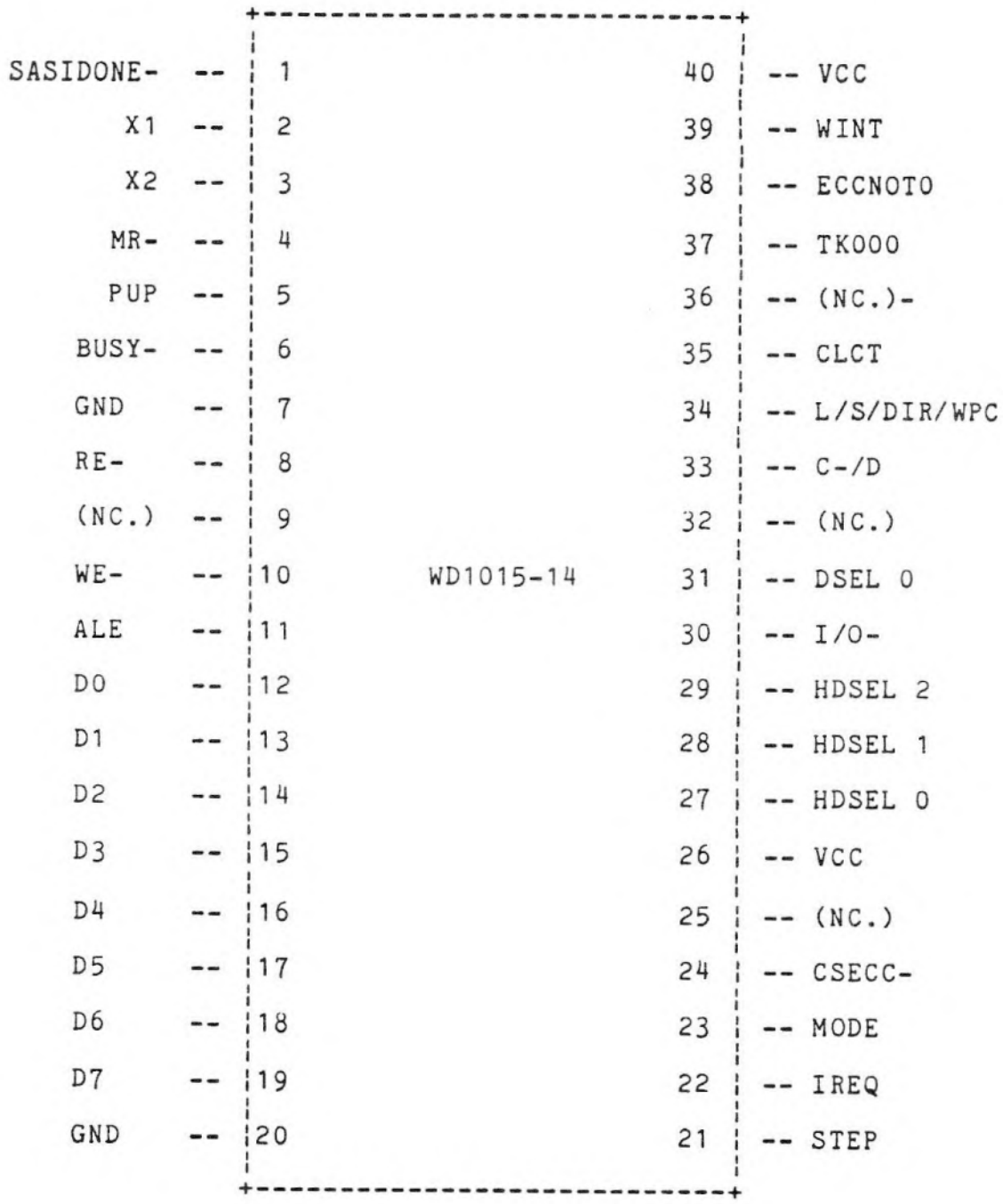
2.0 Reference Documents

	Description / Title	Document Num. / Source
1.	WD1002-HYP Engineering (product) Specs.	61-031111-0003
2.	WD1015-02 Source listing	29-000049-0120

3.0 WD1015-14 Features

* Single +5V power supply
* buffer manager
* 512 byte sectors
* ECC burst error correction up to 11 bits
* SASI command translation
* Buffered seeks
* 6 step rates plus Seagate 1/2 step
* Supports programmable retries on errors
* Self test diagnostics included
* 5 MHZ clock rate
* Implied seeks on all commands
* Supports overlapped seeks
* Controls read/write head selects

4.0 Pinouts


SASIDONE- -- 1
X1 -- 2
X2 -- 3
MR- -- 4
PUP -- 5
BUSY- -- 6
GND -- 7
RE- -- 8
(NC.) -- 9
WE- -- 10
ALE -- 11
D0 -- 12
D1 -- 13
D2 -- 14
D3 -- 15
D4 -- 16
D5 -- 17
D6 -- 18
D7 -- 19
GND -- 20
WD1015-14
40 -- VCC
39 -- WINT
38 -- ECCNOTO
37 -- TK000
36 -- (NC.)-
35 -- CLCT
34 -- L/S/DIR/WPC
33 -- C-/D
32 -- (NC.)
31 -- DSEL 0
30 -- I/O-
29 -- HDSEL 2
28 -- HDSEL 1
27 -- HDSEL 0
26 -- VCC
25 -- (NC.)
24 -- CSECC-
23 -- MODE
22 -- IREQ
21 -- STEP

4.1 Pin Description

PIN	SYMBOL	NAME	FUNCTION
1	SASIDONE	SASI DONE	Indicates that the last SASI bus operation is complete and precipitates an IREQ.
2	X1	CRYSTAL 1	One side of crystal input for internal oscillator. Also input for external source.
3	X2	CRYSTAL 2	Other side of crystal/external source input. Frequency should be 5 MHz.
4	MR-	MASTER RESET	This input is used to init. the internal logic of the processor. The diagnostic TEST routine is also executed.
5	PUP	PULL-UP	This input is pulled up through a 1K resistor.
6	BUSY-	BUSY	This input indicates that the controller is busy
7	GND	GROUND	This input should be grounded by the user in the present application.
8	RE-	READ ENABLE	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.
9	TST3	TEST 3	This output is to left open by the user.
10	WR-	WRITE	Output strobe during a BUS write. Used as write strobe to an external device. Signifies that valid data has been put on the BUS.
11	ALE	ADDRESS LATCH ENABLE	This output signal occurs once during each instuction cycle. The negative edge of ALE strobes address into an external decode latch, used to communicate to the WD1010, WD1100-13, RAM and the state

			sequencer.
19-12	D7-D0	DATA BUS	True I/O bidirectional BUS which can be written to or read synchronously using RE-, WE-, strobes. Also contains the address and data during an external access to/from port devices, under control of ALE, RE-, and WE-.
20	GND	GROUND	Ground.
21	STEP	STEP	This output controls the step pulses to the Winchester disk drive.
22	IREQ	INTERRUPT REQUEST	This output indicates that the controller is ready fro the next operation.
23	MODE	MODE	This output selects the diagnostic Long mode of the ECC device (WD1100-13)
24	CSECC-	ECC CHIP SELECT	This output selects the Ecc device for operation. (WD1100-13)
25	TST4	TEST 4	This input is left open by the user.
26	VCC	+5V	+5 volts
27	HDSEL 0	HEAD SELECT 0	This output selects head 0 of the Winchester disk drive.
28	HDSEL 1	HEAD SELECT 1	This ouput selects head 1 of the Winchester disk drive.
29	HDSEL 2	HEADD SELECT 2	This output selects head 2 of the Winchester disk drive.
30	I/O-	INPUT/OUTPUT	This output is a SASI bus signal that indicates direction of transfer.
31	DSEL0	DRIVE SELECT 0	This output selects drive 0
32	TST5	TEST 5	This output is left open by the user.
33	C-/D	COMMAND/DATA	This output is A SASI signal

			which indicates type of data to transfer. Command or Data. the user.
34	L/S/DIR/WPC	LONG/SHORT DIRECTION/ WRITE PORT CONTROL	This output is dual function. It controls the direction of head movement on the Winchester disk drive and extends the data transfer four bytes for ECC operation.
35	CLCT	CLEAR COUNTER	A high level at this output will clear the lower Ram address counter.
36	N.C.	No connection	This output should be left open by the user.
37	TK000	TRACK 0	This input set high indicate that the drive is at track 0.
38	ECCNOT0	ECC NOT 0	This input set high after a sector read, indicates an ECC error has occurred.
39	WINT	WINCHESTER INTERRUPT	A high level is provided to this input from the WD1010 upon completion of a command.
40	VCC	+5V	Main power supply. +5V +/- 10%

5.0 BMAC Functional Description

The WD1015-14 microcomputer contains the following functions in a single 40 pin package:

8-bit CPU
4K x 8 ROM Program Memory
256 x 8 RAM Data Memory
8-bit I/O Data / Address BUS
19 Signal Control Lines
8-bit Timer / Event Counter
8 Level Stack
2 Working Register Banks

The WD1015-14 was specifically designed to serve as a control processor for the (WD1002-HYP) board. The internal ROM program memory is programmed to decode and execute SASI commands.

The detailed internal architecture and the instruction set are described in the CPU component specification indicated in the references.

5.1 Command Execution

When power is first applied, the MR- input (pin 4), must be strobed to ensure proper initialization of all internal logic. The BMAC is continiously executing self test after POR and MR. While polling for BUSY-. The BMAC will prepare to receive a command. After a command is received this will actually start the six byte SASI command transfer to the controller. Once all six bytes have been transfered the state BMAC sends SASID (SASIDONE) to the Host. The BMAC then will extract these six bytes from the RAM and decode and execute the command. Once the command has been executed the BMAC will send the Completion status byte and one byte of zeroes to the host. The BMAC will activate the I-/O (Input-to the-host), C-/D (Command/Data) lines. For a detailed description of the command flow refer to the source listing.

5.2 Clock and Timing Circuits

Timing generation for the WD1015-14 is completely self-contained with the exception of a frequency reference which can be XTAL, inductor, or external clock source. For the current application, a 5 MHZ crystal derived clock frequency is used. Hence the cycle time for instruction execution is 3.0 u.s. Most instructions require 2 cycle times for execution.

5.3 Master Reset

The MR- input provides a means for initialization for the processor. The MR- must be held at ground (.5V) for at least 10 m.s. after the power supply is within tolerance. Only 5 machine cycles are required if power is already on and the oscillator has stabilized.

MR- performs the following functions:

3. Sets program counter to zero.
4. Sets stack pointer to zero.
5. Selects register bank 0.
6. Selects memory bank 0.
7. Sets BUS to high impedance state.
8. Sets all I/O lines to input mode
9. Disables timer and external interrupts.
10. Stops timer and clears timer flag.
11. Clears flags F0 and F1.
12. All internal registers are set to their default values (see listing)

6.0 SPECIFICATIONS

6.1 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias.....0o C to 70o C
Storage Temperature.....-65o C to +150o C
Voltage on any pin with respect to V_{SS}.....-0.2 V to + 7.0 V
Power dissipation.....1.5 Watt

NOTE 4: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics T_A = 0 deg. C to 70 deg. C
VCC = +5V +/- 10%, VSS = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
VIL	Input Low Voltage	-0.5		0.8	V	All except MR-,X1,X2
VIL1	Input Low Voltage	-0.5		0.6	V	For MR-, X1, X2
VIH	Input High Voltage	2.0		VCC	V	All except MR-,X1,X2
VIH1	Input High Voltage	3.8		VCC	V	For MR-, X1, X2
VOL	Output Low Voltage BUS			.45	V	IOL = 2.0 mA
VOL1	Output Low Voltage RE, WE, ALE, TST3			.45	V	IOL = 1.8 mA
VOL2	Output Low Voltage TST4			.45	V	IOL = 1.0 mA
VOL3	Output Low Voltage All other outputs			.45	V	IOL = 1.6 mA
VOH	Output High Voltage BUS	2.4			V	IOH = -400 uA
VOH1	Output High Voltage RE, WE, LAD, TST3	2.4			V	IOH = -100 uA
VOH2	Output High Voltage All other outputs	2.4			V	IOH = - 40 uA

DC Characteristics Cont.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{IL}	Input leakage curr WINT, TST2			+/-10	uA	$V_{SS} < V_{IN} < V_{CC}$
I_{IL1}	Input leakage curr pins 21-24,27-38,7,5			-500	uA	$V_{SS}+.45 < V_{IN} < V_{CC}$
I_{OL}	Output leakage curr BUS to HI impedance			+/-10	uA	$V_{SS}+.45 < V_{IN} < V_{CC}$
I_{DD}	Vcc2 supply current		5	10	mA	
$I_{CC} + I_{DD}$	Supply Current		50	110	mA	All outputs open

6.2 AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
t_{CY}	Cycle Time	3.0			uS	
t_{LL}	ALE pulse width	530			nS	
t_{AL}	Address setup to ALE	490			nS	
t_{LA}	Addr. hold from ALE	160			nS	
t_{RW}	RE-/WE- Pulsewidth	1300			nS	
t_{DW}	Data setup before WE	1100			nS	
t_{WD}	Data Hold after WE-	450			nS	
t_{DR}	Data hold from RE-	0		270	nS	
t_{RD}	RE- to data in			1000	nS	
t_{AW}	Addr setup to WE-	1050			nS	
t_{AD}	Addr setup to data			2050	nS	read ext. data
t_{AFC}	Addr float to RE,WE	360			nS	
t_{LAFC}	ALE to RE,WE	525			nS	
t_{CA}	RE, WE to ALE	160			nS	

ENGINEERING SPECIFICATION
WX2 GATE ARRAY
WD11C00-17

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1. GENERAL DESCRIPTION

The WX2 Logic Array incorporates numerous functions in one j-leaded 68 pin surface mountable package. It was designed in an effort to cost reduce the WD1002-WX2 disk controller by combining random logic and specialized circuits into one chip. The following list shows the functions that have been incorporated:

1.1) Status Ports

1.2) Read/Write Ports

1.3) Sector Buffer Control

1.4) Disk I/O Control

1.5) ECC

1.6) Reset Timing

The Array interfaces directly to the host data bus via bi-directional high current bus drivers on the D0-D7 pins and high current drivers on DRQ3, IRQ5 pins. Schmitt trigger inputs ensure noise reduction on bus imput pins A0, A1, DACK3-, IOR-, IOW-, RESET.

3 micron C-MOS technology provides for low power consumption and high switching speed.

2. PART IDENTIFICATION

Western Digital Part Number is 62-003004-003

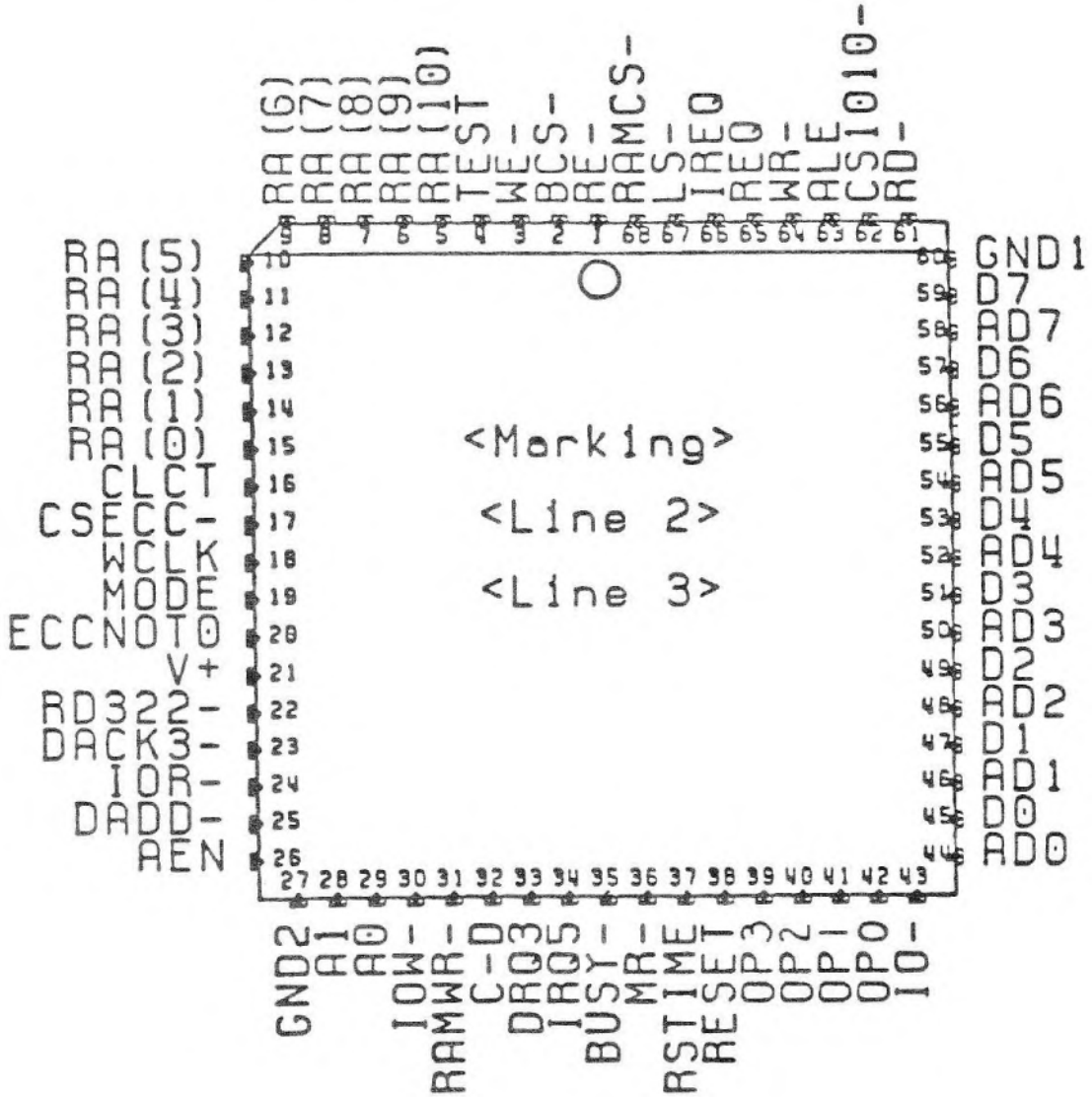
Western Digital Model Number is WD11C00JT-17

Vendor Part Number (Array Technology) is AT-DHS-1050

2.1 RELATED DOCUMENTS

TTL schematic WX2 Gate Array	68-000039
Detailed Schematic WX2 Gate Array	68-000040

3. PIN DESIGNATION



4. PIN DESCRIPTION

PIN #	SYMBOL	PIN NAME	FUNCTION
1	RE-	Read Enable	INPUT when BCS- is low, read strobe Bidirectional, for ECC function. OUTPUT when BCS- is high, follows RD- Pin 61.
2	BCS-	Buffer Chip Select	INPUT active low when WD1010 reads or writes sector buffer, enables RE- Pin 1 and WE- Pin 3 as inputs when low, outputs when high.
3	WE-	Write Enable	INPUT when BCS- is low, write strobe for ECC function Bidirectional, OUTPUT when BCS- is high, follows WR- Pin 64.
4	TEST	Test	INPUT active high, used for test only, controls state of internal RA10 (End of Data) during ECC test. TEST=LOW DATA TEST=HIGH END OF DATA (GENERATE ECC)
5-15	RA10-RAO	Ram Address	OUTPUTS active high, address sector buffer RAM and WD1010.
16	CLCT	Clear Count	INPUT active high clears lower RAM address counter outputs RA -RA7.
17	CSECC-	Chip Select ECC	INPUT active low enables the ECC function.
18	WCLK	Write Clock	INPUT 5 MHz clock for the ECC function.

PIN #	SYMBOL	PIN NAME	FUNCTION
19	MODE	Mode	INPUT when high selects normal mode of the ECC function. (i.e. check bytes are generated after end of data) When low selects the long mode and inhibits the preset function of the ECC logic. (i.e. check bytes are not generated after end of data and logic passes check bytes transparently from host to disk)
20	ECC NOT O	ECC NOT ZERO	OUTPUT active high indicates to WD1015 that an error has been detected while comparing the check bytes at the end of the data stream with the check bytes generated internally.
21	VCC	+5V DC	INPUT supply voltage.
22	RD322-	Read Port 322	OUTPUT active low when host reads status port 322.
23	DACK3-	DMA Acknowledge 3	INPUT active low acknowledges DMA request 3 (DRQ 3).
24	IOR	I/O Read	INPUT active low enables data onto the DO-D7 outputs when host wants to read data or status.
25	DADD-	Device Address Code	INPUT active low when address 320 or 324 is present on the host address bus.

PIN #	SYMBOL	PIN NAME	FUNCTION
26	AEN	Address Enable	INPUT active high indicates that the DMA controller (Host) has control over the Bus, de-gates host processor and other devices from the I/O channel. Used to enable Host to Disk I/O functions.
27	GND	Ground	GROUND
28	A1	Address Bit 1	INPUT active high when host assorts A1 to high state, used to enable Host to Disk I/O functions.
29	A0	Address Bit 0	INPUT active high when host asserts A0 to high state, used to enable Host to Disk I/O functions.
30	IOW-	I/O Write	INPUT active low strobes data from the Data Bus into internal devices or into the sector buffer RAM when host performs a write function.
31	RAMWR-	Ram Write	OUTPUT active low when either Host, WD1010 or WD1015 want to write to the sector buffer RAM.
32	$\overline{C}$/D	Control/Data	INPUT when low indicates that controller expects either a command or status block transfer, when high indicates that controller expects a data block transfer. Used to enable Disk I/O control section.

PIN #	SYMBOL	PIN NAME	FUNCTION
33	DRQ3	DMA REQUEST 3	OUTPUT active high requests DMA service from the Host, remains high until DACK 3- goes low. Asserted when controller is ready to accept data or data is ready to be read.
34	IRQ5	Interrupt Request 5	OUTPUT active high signals to the Host that service is required, remains high until Host interrupt service routine resets it. Activated when controller has completed a disk operation.
35	BUSY-	Busy	OUTPUT active low indicates that the Host has selected the controller and is about to perform an I/O operation, thus the controller is busy and can not accept another command.
36	MR-	Master Reset	BIDIRECTIONAL input active low when external power up reset detects dropping VCO level, clears all internal registers. OUTPUT active low when Host either performs a soft reset or a hardware reset from the bus is detected via the RESET Pin-38.
37	RSTIME	Reset Time	INPUT threshold adjust for the duration of the MR- Pin 36 active low time.

PIN #	SYMBOL	PIN NAME	FUNCTION
38	RESET	RESET	INPUT active high when Host performs a bus reset, clears all internal registers and activates MR- Pin 36 to activate low.
39-42	OP0,1,2,3	Option 0,1,2,3	INPUTS normally high via internal pull up resistors, can be activated low by applying GND to the input. Disk configuration readable on on Data Bus by Host via status read to port 322. OP0 - D0 OP1 - D1 OP2 - D2 OP3 - D3
43	I/$\overline{O}$	Input/Output	INPUT controls direction of internal data bus buffer from Host's point of view. When High = Input to Host, the ADX bus is driven onto the DX bus. When Low = Output from Host, the DX bus is received and driven to the ADX bus.
44, 46 48, 50 52, 54 56, 58	AD0-AD7	Address/Data Bus	BIDIRECTIONAL BUS carries Address information to internal RAM address counter and control de-multiplexer. Carries data to and from internal ECC function and external Sector Buffer RAM.

PIN #	SYMBOL	PIN NAME	FUNCTION
45	D0	Data Bus 0	BIDIRECTIONAL BUS interfaces controller to Host data bus.
47	D1	Data Bus 1	
49	D2	Data Bus 2	
51	D3	Data Bus 3	
53	D4	Data Bus 4	
55	D5	Data Bus 5	
57	D6	Data Bus 6	
59	D7	Data Bus 7	
60	GND	GND	GROUND
61	RD-	Read	INPUT active low when WD1015 performs a read operation.
62	CS1010-	Chip Select 1010	OUTPUT active low when WD1015 performs a read or write operation.
63	ALE	Address Latch Enable	INPUT active high when WD1015 asserts ALE used internally to select and latch the control de-multiplexer.
64	WR-	Write	INPUT active low when WD1015 performs a write operation.
65	REQ	Request	OUTPUT active high indicates to the Host that the controller is ready to accept data from or transfer data to the Host. Handshake signal for transfers between Host and Controller. The state of this output is read on D0 by the Host via a status read to Port 321.
66	IREQ	Interrupt Request	OUTPUT when aserted high it enables long/short mode when it is low it indicates to the 1015 and to the Host that the operation is complete.

67	LS/DIR/WPC	Long/Short/ Direction/ Write Reduced	INPUT when this signal is high during Host-Controller transfer the controller is in the long mode (Data Transfer). When this signal is low during Host-Controller transfer the controller is in short mode (command transfer). During 1010-Disk operation this signal provides direction for head movement and also indicates that write precompensation is enabled when low.
68	RAMCS-	RAM Chip Select	OUTPUT active low enables external Sector Buffer RAM for read/write operations by Host, WD1015 or WD1010

5. AC/DC Specification

Absolute maximmum ratings
DC supply-voltage range V_{DD} (referenced to V_{SS}): -0.5 to 7.0V

Input voltage range, all inputs: V_{SS} - 0.5 to V_{DD} + 0.5V

Specified operating range
V_{SS} = 0V, V_{DD} = 5V 10% $\pm$ 0 $\leq$ TA $\leq$ 70° C

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
V_{IL}	TTL Low Level Input Voltage	Pins: 1,2,3,4,16, 17,18,19,25,32,39, 40,41,42,43,44,46, 48,50,52,54,56,58, 61,63,64,66,67			0.8	Volts
V_{IH}	TTL High Level Input Voltage	Pins: (same as V_{IL})	2.4			Volts
V_{IL}	Schmitt Threshold Voltage Low	Pins: 23,24,26,28, 29,30,37,38,45,47, 49,51,53,55,57,59	0.9			Volts
V_{TH}	Schmitt Threshold	Pins: (same as V_{TL})			2.4	Volts
V_{HY}	(HI)	"" "" "" ""	0.35			Volts
I_{OL}	Low Level Output Current	V_{OL}=0.4V.	5.0			mA
	Single Buffer	Pins: 5,6,7,8,9,10 11,12,13,14,15,20, 22,31,35,62,65,68				
	Tri-state Single Buffer	Pins: 44,46,48,50, 52,54,56,58	5.0			mA
	Tri-state Double Buffer	Pins: 1,3,33,34,45 47,49,51,53,55	10.0			mA
	Open Drain N-Channel	Pins: 36,37	5.0			mA
I_{OH}	High Level Output Current	V_{OH}=2.4V.				
	Single Buffer	Pins: (same as I_{OL})	-5.0			mA
	Tri-state Single Buffer	Pins: (same as I_{OL})	-5.0			
	Tri-state Double Buffer	Pins: (same as I_{OL})	-10.0			mA
I_{DD}	Supply Current				15	mA
I_I	Input Leakage	Vin=0 or 5.5V	-10.0			µA
I_Z	Tri-State Leakage	Vo=0 or 5.5V	-10.0		10	µA

PROPAGATION DELAYS

From		To	Time(nS)	Comments
WCLK-	+clk	ECCNOTO- valid	25.3	only on bad ecc
RD-	true	AD0 - AD7 valid	52.6	reading out ecc
REQ	+clk	IRQ5- true	16.0	
IOW-	+clk	IRQ5- false	32.3	
IREQ	true	DRQ3- true	19.2	
DACK3-	true	DRQ3- false	33.4	
RA3/RA10	true	DRQ3- false		
IREQ	true	REQ true	13.0	
RA3/RA10	true	REQ false	9.0	
RD-/WR-	+clk	RA3 stable	44.6	from clock to RA10
RD-/WR-	+clk	RA9 stable	49.0	from clock to RA10
RD-/WR-	+clk	RA10 stable	59.0	from clock to RA10
IOW-	true	BUSY- true	34.5	Write to port 322
IOR-	true	BUSY- false	37.0	Read port 322
RESET	true	BUSY- false		
RD-/WR-	true	CS1010- true	21.1	
RD-/WR-	false	CS1010- false	16.4	
IOW-	true	MR- true	39.0	
RESET	true	MR- true	47.0	
R=1.3M C=2200pf		MR- width	1.42 mS	
R=12K C=2200pf		MR- width	13.0 uS	
IOW-	true	AD0-AD7 high to low	47.3	enable to valid
IOW-	true	AD0-AD7 low to high	53.6	enable to valid
IOW-	false	AD0-AD7 float	53.0	disable to float
D0-D7	inputs	AD0-AD7 stable	27.1	thru prop delay
IOR-	true	D0 - D7 stable	50.5	enable to valid
IOR-	false	D0 - D7 float	30.0	disable to float
AD0-AD7	inputs	D0 - D7 stable	27.1	thru prop delay
IOW-	true	RAMWR- true	27.0	
IOW-	false	RAMWR- false	27.1	
WE-	true	RAMWR- true	18.2	
WE-	false	RAMWR- false	22.1	

NOTE: This timing information is preliminary and will be updated when the appropriate adjustment factors guaranteeing the timing over the wafer process are available.

From		To	Time(nS)	Comments
RD-/WR-	true	RAMWR- true	34.2	
RD-/WR-	false	RAMWR- false	35.2	
WR-	true	WE- true	19.6	
WR-	false	WE- false	15.6	
RD-	true	RE- true	18.2	
RD-	false	RE- false	14.3	
IOR-	true	RD322- true	23.2	
IOR-	false	RD322- false	18.1	
IOR-/IOW-	true	RAMCS- true	27.2	
IOR-/IOW-	false	RAMCS- false	28.0	

Legend:

nS = nanoseconds
uS = microseconds
mS = milliseconds
signal- = low-true signal because of dash (-) following label
+clk = delay is from clock of flip-flop by rising edge of this signal
-clk = delay is from clock of flip-flop by falling edge of this signal
true = signal is asserted: low if low-true, high if high-true
false = signal is de-asserted: high if low-true, low if high-true

S E T U P A N D H O L D T I M E S

Typical times (Worst case times divided by 1.3)
NOTE: This includes dividing flip-flop setup and hold times by 1.3

Clock to FF	Data Input	Setup	Hold
IOW-	D0 or D1 data, create DMAEN-	-0.6	11.4
RD-/WR-	AD1 - AD3 data, load RA8 - RA10	-14.8	25.6
ALE	AD5 - AD7 data, decoder 1 of 8	7.7	3.5
IOR-	C/D- or I/O- data, cir BUSY	3.2	8.0
IOR-/IOW	C-/D or I/O- data, clock BUSY	5.6	7.2
RD-/WR-	AD0-AD7 data, byte to ECC reg.	0.3	10.9
WCLK	RD-/WR- data, 1st - 2nd ECC clk	17.0	-5.8

WCLK frequency and symmetry
WCLK period = 200 nS +/- 10 nS
WCLK high time = 100 nS +/- 10 nS
WCLK low time = 100 nS +/- 10 nS

Worst case 80 degree C times:

Clock to FF	Data Input	Setup	Hold
IOW-	D0 or D1 data, create DMAEN-	-0.9	14.9
RD-/WR-	AD1 - AD3 data, load RA8 - RA10	-9.4	33.0
ALE	AD5 - AD7 data, decoder 1 of 8	10.1	3.9
IOR-	C/D- or I/O- data,	4.2	9.8
IOR-/IOW-	C-/D or I/O- data,	7.2	8.8
RD-/WR-	AD0-AD7 data,	0.5	13.5
WCLK	RD-/WR- data,	22.2	-8.2

WCLK frequency and symmetry
WCLK period = 200 nS +/- 10 nS
WCLK high time = 100 nS +/- 10 nS
WCLK low time = 100 nS +/- 10 nS

```
Setup and hold path:  1,2
Name of path:         IOW- clock, D0 or D1 data, create DMAEN-

path IOW- LH to FF clock input:

gate    output  delay
IP      LH      0.4 +          =   0.4
STP     HL      1.8 + .2 * 1 =   2.0
I1      LH      1.8 + .3 * 1 =   2.1
I1      HL      1.6 + .2 * 5 =   2.6
NA4     LH      3.1 + .3 * 1 =   3.4
I1      HL      1.6 + .2 * 1 =   1.8
I1      LH      1.8 + .3 * 5 =   3.3
I1      HL      1.6 + .2 * 1 =   1.8
                              ------
                        total   17.4 nS

path DI(0) or DI(1):
Clock to FF     Data Input
STP     HL      1.6 + .2 * 1 =   1.8
I2      LH      1.8 + .3 * 3 =   2.7
                              -------
                        total     4.5 nS

WC Setup time = 17.4 - 4.5 = 12.9, 12.0 - 12.9 = -0.9 nS
WC Hold time  = 17.4 + 2.0 = 19.4, 19.4 -  4.5 = 14.9 nS

Typ Setup time = 13.4 - 3.5 = 9.9, 9.3 - 9.9 = -0.6 nS
Typ Hold time  = 13.4 + 1.5 = 14.9, 14.9 - 3.5 = 11.4 nS
**********************************************************
Setup and hold path:  5
Name of path:         RD-/WR- clock, AD1 - AD3 data, load
                      cntr RA8 - RA10

path RD-/WR- HL to FF clock input:

gate    output  delay
IP      HL      0.4 +  0       =   0.4
TTLIN   LH      8.3 +  0       =   8.3
I1      HL      1.6 + .2 * 1 =   1.8
I2      LH      1.8 + .3 * 4 =   3.0   counted 3 for tristate
AD2N    HL      4.7 + .3 * 1 =   5.0   FET driver 2 ands into
I1      LH      1.8 + .3 * 1 =   2.1   nor gate
NA2     HL      2.3 + .3 * 1 =   2.6
I1      LH      1.8 + .3 * 4 =   3.0
NA4     HL      4.8 + .6 * 1 =   5.4
I1      LH      1.8 + .3 * 1 =   2.1
I1      HL      1.6 + .2 * 2 =   2.0   -CSCNTR
I2      LH      1.8 + .3 * 6 =   3.6
NA3     HL      2.7 + .2 * 2 =   3.1
                              ------
                        total   42.4 nS
```

Comment: The above signal goes to the Preset and Clear inputs of the FF. Thus, the only requirement is that the AD1 - AD3 signals be valid until end of RD- or WR- at FF, plus hold time.

gate	output	delay				
TTLIN	HL	8.3	+	0	=	1.8
I2	LH	1.8	+	.3 * 3	=	2.7
					total	11.0 nS

WC Setup time = 42.4 - 11.0 = 31.4, 12.0 - 31.4 = -19.4 nS
WC Hold time = 42.4 + 2.0 = 44.4, 44.4 - 11.0 = 33.0 nS

Typ Setup time = 32.6 - 8.5 = 24.1, 9.3 - 24.1 = -14.8 nS
Typ Hold time = 32.6 + 1.5 = 34.1, 34.1 - 8.5 = 25.6 nS

****

Setup and hold path: 6
Name of path: ALE clock, AD5 or AD7 data, decoder 1 of 8

path ALE LH to FF clock input:

gate	output	delay				
IP	LH	0.4	+		=	0.4
TTLIN	HL	3.9	+	0 * 1	=	3.9
I1	LH	1.8	+	.3 * 1	=	2.1
I1	HL	1.6	+	.2 * 1	=	1.8
					total	8.2 nS

path AD5 to AD7 to FF D input:

gate	output	delay				
TTLIN	HL	3.9	+	0 * 1	=	3.9
I2	LH	1.8	+	.3 * 3	=	2.4
					total	6.3 nS

WC Setup time = 8.2 - 6.3 = 1.9, 12.0 - 1.9 = 10.1 nS
WC Hold time = 8.2 + 2.0 = 10.2, 10.2 - 6.3 = 3.9 nS

Typ Setup time = 6.3 - 4.8 = 1.5, 9.2 - 1.5 = 7.7 nS
Typ Hold time = 6.3 + 2.0 = 8.3, 8.3 - 4.8 = 3.5 nS

****

```
Setup and hold path:  7,8
Name of path:         IOR- clock, C/D- or I/O- data, clear BUSY
                      by IOR-
```

path IOR- LH to FF clock input:

gate	output	delay				
IP	LH	0.4	+		=	0.4
STP	HL	1.6	+	.2 * 1	=	1.8
I1	LH	1.8	+	.3 * 2	=	2.4
NA2	HL	2.3	+	.3 * 2	=	2.9
NA4	LH	3.1	+	.3 * 1	=	3.4
NA2	HL	2.3	+	.3 * 2	=	2.9
I2	LH	1.8	+	.3 * 6	=	3.6
I1	HL	1.6	+	.2 * 1	=	1.8
					total	19.2 nS

path C/D- or I/O- to FF D input:

gate	output	delay				
IP	LH	0.4	+	0	=	0.4
TTLIN	HL	3.9	+	0 * 2	=	3.9
I1	LH	1.8	+	.3 * 2	=	2.4
I1	HL	1.6	+	.2 * 1	=	1.8
NA2	LH	2.3	+	.3 * 2	=	2.9
					total	11.4 nS

```
WC Setup time = 19.2 - 11.4 = 7.8, 12.0 -  7.8 =  4.2 nS
WC Hold time  = 19.2 + 2.0 = 21.2, 21.2 - 11.4 =  9.8 nS

Typ Setup time = 14.8 - 8.8 = 6.0,  9.2 -  6.0 = 3.2 nS
Typ Hold time  = 14.8 + 2.0 = 16.8, 16.8 -  8.8 = 8.0 nS
**********************************************************
Setup and hold path:  9,10,11,12
Name of path:         IOR-/IOW- clock, C-/D or I/O- data,
                      generate polled DACC- to clock BUSY FF
                      generate DMA DACC- to clock BUSY FF
```

path IOR-/IOW- LH to FF clock input:

gate	output	delay					
IP	LH	0.4	+		=	0.4	
STP	HL	1.6	+	.2 * 1	=	1.8	
I1	LH	1.8	+	.3 * 2	=	2.4	
NA2	HL	2.3	+	.3 * 2	=	2.9	
NA4	LH	3.1	+	.3 * 1	=	3.4	
NA2	HL	2.3	+	.3 * 2	=	2.9	
I2	LH	1.8	+	.3 * 4	=	2.4	-DACC +clk
I1	HL	1.6	+	.2 * 2	=	2.0	DACC -clk
					total	18.2 nS	

Comment: Due to inverter to -clk input on FF, setup must be 2 nS earlier than the calculation result.

path C-/D or I/O- to FF D input:

gate	output	delay					
IP	LH	0.4	+	0	=	0.4	
TTLIN	HL	3.9	+	0 * 2	=	3.9	
I1	LH	1.8	+	.3 * 2	=	2.4	
I1	HL	1.6	+	.2 * 1	=	1.8	
NA2	LH	2.3	+	.3 * 2	+	2.9	
					total	11.4 nS	

WC Setup time = 18.2 - 11.4 = 6.8, 14.0 - 6.8 = 7.2 nS
WC Hold time = 18.2 + 2.0 = 20.2, 20.2 - 11.4 = 8.8 nS

Typ Setup time = 14.0 - 8.8 = 5.2, 10.8 - 5.2 = 5.6 nS
Typ Hold time = 14.0 + 2.0 = 16.0, 16.0 - 8.8 = 7.2 nS

****

Setup and hold path: 15
Name of path: RD-/WR- clock, AD0-AD7 data, within ECC section

One important setup & hold time is the AD0-AD7 relationship to the RD-/WR- signal. Internal signal SHIFT is false at this time.

path RD-/WR- to FF clock inputs:

gate	output	delay					
IP	LH	0.4	+	0	=	0.4	
TTLIN	HL	3.9	+	0	=	3.9	
I1	LH	1.6	+	.2 * 1	=	1.8	
I2	HL	1.8	+	.3 * 1	=	2.1	
TSD	LH	2.5	+	0	=	2.5	
I2	HL	1.6	+	.2 * 1	=	1.8	
FETs	LH	1.2	+	1.0	=	2.2	allow 12 pF
TTLIN	HL	3.9	+	0	=	3.9	
I2	LH	1.8	+	.3 * 2	=	2.4	REB/WEB
I1	HL	1.6	+	.2 * 1	=	1.8	
NA2	LH	2.3	+	.3 * 1	=	2.6	
NA3	HL	2.7	+	.2 * 1	=	2.9	
I3	LH	1.8	+	.3 * 1	=	2.1	CLKEN
I12	HL	1.6	+	.2 * 2	=	2.0	-SRCLK clocks all 32 FF's
I12	LH	1.8	+	.3 * 2	=	2.4	SRCLK clocks all 32 FF's
					total	34.8 nS	

path AD0-AD7 to FF D input:

gate	output	delay					
TTLIN	LH	8.3	+	0	=	8.3	
I2	HL	1.6	+	.2 * 3	=	2.2	ADI(0-7)
I1	LH	1.8	+	.3 * 1	=	2.1	
NO2	HL	3.1	+	.2 * 1	=	3.3	
XNR	LH	2.5	+	.3 * 2	=	3.1	estimate
I1	HL	1.6	+	.2 * 1	=	1.8	
XNR	LH	2.5	+	0	=	2.5	
						-------	
				total		23.3 nS	

WC Setup time = 34.8 - 23.3 = 11.5, 12.0 - 11.5 = 0.5 nS
WC Hold time = 34.8 + 2.0 = 36.8, 36.8 - 23.3 = 13.5 nS

Typ Setup time = 26.8 - 17.9 = 8.9, 9.2 - 8.9 = 0.3 nS
Typ Hold time = 26.8 + 2.0 = 28.8, 28.8 - 17.9 = 10.9 nS

****

Setup and hold path: 16
Name of path: WCLK frequency and symmetry

WCLK frequency and symmetry need specification.

WCLK period = 200 nS +/- 10 nS

WCLK high time = 100 nS +/- 10 nS
WCLK low time = 100 nS +/- 10 nS

Setup and hold path: 17
Name of path: WCLK clock, RD-/WR- data,
Synchronizing circuit, page 3, sect 2B

This circuit is designed so that REB or WEB can be totally asynchronous to the WCLK input. For this reason, there is no need to specify a timing relationship of REB or WEB to WCLK. However, in the WX2 case, since WCLK clocks both the 1010 and the Dewey, operation is synchronous.

The setup and hold times are NOT REQUIREMENTS since any relationship will work. Each byte will be handled by the ECC section in 0.8 to 1.0 uS. This falls well within the 1.6 uS per byte transfer rate of the 1010.

path WCLK HL to FF clock input:

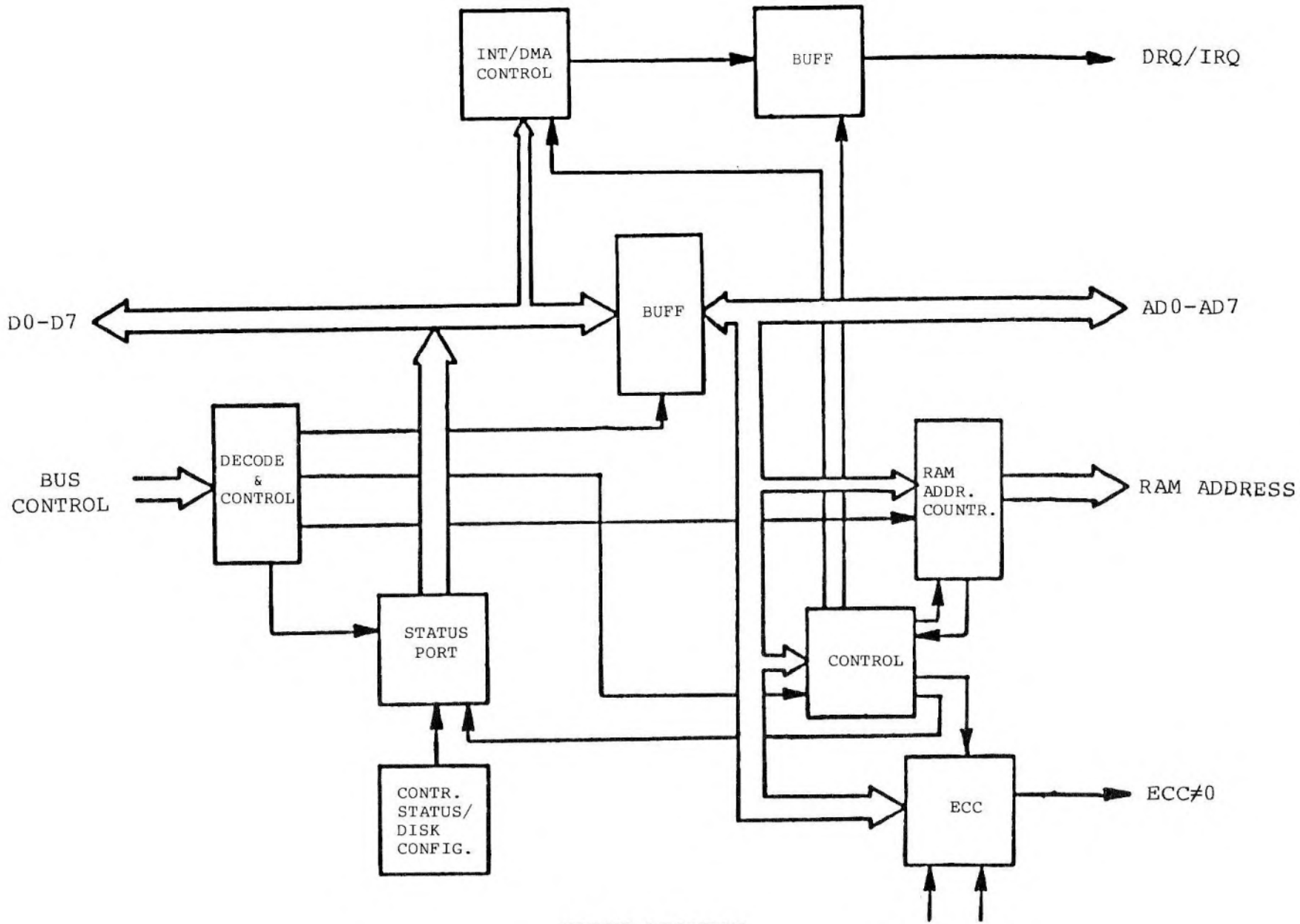
gate	output	delay					
IP	HL	0.4	+		=	0.4	
TTLIN	LH	8.3	+	0 * 1	=	8.3	
I1	HL	1.6	+	.2 * 1	=	1.8	
I1	LH	1.8	+	.3 * 1	=	2.1	+clk on FF
I1	HL	1.6	+	.2 * 1	=	1.8	-clk on FF
						------	
					total	14.4 nS	

path RD-/WR- to FF D input:

gate	output	delay					
TTLIN	HL	3.9	+	0	=	3.9	
I2	LH	1.8	+	.3 * 1	=	2.1	REB/WEB
I1	HL	1.6	+	.2 * 1	=	1.8	
NA2	LH	2.3	+	.3 * 1	=	2.6	
NA3	HL	2.7	+	.2 * 1	=	2.9	
I3	LH	1.8	+	.3 * 1	=	2.1	CLKEN
I12	HL	1.6	+	.2 * 1	=	1.8	-SRCLK
I12	LH	1.8	+	.3 * 1	=	2.1	SRCLK
FF	HL	5.0	+	.3 * 1	=	5.3	FF clk to Q out delay
						-------	
					total	24.6 nS	

WC Setup time = 14.4 - 24.6 = -10.2, 12.0 - (-10.2) = 22.2 nS
WC Hold time = 14.4 + 2.0 = 16.4, 16.4 - 24.6 = -8.2nS

Typ Setup time = 11.1 - 18.9 = -7.8, 9.2 - (-7.8) = 17.0 nS
Typ Hold time = 11.1 + 2.0 = 13.1, 13.1 - 18.9 = -5.8 nS



BLOCK DIAGRAM
WX2 GATE ARRAY

RADIO SHACK, A Division of Tandy Corporation

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CANADA: BARRIE, ONTARIO L4M 4W5

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